

Data Sheet



DiskOnChip Millennium MD2800, MD2810 8MB Single Chip Flash Disk

Features

- Single chip, easy-to-integrate, plug-and-play flash disk
- Low power, single 3.3V or 5V power supply
- 8MB (64Mbit) capacity
- Small form factor - available in 32-pin TSOP-II or DIP
- EDC/ECC for high data reliability
- Full boot capability with auto-loading boot page cache
- Broad O/S support: DOS, Windows 95 and 98, Windows NT 4.0, Windows CE, Embedded NT, pSOS+, QNX, VxWorks, Linux, and others
- O/S-less environment support
- Windows CE and Tornado native support
- Small (8KB) memory window size
- Embedded *TrueFFS*[®] technology provides:
 - Full hard-disk read/write and boot capability emulation
 - Third-generation wear leveling
 - Automatic block management
 - Power loss recovery
- Compatible with major processors: x86, MediaGX, PowerPC, 68K, MIPS, SHx, StrongARM, and others



Applications

- Embedded systems
- Internet access devices
- Internet set-top box or ITV, web browser
- WBT, thin client, network computer
- Routers, networking
- Web-phones, car-PC, DVD, HPC
- Point of sale
- Industrial PC's
- Telecom
- Medical

March 2000

1. General Description

The DiskOnChip Millennium is the third generation of M-Systems' DiskOnChip series of products. The Millennium series is the world's first monolithic solid state flash disk. It combines a disk controller with flash memory on a single die. DiskOnChip Millennium is available in a standard 32-pin DIP or 32-pin TSOP-II packages. DiskOnChip Millennium products are optimized for use where minimal weight, space, and power consumption are required, such as information appliances, set-top boxes, thin clients or network computers, thin servers, and embedded, portable PC-compatible computers. It is therefore a very attractive alternative to conventional hard and floppy disk drives.

The DiskOnChip family has been designed into more than 400 standard embedded motherboards, where it provides low cost, low power, high capacity, and high reliability flash-disk solutions.

DiskOnChip Millennium can be plugged into a standard DIP socket or soldered directly onto the motherboard, eliminating the need for mechanical disk drives, bulky ribbon cables, and connectors. The monolithic design of the DiskOnChip Millennium ensures high reliability even when subjected to levels of shock, vibration, and temperature changes that would destroy a conventional magnetic disk drive system.

Designed for ease of use and minimal integration overhead, the DiskOnChip Millennium can be pre-programmed for fast production or programmed on board during production. In addition, future software upgrades and formatting can be done on the target platform. There is no need to remove DiskOnChip Millennium from its socket to modify or reformat its contents.

2. Detailed Feature List

TrueFFS[®] Technology

TrueFFS is M-Systems' patented flash file system management technology. It allows flash components to fully emulate hard disks, so that they can be written to and read from like any other hard disk, rather than as a memory device. As such, it speeds up design and integration time. In addition, TrueFFS software simplifies and enhances the use of flash memory disks by:

- Using third generation wear leveling, which ensures that all blocks are erased an equal number of times; this increases the life of the flash media by orders of magnitude.
- Using virtual blocking of flash device to make erasure of large blocks transparent to the operator.
- Automatic block management – blocks that fail are automatically replaced from a pool of spares.
- Implementing a robust power-loss recovery mechanism to guarantee absolute protection of data.
- Providing conventional address support for 8-bit, 16-bit, and 32-bit architecture configurations. Support for the 16-bit and 32-bit bus architectures, commonly used in RISC processors, can be achieved by your using the LSB of the data bus as follows:
 - For 16-bit address boundary shifts, you should shift the address lines by *one*, so that the host address line A1 will connect to DiskOnChip address line A0, the host address line A2 will connect to DiskOnChip line A1, and so on.
 - For 32-bit address boundary shifts, you should shift the address lines by *two*, so that the host address line A2 will connect to DiskOnChip address line A0, the host address line A3 will connect to DiskOnChip line A1, and so on.

See application note AP-DOC-30 for further information.

Small Form Factor and Low Power

Integration of a flash disk on a single monolithic die gives the DiskOnChip Millennium unique features, including:

- Small footprint (32-pin TSOP-II or DIP packages).
- Low power consumption – Internal functions are synchronized with the CPU's read and write strobes. This innovation eliminates the need for an external clock. The design is completely static.
- Single 3.3V or 5V power supply.

These features make the DiskOnChip Millennium the best cost/performance solution for computers that require minimal weight, space, and power consumption, providing a very attractive alternative to conventional hard and floppy disk drives.

Temperature Ranges

The DiskOnChip Millennium is available in both commercial (0° to 70°C) and extended (-40° to +85 C) temperature ranges.

Capacity Ranges and Cascading

The TSOP version can be easily expanded from 8MB to 16MB, 24MB, or 32MB capacities by cascading up to four chips, without any additional glue logic.

The DIP version can be replaced in-socket by larger capacity products from the pin-compatible DiskOnChip 2000 family.

Easy Integration

The following DiskOnChip Millennium features ensure fast and easy integration:

- Compatible with standard EEPROM pin-out.
- Supports local bus and ISA bus interface.
- Includes a 512-byte, auto-loading, programmable boot page cache for IPL data.
- Small memory-mapped window size – requires only 8KB (can be used with larger window sizes).
- Static operation – no clock required.
- 16 mA output drive (5 mA at 3.3V).

Robust Error Correction

The DiskOnChip family utilizes a Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), providing the following error immunity for each 512-byte block of data:

- Correction of up to two 10-bit symbols, including two random bit errors.
- Correction of single bursts up to 11 bits.
- Detection of single bursts up to 31 bits and double bursts up to 11 bits.
- Detection of up to 4 random bit errors.

High Reliability

The DiskOnChip Millennium can be plugged into a standard DIP socket or soldered directly onto the motherboard, eliminating the need for mechanical disk drives, bulky ribbon cables, and connectors. The monolithic design of the DiskOnChip Millennium ensures high reliability even when subjected to levels of shock, vibration, and temperature changes that would destroy a conventional magnetic disk drive.

High Speed

The DiskOnChip Millennium implements a tightly coupled pipelined architecture for data transfers, eliminating bottlenecks typical in this area; it doubles read performance and significantly improves write performance in comparison to competitive alternatives. DiskOnChip Millennium can sustain a system write speed of over 550KB per second, read speed of more than 1.4MB per second (measured in ISA no wait state environment) and read/write burst transfer rates of nearly 13.3MB per second.

Compatibility with DiskOnChip 2000 Series

The DiskOnChip Millennium 32-pin DIP provides pin compatibility with the M-Systems DiskOnChip 2000 series of products.

The 32-pin TSOP package includes additional functionality such as busy signal and reset signal. There is easy expansion (no glue logic) from 8MB to 16MB, 24MB, or 32MB by using two, three, or four devices in the same 8KB memory-mapped window.

The TrueFFS driver automatically supports both the DiskOnChip Millennium and DiskOnChip 2000 series, starting with Version 1.21 and above.

Broad Operating System and Processor Support

The DiskOnChip family of products is supplied with TrueFFS firmware that supports a wide range of operating systems (O/S), including DOS, Windows 95/98/2000, Windows CE, Windows NT, and Windows Embedded NT.

Real time operating systems (RTOS) supported include QNX, VxWorks, pSOS, Linux, FreeBSD, PharLap ETS, and SMX.

In addition, leading operating systems such as Windows CE and Tornado offer native support for the DiskOnChip family of products for easy integration.

For O/S-less applications and customized solutions, M-Systems offers its DiskOnChip OSAK (Operating System Adaptation Kit), an ANSI-C source code kit designed specifically to support O/S-less environments.

The DiskOnChip family of products is compatible with all major processors, supporting popular processors such as x86, 68K, MediaGx, PowerPC, MIPS, SHx, StrongARM, and many others.

Portable solution – Shorter Time To Market

The development and integration time for implementing a flash disk is greatly reduced by DiskOnChip's standard software interface, which provides portability to other operating systems and processors and thereby shortens the time to market.

Complete Solution

The DiskOnChip Millennium series offers a full flash disk solution that includes different package and temperature options, evaluation boards, software drivers tailored to your operating system, data sheets, application support, and online e-mail support.

3. Package Description and Pin List

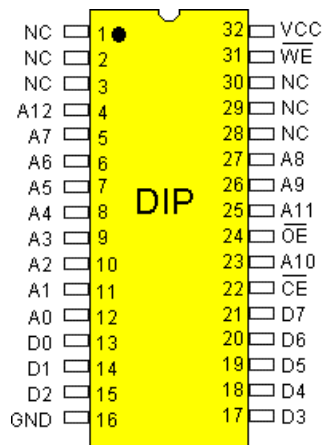


Figure 1: DIP Pin Out

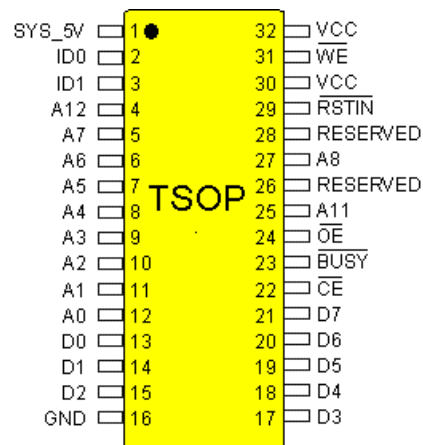


Figure 2: TSOP-II Pin Out

Pin Name	Description	Direction
A[12:0]	Address bus	Inputs
D[7:0]	Data bus	I/O
CE#	Chip Enable, active low	Input
OE#	Output Enable, active low	Input
WE#	Write Enable, active low	Input
SYS_5V	Connect to VCC for 5V systems or to GND for 3.3V systems (TSOP only)	Input
RSTIN#	Reset input, active low (TSOP only)	Input
BUSY#	Open drain; active low output indicates that the DiskOnChip Millennium is initializing and should not be accessed (TSOP only) .	Output
ID[1:0]	Configuration control inputs to support multiple chips cascaded in the same memory window (TSOP only) First chip - ID1, ID0 = GND, GND (0,0); must be set for one-chip configurations Second chip - ID1, ID0 = GND, VCC (0,1) Third chip - ID1, ID0 = VCC, GND (1,0) Fourth chip - ID1, ID0 = VCC, VCC (1,1)	Inputs
NC	No connection. These pins may be left floating, or tied to VCC, GND, or logic levels. Absolute Maximum Ratings must be observed.	
RESERVED	These pins are reserved for future expansion and must be left floating (TSOP only) .	
VCC	Power. All VCC pins must be connected.	
GND	Ground. All GND pins must be connected.	

4. Designing with the DiskOnChip Millennium Flash Disk

4.1. Hardware

The DiskOnChip Millennium should be connected as a standard memory device using standard memory interface signals. Typically, the DiskOnChip Millennium can be mapped to any free 8KB memory space. In a PC architecture, if the memory window allocated to the DiskOnChip Millennium is larger than 8KB, an automatic anti-aliasing mechanism prevents the firmware from being loaded more than once. Figure 3 illustrates a typical interface of the DiskOnChip Millennium to a system.

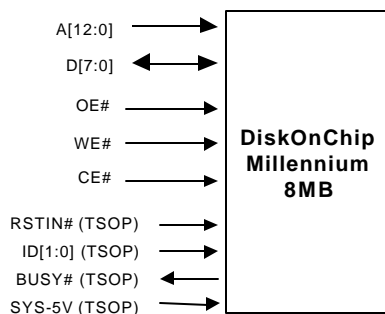


Figure 3: Simplified I/O Diagram

4.2. Fail-safe boot-block in DiskOnChip Millennium

The first 2KB and last 2KB (out of a total of 8KB) of the DiskOnChip Millennium memory window each include a single programmable, fail-safe, boot-block of 512 bytes. These 512 bytes are aliased four times in each 2KB. The last 2KB window is aliased to the first 2KB window, thereby delivering a 512-byte boot-block aliased a total of eight times.

This boot-block can be used by the CPU to fetch and execute instructions in place (XIP) at boot time, bypassing the NAND flash limitation. The boot-block usually includes basic hardware initialization code and the IPL (Initial Program Loader), which loads the rest of the platform initialization code and the SPL (Secondary Program Loader). These steps are followed by loading of the Operating System and execution of the application.

Figure 4 shows the DiskOnChip Millennium boot-block memory map.

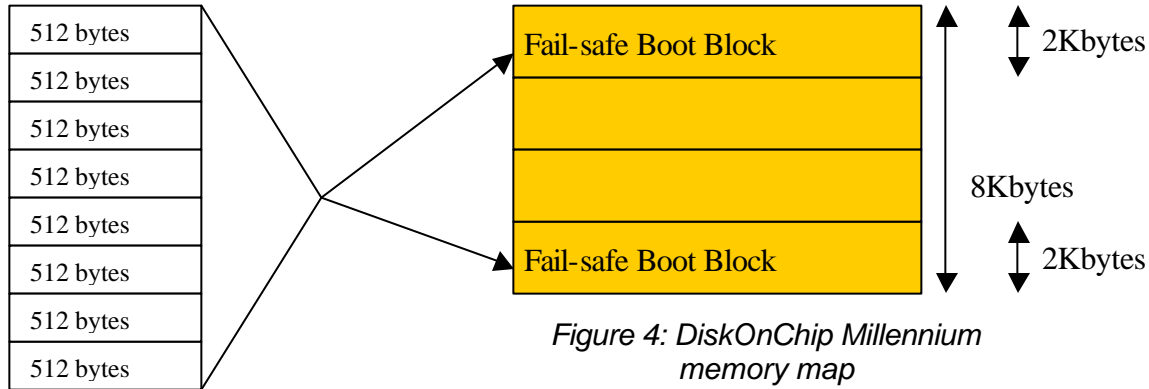


Figure 4: DiskOnChip Millennium memory map

4.3. Multiple Chip Configuration

Up to four TSOP DiskOnChip devices can be cascaded without external decoding circuitry. The ID[1:0] configuration inputs determine the identity of each DiskOnChip. Systems which employ only one DiskOnChip must configure the ID[1:0] inputs as {00}. Additional chips will be configured as {01}, {10}, and {11}.

When multiple DiskOnChip devices are connected using the ID[1:0] option, all I/O pins must be wired in common, including the BUSY# output if it is used by the host system.

4.4. Software

The DiskOnChip Millennium, under control of TrueFFS, is accessed using standard file system calls like any other block device. Applications can write to and read from any sector on the DiskOnChip Millennium, which is compatible with all diagnostic utilities, applications, and file systems.

The flash memory within DiskOnChip Millennium is accessed by TrueFFS through an 8KB window in the CPU's memory space. TrueFFS handles the paging of this window in the flash array, as well as providing flash disk emulation that includes flash table management, wear leveling, mapping out bad blocks, and background space reclamation of unused flash blocks.

The same 8KB address space will be retained in future versions of DiskOnChip Millennium that will offer greater capacities.

4.5. Designing the DiskOnChip Millennium into PC Architecture

When used in a PC-compatible architecture, the DiskOnChip Millennium should be allocated an 8KB memory window in the BIOS expansion memory range, which is usually located between 0C8000h and 0EFFFFh.

Figure 5 shows the DiskOnChip Millennium memory window in relation to the PC memory map.

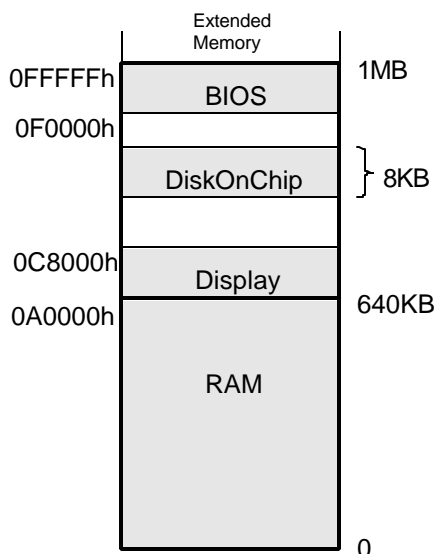


Figure 5: PC Memory Map

After reset, the BIOS first executes the POST (Power On Self-Test). Then the BIOS searches for all expansion ROM devices. When the DiskOnChip Millennium is found, the BIOS executes the Initial Program Loader (IPL) code located in the Boot-Block area of the DiskOnChip Millennium. This code loads the TrueFFS driver into system memory, installs the DiskOnChip Millennium as a disk in the system, and returns control back to the BIOS code. The operating system subsequently attempts to identify the disks that are available and the DiskOnChip Millennium software (TrueFFS) responds by emulating a hard disk.

From this point onward, DiskOnChip Millennium appears as a standard disk drive. It is assigned a drive letter and it can be used by any software application. No BIOS set-up modifications or autoexec.bat/config.sys modifications are required. No external software is required.

DiskOnChip Millennium can be used as the only disk in the system, in which case it will be accessed as drive C. It can work with or without a floppy drive, or with additional hard disks. When working with a hard disk, the DiskOnChip Millennium can be configured as the last drive (the default configuration). In this case, the hard disk will be C and the DiskOnChip Millennium will be D. It can also be configured as the first drive. In this case, the hard disk will be D and the DiskOnChip Millennium will be C.

DiskOnChip Millennium can be used as the boot device when configured as drive C. In this configuration, you must format the DiskOnChip Millennium as a bootable device by copying the OS files onto the disk. When running DOS, this can be done by using the SYS command.

5. Disk Capacities and Media Contents

5.1. Disk Capacities

Formatted capacities are given in the following table:

Product	Number of cascaded devices	Formatted Capacity (bytes) ¹	Sectors	Formatted Capacity under DOS 6.22 (bytes) ²	Sectors under DOS 6.22
MD2800-D08 (DIP)	None ³	8,151,040	15,920	8,128,512	15,876
MD2810-D08 (TSOP)	1	8,151,040	15,920	8,128,512	15,876
MD2810-D08 (TSOP)	2	16,375,808	31,984	16,324,608	31,884
MD2810-D08 (TSOP)	3	24,592,384	48,032	24,516,608	47,884
MD2810-D08 (TSOP)	4	32,817,152	64,096	32,724,992	63,916

5.2. Media Contents

The DiskOnChip Millennium DIP version is shipped from M-Systems already formatted and with a DOS driver.

The DiskOnChip Millennium TSOP version is shipped unformatted.

¹ Capacity reported by the driver after low-level formatting

² Capacity reported by the driver after high-level formatting using DOS 6.22 FAT file system

³ DIP package cannot be cascaded

6. Theory of Operation

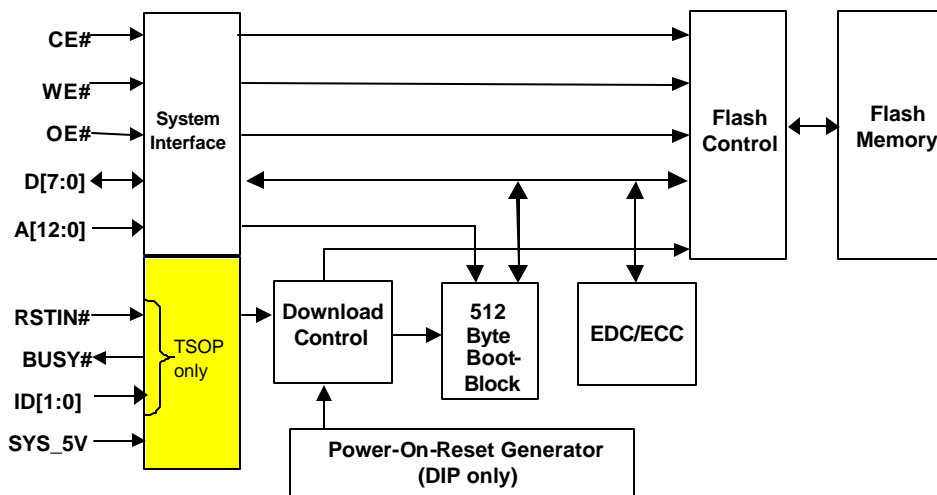


Figure 6: DiskOnChip Millennium Simplified Block Diagram

The DiskOnChip appears to the system as a standard EEPROM.

The DIP and TSOP versions of DiskOnChip Millennium are similar, except for the following:

- **RSTIN#:** The DIP contains an internal voltage detector and one-shot circuit to generate an internal reset pulse upon power-on. The TSOP provides a RSTIN# input that must be asserted by the host system upon power-on.
- **BUSY#:** The TSOP version has an open-drain BUSY# output signal that is asserted upon assertion of the RSTIN# input and remains asserted until the download operation (described below) has been completed. The DIP version has no BUSY# output and therefore requires a sufficient time delay before the first access to guarantee that the download operation is complete.
- **SYS_5V:** The TSOP version has an input that allows configuration for 3.3V or 5V voltage supply. The DIP version is not user configurable for voltage supply, but may be ordered in either 3.3V or 5V versions.
- **ID[1:0]:** The TSOP version has configuration control inputs for supporting multiple chips cascaded using the same memory window.

Upon power-up (DIP version) or the negation of the RSTIN# input (TSOP version), the DiskOnChip Millennium downloads the Initial Program Loader (IPL) data into the boot-block from the first 512 bytes of flash memory. As a failsafe mechanism, DiskOnChip Millennium uses its internal Error Detection and Correction (EDC/ECC) logic to verify the integrity of this data. If DiskOnChip Millennium detects an error, it will automatically download the redundant copy of the IPL, which is stored in the following page of the flash memory. The entire download process takes less than 1 millisecond. Access to the DiskOnChip Millennium is not permitted before the download process is completed.

At the completion of the download process, the host system can execute the IPL code from the boot-block. This code loads the TrueFFS software from the flash memory into the host's memory. This operation is necessary since the NAND-type flash memory does not support random access, and therefore cannot be used to execute the boot code. The firmware is identical for all DiskOnChip Millennium capacities, since TrueFFS automatically detects the memory capacity of the DiskOnChip Millennium. The boot-block can be used to initialize the platform hardware and to replace the external boot ROM.

6.1. EDC/ECC

DiskOnChip uses the Reed-Solomon ECC/EDC algorithm to ensure high data reliability. Each time a block of data is written to the flash, a six-byte checksum is also written. Each time the data is read back from the flash, a new six-byte code is computed. TrueFFS uses these checksums for error detection and, if necessary, error correction.

7. Package Selection

The DiskOnChip Millennium DIP package is pin-to-pin compatible with standard 32-pin EEPROM devices. M-Systems is dedicated to supporting this pin-out with the DiskOnChip Millennium and with all future DiskOnChip products. The 32-pin TSOP-II package is offered to meet the requirements of applications in which height and space are critical factors, and a surface mount package is desirable.

8. Signal Integrity

The DiskOnChip Millennium derives its internal clock signal from the CE#, OE#, and WE# inputs. Since access to the DiskOnChip Millennium registers is volatile in nature, much like a FIFO or UART, special care should be taken to ensure that these signals have clean rising and falling edges, free from ringing that could be interpreted as multiple edges. To guarantee proper operation, printed circuit board traces for these three signals should either be kept short or be properly terminated.

9. Electrical Specifications

9.1. Absolute Maximum Ratings

Parameter	Symbol	Rating ¹	Units	Notes
DC supply voltage	V_{CC}	-0.3 to 6.0	V	
Input pin voltage	V_{IN}	-0.3 ² to 6.6	V	
Input pin current	I_{IN}	-10 to 10	mA	25°C
Lead temperature	T_{LEAD}	260	°C	10 Sec

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: The voltage on any pin may undershoot to -2.0V or overshoot to 8.6V for <20ns.

9.2. Capacitance

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	10	pF

Note: Capacitance is not 100% tested.

9.3. Operating and Storage Temperature Ranges

Commercial operating temperature	0°C to +70°C
Extended operating temperature	-40°C to +85°C
Storage temperature (commercial and extended))	-55°C to +150°C

9.4. Humidity

10%-90% relative, non-condensing.

9.5. Endurance

Commercial operating temperature	1,000,000 W/E cycles
Extended operating temperature	300,000 W/E cycles

9.6. DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
V _{cc}	Supply Voltage	SYS_5V = 1	4.5	5.0	5.5	V	
		SYS_5V = 0	3.0	3.3	3.6	V	
V _{ih}	High Level Input Voltage	SYS_5V input V _{cc} = 5.5V	3.2			V	
		SYS_5V input V _{cc} = 3.6V	2.1			V	
		All other inputs	2.1			V	
V _{il}	Low Level Input Voltage				0.7	V	
V _{hys}	Hysteresis	All inputs	0.4			V	
I _{ohmax}	Maximum High Level Output Current	V _{cc} > 4.5V D outputs	-16			mA	
		V _{cc} < 4.5V D outputs	-5			mA	
I _{olmax}	Maximum Low Level Output Current	V _{cc} > 4.5V D outputs	16			mA	
		V _{cc} > 4.5V BUSY# output	8			mA	
		V _{cc} < 4.5V D outputs	5			mA	
		V _{cc} < 4.5V BUSY# output	3			mA	
V _{oh}	High Level Output Voltage	I _{oh} = I _{ohmax}	2.4			V	
V _{OL}	Low Level Output Voltage	I _{ol} = I _{olmax}			0.4	V	
I _{IL}	Input Leakage Current	SYS_5V input			-200	μA	1
		All other inputs			±10	μA	
I _{oz}	Output Leakage Current				±10	μA	
I _{cc}	Active Supply Current	Cycle Time = 100 nS, outputs open V _{cc} = 5.0V		25	45	mA	
		V _{cc} = 3.3V		16	30	mA	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Notes
lccs	Standby Supply Current	CE# > Vcc-0.2V All other inputs: Vin < 0.2V or Vin > Vcc-0.2V			100	μA	

¹ SYS_5V is internally pulled up for <180 mS at power-on. During this time the maximum input current of this pin is -200 μA.

9.7. AC Operating Conditions

Timing specifications are based on the following conditions:

Parameter	Value
Ambient Temperature (TA)	-40° to +85° C
Supply Voltage	5V ± 0.5V or 3.3V ± 0.3V
Input Pulse Level	0.4V to 2.6V
Input Rise and Fall Times	5 nS
Input Timing Levels	0.8V and 2.0V
Output Timing Levels	1.5V
Output Load all other outputs	100 pF

9.8. Timing Specifications

9.8.1. Read Cycle Timing

Symbol (refer to Figure 6)	Description	3.3V		5V		Units	Notes
		Min	Max	Min	Max		
Tsu(A)	Address to OE# ↓ setup time	0		0		nS	
THo(A)	OE# ↑ to Address hold time	0		0		nS	
Tsu(CE0)	CE# ↓ to OE# ↓ setup time	—		—		nS	1
THo(CE0)	OE# ↑ to CE# ↑ hold time	—		—		nS	2
THo(CE1)	OE# or WE# ↑ to CE# ↓ hold time	8		7		nS	
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	8		7		nS	
TREC(OE)	OE# negated to start of next cycle	11		10		nS	
TACC	Read access time (RAM)		130		85	nS	
	Read access time (all other addresses)		100		65	nS	
TLOZ(D)	OE# ↓ to D driven	20		18		nS	
THIZ(D)	OE# ↑ to D Hi-Z delay		20		17	nS	

¹ CE# may be asserted any time before or after OE# is asserted. If CE# is asserted after OE#, all timing relative to OE# asserted should instead be referenced to the time CE# was asserted.

² CE# may be negated any time before or after OE# is negated. If CE# is negated before OE#, all timing relative to OE# negated should instead be referenced instead to the time CE# was negated.

Note: RAM is accessed during read operations from addresses 0000h-07FFh and 1800h-1FFFh and is accessed only during the boot process.

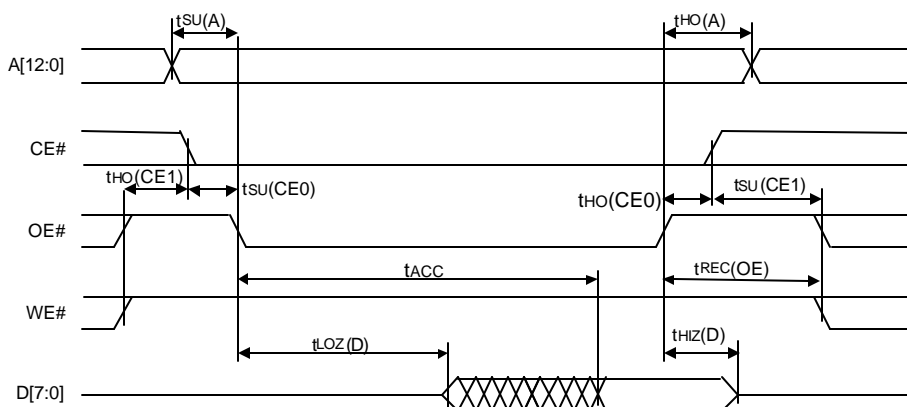


Figure 7: Read Cycle Timing

9.8.2. Write Cycle Timing

Symbol (refer to Figure 7)	Description	3.3V		5V		Units	Notes
		Min	Max	Min	Max		
tsu(A)	Address to WE# ↓ setup time	0		0		nS	
tHO(A)	WE# ↑ to Address hold time	0		0		nS	
Tw(WE)	WE# asserted width	65		46		nS	
Tsu(CE0)	CE# ↓ to WE# ↓ setup time	—		—		nS	1
THo(CE0)	WE# ↑ to CE# ↑ hold time	—		—		nS	2
THo(CE1)	OE# or WE# ↑ to CE# ↓ hold time	8		7		nS	
Tsu(CE1)	CE# ↑ to WE# ↓ or OE# ↓ setup time	8		7		nS	
TREC(WE)	WE# ↑ to start of next cycle	11		10		nS	
tsu(D)	D to WE# ↑ setup time	43		29		nS	
tHO(D)	WE# ↑ to D hold time	0		0		nS	

¹ CE# may be asserted any time before or after WE# is asserted. If CE# is asserted after WE#, all timing relative to WE# asserted should instead be referenced to the time CE# was asserted.

² CE# may be negated any time before or after WE# is negated. If CE# is negated before WE#, all timing relative to WE# negated will be referenced instead to the time CE# was negated.

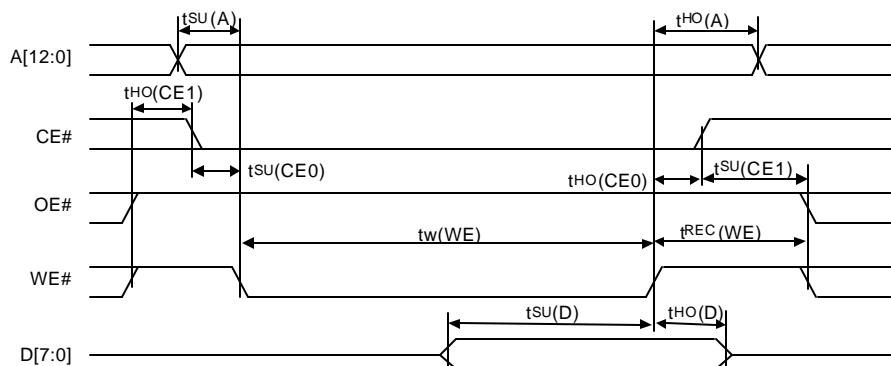


Figure 8: Write Cycle Timing

9.8.3. Power-on Timing

DiskOnChip Millennium devices in the TSOP version are reset based on the state of the RSTIN# input. DiskOnChip Millennium devices in the DIP version generate an internal reset pulse on power-on, which is asserted for a maximum of 165 mS after VCC has reached the minimum operating voltage. For either device, when the reset condition is negated, the DiskOnChip Millennium will initiate the download procedure from flash memory into the internal IPL RAM.

Note: Host systems must keep requirements described below for first access of the DiskOnChip Millennium.

DIP Package Power-on Timing

The DIP version power-on timing is shown in Figure 8 and Table 4 below. It is illegal for the host to access the DiskOnChip Millennium before the internal RESET signal has been negated and the download process completed, therefore the host must delay $t_{REC}(VCC-CE)$ before the first access to the DiskOnChip Millennium.

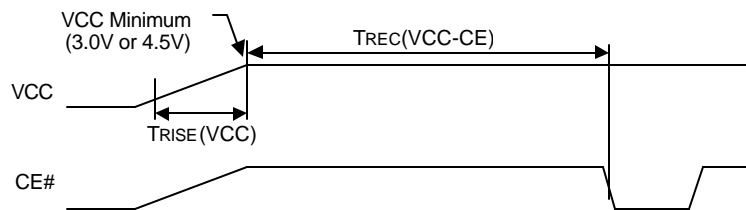


Figure 9: Reset Timing – DIP Package

Symbol (refer to Figure 8)	Description	Min	Max	Units	Notes
$T_{rec}(VCC-CE)$	VCC stable to first access	165		mS	
$T_{rise}(VCC)$	VCC rise time		44	mS	1

¹ Specified as the first positive crossing above 0.5V to the final positive crossing above 3.0V or 4.5V.

TSOP Package Power-on Timing

The TSOP version power-on timing is shown in Figure 9 and Table 5 below. Hosts may employ any of the following methods to guarantee the timing requirements of the first access to the DiskOnChip Millennium:

- Use a software timing loop to wait at least $t_p(\text{BUSY1})$ before accessing the DiskOnChip Millennium after the reset pulse is negated.
- Poll the state of the BUSY# output.
- Use the BUSY# output to hold the host in a wait state before completing the first access.

Note: Host systems that boot from the DiskOnChip Millennium must employ the last option (holding host in wait state), or use another method that guarantees the required timing of the first access.

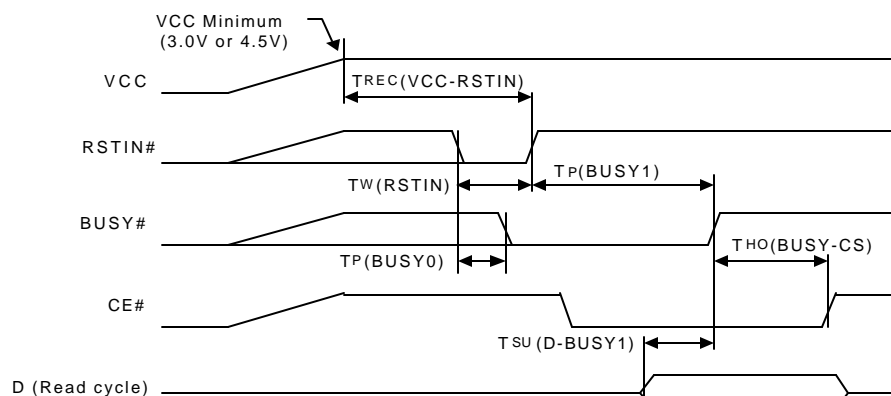


Figure 10: Reset Timing – TSOP Package

Symbol (Refer to Figure 9)	Description	Min	Max	Units	Notes
$t_{rec}(\text{VCC-RSTIN})$	VCC stable to RSTIN# ↑	100		nS	1
$t_w(\text{RSTIN})$	RSTIN# asserted pulse width	22		nS	
$t_p(\text{BUSY0})$	RSTIN# ↓ to BUSY# ↓		51	nS	
$t_p(\text{BUSY1})$	RSTIN# ↑ to BUSY# ↑		370	μS	3
$t_{h0}(\text{BUSY-CE})$	BUSY# ↑ to CE# ↑	0		nS	2
$t_{su}(\text{D-BUSY1})$	Data valid to BUSY# ↑	0		nS	2

¹ Specified as the first positive crossing above 0.5V to the final positive crossing above 3.0V or 4.5V.

² Normal read/write cycle timing applies. This parameter applies only to the case when the cycle is extended until the negation of the BUSY# signal.

³ If the assertion of RSTIN# occurs during a flash erase cycle, this time could reach a maximum of 500 μS.

10. Mechanical Specifications

10.1. Thermal Characteristics

Thermal characteristics for each of the package options are shown in the following table.

Package	Thermal Resistance ($^{\circ}\text{C/W}$)	
	Junction to Case (q_{JC})	Junction to Ambient (q_{JA})
DIP	25	60
TSOP	25	85

10.2. Package Dimensions

10.2.1. DIP Dimensions

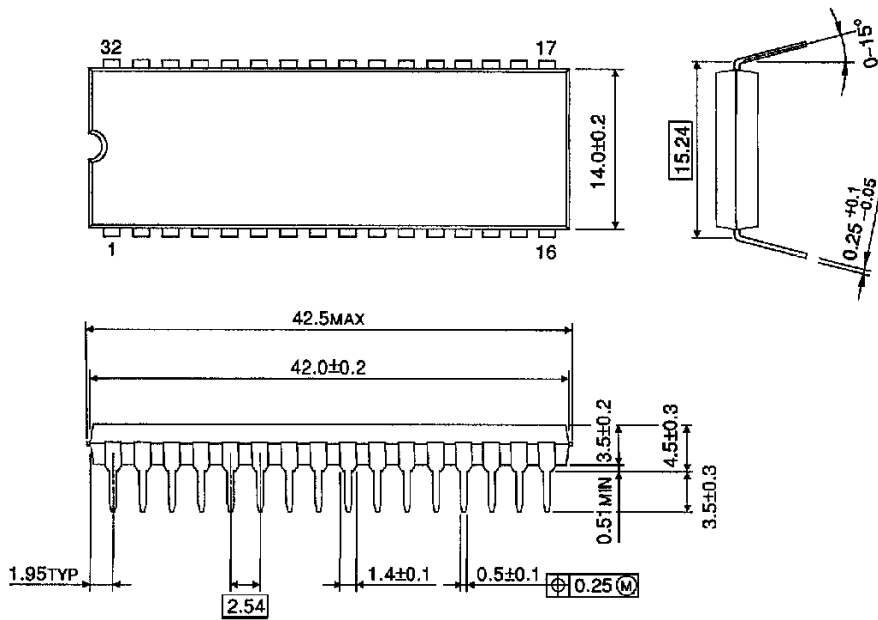


Figure 11: DIP Package Dimensions

10.2.2. TSOP Dimensions

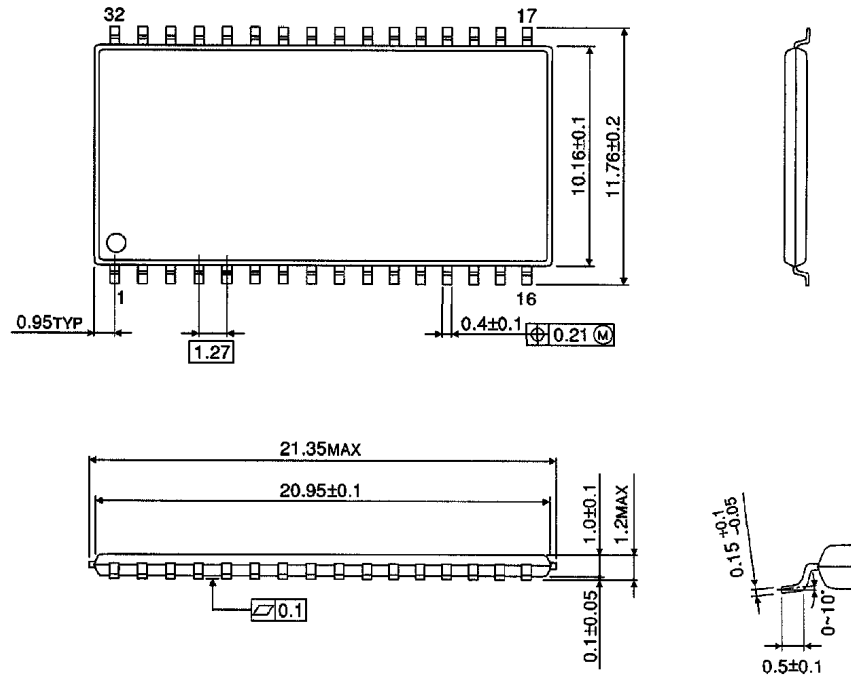


Figure 12: TSOP Package Dimensions

11. Ordering Information

MD-2800-DCC-V-T (DIP-32 Package)

CC: Capacity (MB) 08
V: Supply Voltage Blank 5V
V3 3.3V
T: Temperature Range Blank Commercial 0°C to +70°C
X Extended -40°C to +85°C

MD-2810-DCC-T (TSOP-II-32 Package)

CC: Capacity (MB) 08
T: Temperature Range Blank Commercial 0°C to +70°C
X Extended -40°C to +85°C

12. Additional Information

Document/Tool	Description
DiskOnChip Utilities	DiskOnChip Utilities User Manual
DiskOnChip Quick Installation Guide	DiskOnChip Quick Installation Guide
AP-DOC-10	Application Note: Designing with DiskOnChip DIP
AP-DOC-16	Application Note: Using DiskOnChip with QNX
AP-DOC-17	Application Note: Using DiskOnChip with Windows CE
AP-DOC-020	Application Note: DiskOnChip Boot Developers Kit
IM-DOC-21	Application Note: Using DiskOnChip with Linux O/S
IM-DOC-22	Application Note: Using DiskOnChip with VxWorks
AP-DOC-30	Application note - Designing with DiskOnChip Millennium in a RISC Environment
AP-DOC-31	Application note - Designing with DiskOnChip Millennium in a PC Environment
AP-DOC-39	Application Note: Onboard Programming of the DiskOnChip Millennium
DiskOnChip OSAK Product Brief	DiskOnChip OSAK Product Brief
DiskOnChip DIP EVB	DiskOnChip DIP Evaluation Board
DiskOnChip Millennium EVB	DiskOnChip Millennium Evaluation Board
DiskOnChip GANG Programmer	DiskOnChip 1+8 Gang Programmer
DiskOnChip ZIF Adapter	DiskOnChip Millennium TSOP-II ZIF Adapter for the GANG Programmer

How to Contact Us

Internet: <http://www.m-sys.com>

E-mail: info@m-sys.com

USA Office:

M-Systems Inc.
8371 Central Ave, Suite A
Newark CA 94560, U.S.A
Phone: 1-510-494-2090
Fax: 1-510-494-5545

Japan Office:

M-Systems Japan Inc.
1-11-15 Higashi Gotonda Shinagawa-ku
Tokyo, 141-0022 Japan
Phone: 81-3-3445-9042
Fax: 81-3-3445-9045

Taiwan Office:

M-System Asia Ltd.
11F-2, No. 81, Sec.2, Chang Teh Rd.
Taipei, Taiwan, R.O.C.
Phone: 886-2-2550-1741
Fax: 886-2-2550-1745

U.K. Office:

M-Systems UK Ltd.
PO Box 20
Chalgrove SPDO
OX44 7YP
Phone: 44-1865-891-123
Fax: 44-1865-891-391

Israel Office:

M-Systems Ltd.
Atidim Industrial Park P.O.B 58036
Tel Aviv 61580, Israel
Phone: 972-3-647-7776
Fax: 972-3-647-6668

M-Systems assumes no responsibility for the use of the material described in this document. Information contained herein supersedes previously published specifications for this device from M-Systems. M-Systems reserves the right to change this document without notice.