ANALOG
DEVICES

Dual, Low Noise, Single-Supply Variable Gain Amplifier

AD605

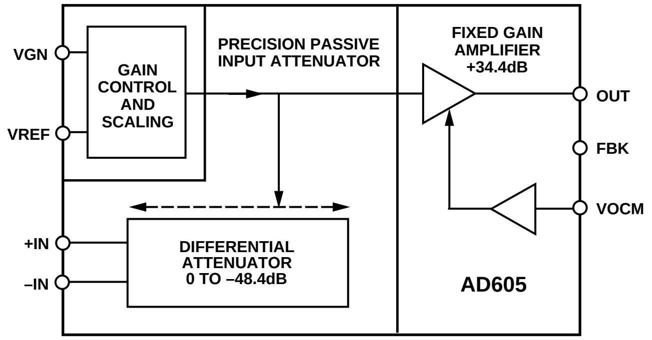
FEATURES

- **Two Independent Linear-in-dB Channels**
- **Input Noise at Maximum Gain: $1.8\ \text{nV}/\sqrt{\text{Hz}}$, $2.7\ \text{pA}/\sqrt{\text{Hz}}$**
- **Bandwidth: 40 MHz (–3 dB)**
- **Differential Input**
- **Absolute Gain Range Programmable:**
  –14 dB to +34 dB (FBK Shorted to OUT), through
  0 dB to +48 dB (FBK Open)
- **Variable Gain Scaling: 20 dB/V through 40 dB/V**
- **Stable Gain with Temperature and Supply Variations**
- **Single-Ended Unipolar Gain Control**
- **Output Common-Mode Independently Set**
- **Power Shutdown at Lower End of Gain Control**
- **Single +5 V Supply**
- **Low Power: 90 mW/Channel**
- **Drives A/D Converters Directly**

APPLICATIONS

- **Ultrasound and Sonar Time-Gain Control**
- **High Performance AGC Systems**
- **Signal Measurement**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD605 is a low noise, accurate, dual channel, linear-in-dB variable gain amplifier, which is optimized for any application requiring high performance, wide bandwidth variable gain control. Operating from a single +5 V supply, the AD605 provides differential inputs and unipolar gain control for ease of use. Added flexibility is achieved with a user determined gain range and an external reference input which provides user determined gain scaling (dB/V).

The high performance linear-in-dB response of the AD605 is achieved with the differential input, single supply, exponential amplifier (DSX-AMP) architecture. Each of the DSX-AMPs comprise a variable attenuator of 0 dB to –48.4 dB followed by a high speed fixed gain amplifier. The attenuator is based on a 7 stage R-1.5-R ladder network. The attenuation between tap points is 6.908 dB and 48.360 dB for the entire ladder network. The DSX-AMP architecture results in $1.8\ \text{nV}/\sqrt{\text{Hz}}$ input noise spectral density and will accept a ±2.0 V input signal when VOCM is biased at VP/2.

Each independent channel of the AD605 provides a gain range of 48 dB which can be optimized for the application. Gain ranges between –14 dB to +34 dB and 0 dB to +48 dB can be selected by a single resistor between pins FBK and OUT. The lower and upper gain range are determined by shorting pin FBK to OUT, or leaving pin FBK unconnected respectively. The two channels of the AD605 can be cascaded to provide 96 dB of very accurate gain range in a monolithic package.

The gain control interface provides an input resistance of approximately 2 MΩ and scale factors from 20 dB/V to 30 dB/V for a VREF input voltage of 2.5 V to 1.67 V respectively. Note that scale factors up to 40 dB are achievable with reduced accuracy for scales above 30 dB. The gain scales linearly with control voltages (VGN) of 0.4 V to 2.4 V for the 20 dB/V scale and 0.20 V to 1.20 V for the 40 dB/V scale. When VGN is <50 mV the amplifier is powered-down to draw 1.9 mA. Under normal operation, the quiescent supply current of each amplifier channel is only 18 mA.

The AD605 is available in a 16-pin plastic DIP and SOIC, and is guaranteed for operation over the –40°C to +85°C temperature range.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

AD605–SPECIFICATIONS

(Each Channel at T_A = +25°C, V_S = +5 V, R_S = 50 Ω, R_L = 500 Ω, C_L = 5 pF, VREF = 2.5 V (Scaling = 20 dB/V) , –14 dB to +34 dB gain range, unless otherwise noted.)

Model		**AD605A**			**AD605B**			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
INPUT CHARACTERISTICS								
Input Resistance			175 ± 40			175 ± 40		Ω
Input Capacitance			3.0			3.0		pF
Peak Input Voltage			2.5 ± 2			2.5 ± 2		V
Input Voltage Noise	VGN = 2.9 V		1.8			1.8		nV/$\sqrt{\text{Hz}}$
Input Current Noise	VGN = 2.9 V		2.7			2.7		pA/$\sqrt{\text{Hz}}$
Noise Figure	R_S = 50 Ω, f = 1 MHz, VGN = 2.9 V		8.4			8.4		dB
	R_S = 200 Ω, f = 1 MHz, VGN = 2.9 V		12			12		dB
Common-Mode Rejection Ratio	f = 1 MHz, VGN = 2.65 V		–20			–20		dB
OUTPUT CHARACTERISTICS								
–3 dB Bandwidth	Constant with Gain		40			40		MHz
Slew Rate	VGN = 1.5 V, Output = 1 V Step		170			170		V/µs
Output Signal Range	$R_L \geq$ 500 Ω		2.5 ± 1.5			2.5 ± 1.5		V
Output Impedance	f = 10 MHz		2			2		Ω
Output Short-Circuit Current			±40			±40		mA
Harmonic Distortion	VGN = 1 V, VOUT = 1 V p-p,							
HD2	f = 1 MHz		–64			–64		dBc
HD3	f = 1 MHz		–68			–68		dBc
HD2	f = 10 MHz		–51			–51		dBc
HD3	f = 10 MHz		–53			–53		dBc
Two-Tone Intermodulation	R_S = 0 Ω, VGN = 2.9 V, VOUT = 1 V p-p							
Distortion (IMD)	f = 1 MHz		–72			–72		dBc
	f = 10 MHz		–60			–60		dBc
1 dB Compression Point	f = 10 MHz, VGN = 2.9 V, Output Referred		+15			+15		dBm
3rd Order Intercept	f = 10 MHz, VGN = 2.9 V, VOUT = 1 V p-p, Input Referred		–1			–1		dBm
Channel-to-Channel Crosstalk	Ch1: VGN = 2.65 V, Inputs Shorted, Ch2: VGN = 1.5 V (Mid Gain), f = 1 MHz, VOUT = 1 V p-p		–70			–70		dB
Group Delay Variation	1 MHz < f < 10 MHz, Full Gain Range		±2.0			±2.0		ns
VOCM Input Resistance			45			45		kΩ
ACCURACY								
Absolute Gain Error								
–14 dB to –11 dB	0.25 V < VGN < 0.40 V	–1.2	+1.0	+3.0	–1.2	+0.75	+3.0	dB
–11 dB to +29 dB	0.40 V < VGN < 2.40 V	–1.0	±0.3	+1.0	–1.0	±0.2	+1.0	dB
+29 dB to +34 dB	2.40 V < VGN < 2.65 V	–3.5	–1.25	+1.2	–3.5	–1.25	+1.2	dB
Gain Scaling Error	0.4 V < VGN < 2.4 V		±0.25			±0.25		dB/V
Output Offset Voltage	VREF = 2.500 V, VOCM = 2.500 V	–50	±30	50	–50	±30	50	mV
Output Offset Variation	VREF = 2.500 V, VOCM = 2.500 V		30	95		30	50	mV
GAIN CONTROL INTERFACE								
Gain Scaling Factor	VREF = 2.5 V, 0.4 V < VGN < 2.4 V	19	20	21	19	20	21	dB/V
	VREF = 1.67 V		30			30		dB/V
Gain Range	FBK Short to OUT		–14 – +34			–14 – +34		dB
	FBK Open		0 – +48			0 – +48		dB
Input Voltage (VGN) Range	20 dB/V, VREF = 2.5 V		0.1 – 2.9			0.1 – 2.9		V
Input Bias Current			–0.4			–0.4		µA
Input Resistance			2			2		MΩ
Response Time	48 dB Gain Change		0.2			0.2		µs
POWER SUPPLY								
Power Dissipation			90			90		mW
VREF Input Resistance			10			10		kΩ
Quiescent Supply Current	VPOS		18	23		18	23	mA
Power Down	VPOS, VGN < 50 mV		1.9	3.0		1.9	3.0	mA
Power-Up Response Time	48 dB Gain, V_{OUT} = 2 V p-p		0.6			0.6		µs
Power-Down Response Time			0.4			0.4		µs

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $+V_S$	
Pins 12, 13 (with Pins 4, 5 = 0 V)	+6.5 V
Input Voltages	
Pins 2, 3, 6, 7	VPOS/2 ±2 V Continuous
Pins 1, 8, 9, 16	VPOS, 0
Internal Power Dissipation	
Plastic (N)	1.4 W
Small Outline (R)	1.2 W
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature, Soldering 60 seconds	+300°C

NOTES

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

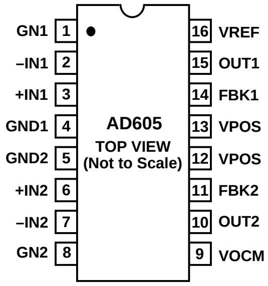
[2] When driven from an external low impedance source.

ORDERING GUIDE

Model	Temperature Range	Package Option*	θ_{JA}
AD605AN	–40°C to +85°C	N-16	85°C/W
AD605AR	–40°C to +85°C	R-16A	100°C/W
AD605BN	–40°C to +85°C	N-16	85°C/W
AD605BR	–40°C to +85°C	R-16A	100°C/W

*N = Plastic DIP, R = Small Outline IC (SOIC).

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD605 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTIONS
16-Pin Package for Dual Channel AD605

Pin No.	Mnemonic	Description
1	VGN1	CH1 Gain-Control Input and Power-Down Pin. If grounded, device is off, otherwise positive voltage increases gain.
2	–IN1	CH1 Negative Input.
3	+IN1	CH1 Positive Input.
4	GND1	Ground.
5	GND2	Ground.
6	+IN2	CH2 Positive Input.
7	–IN2	CH2 Negative Input.
8	VGN2	CH2 Gain-Control Input and Power-Down Pin. If grounded, device is off, otherwise positive voltage increases gain.
9	VOCM	Input to this pin defines common-mode voltage for OUT1 and OUT2.
10	OUT2	CH2 Output.
11	FBK2	Feedback Pin that Selects Gain Range of CH2.
12	VPOS	Positive Supply.
13	VPOS	Positive Supply.
14	FBK1	Feedback Pin that Selects Gain Range of CH1.
15	OUT1	CH1 Output.
16	VREF	Input to this pin sets gain-scaling for both channels: 2.5 V = 20 dB/V, 1.67 V = 30 dB/V.

AD605–Typical Performance Characteristics (per Channel)

(V_{REF} = 2.5 V (20 dB/V Scaling), f = 1 MHz, R_L = 500 Ω, C_L = 5 pF, T_A = 25°C, V_{SS} = +5 V)

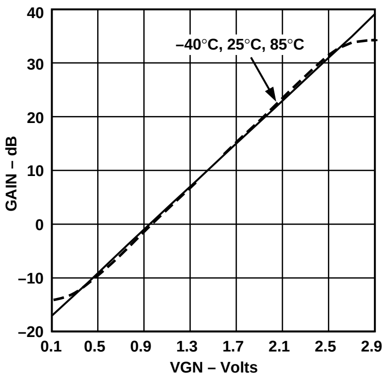


Figure 1. Gain vs. VGN

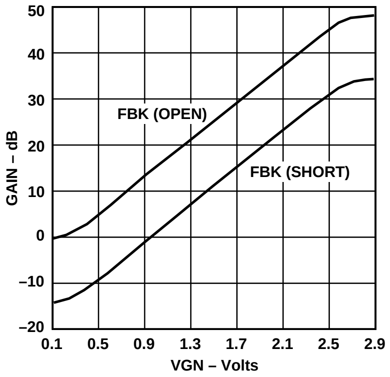


Figure 2. Gain vs. VGN for Different Gain Ranges

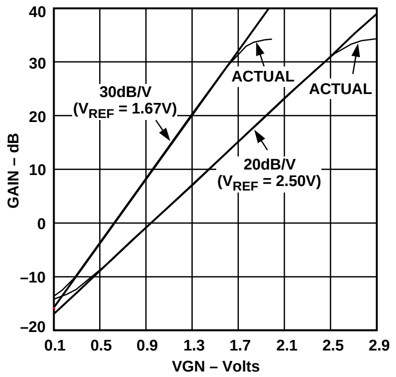


Figure 3. Gain vs. VGN for Different Gain Scalings

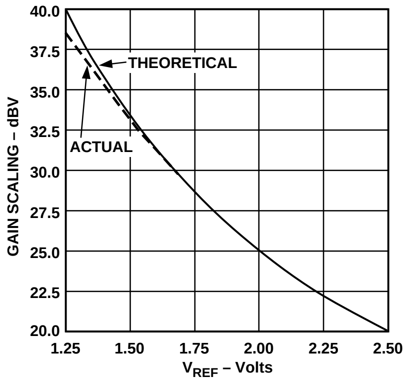


Figure 4. Gain Scaling vs. V_{REF}

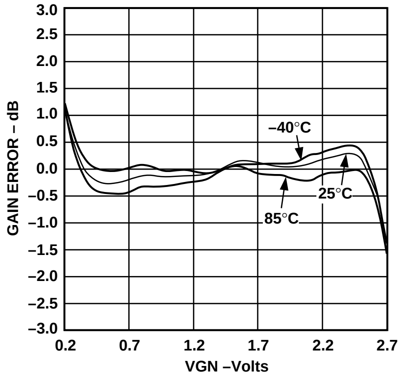


Figure 5. Gain Error vs. VGN at Different Temperatures

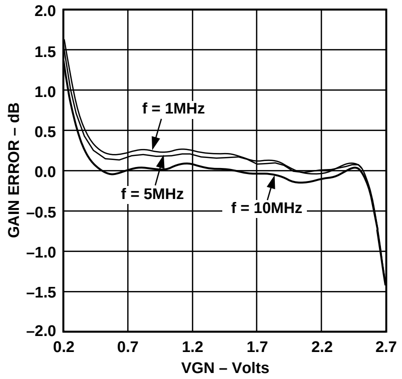


Figure 6. Gain Error vs. VGN at Different Frequencies

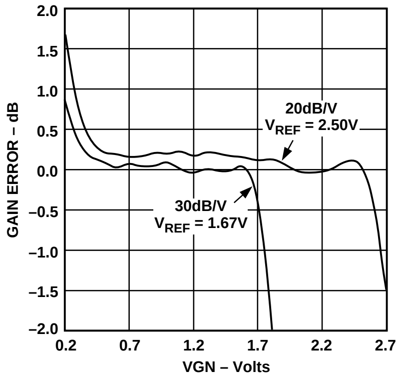


Figure 7. Gain Error vs. VGN for Different Gain Scalings

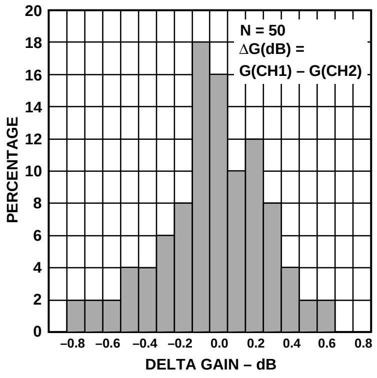


Figure 8. Gain Match, VGN1 = VGN2 = 1.0 V

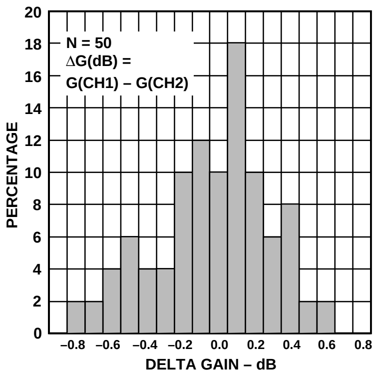


Figure 9. Gain Match, VGN1 = VGN2 = 2.50 V

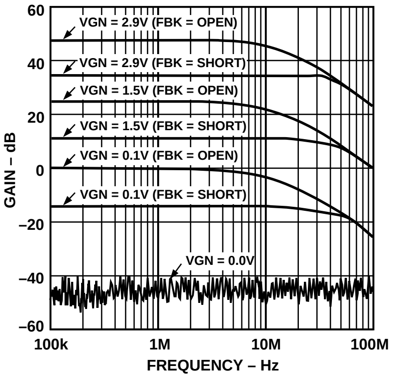


Figure 10. AC Response

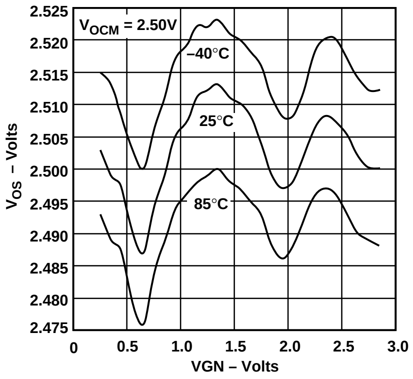


Figure 11. Output Offset vs. VGN

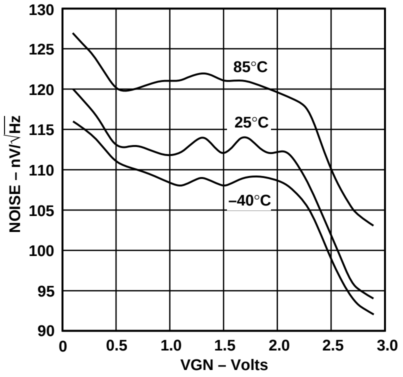


Figure 12. Output Referred Noise vs. VGN

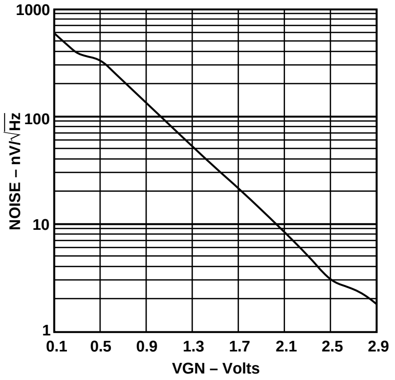


Figure 13. Input Referred Noise vs. VGN

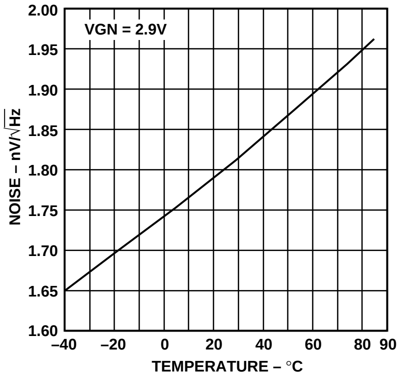


Figure 14. Input Referred Noise vs. Temperature

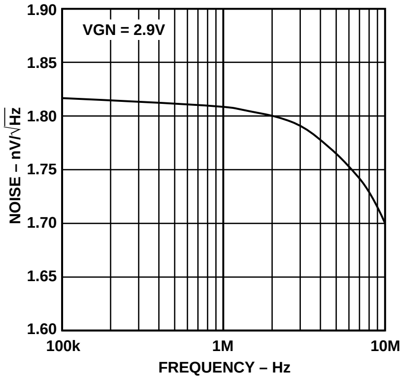


Figure 15. Input Referred Noise vs. Frequency

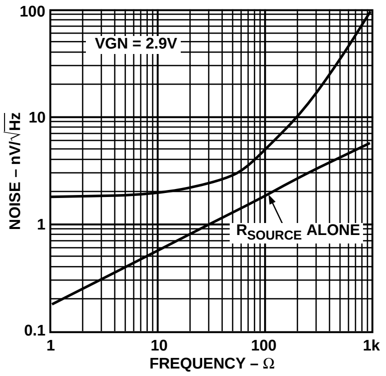


Figure 16. Input Referred Noise vs. R_{SOURCE}

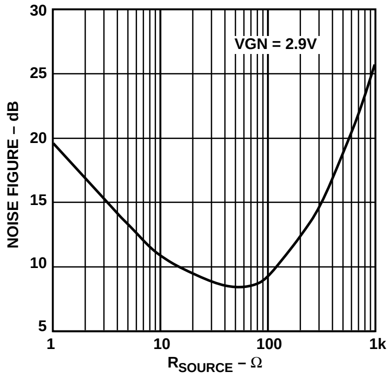


Figure 17. Noise Figure vs. R_{SOURCE}

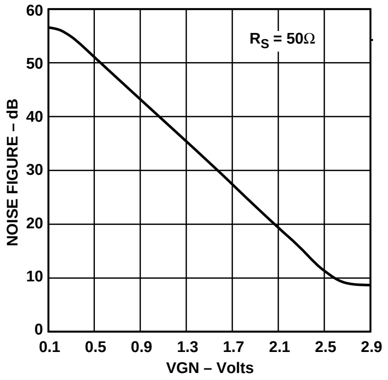


Figure 18. Noise Figure vs. VGN

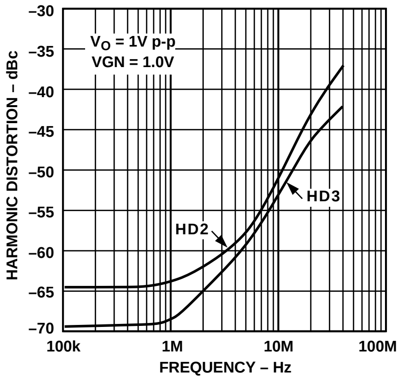


Figure 19. Harmonic Distortion vs. Frequency

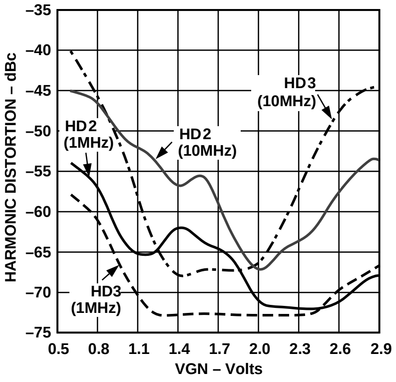


Figure 20. Harmonic Distortion vs. VGN

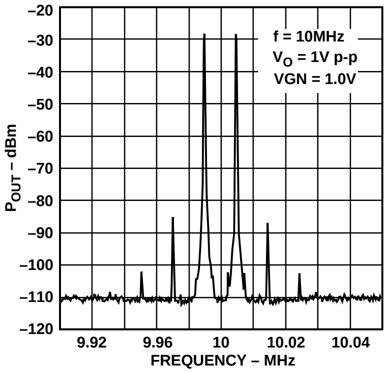


Figure 21. Intermodulation Distortion

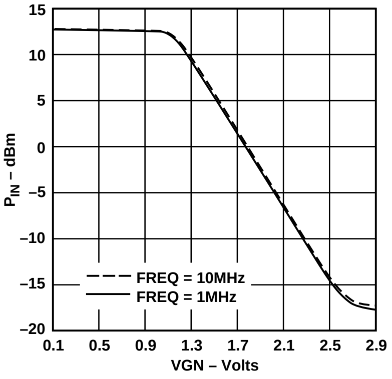


Figure 22. 1 dB Compression vs. VGN

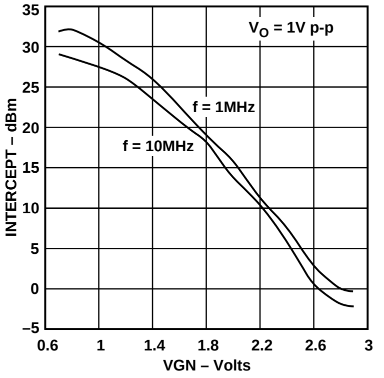


Figure 23. 3rd Order Intercept vs. VGN

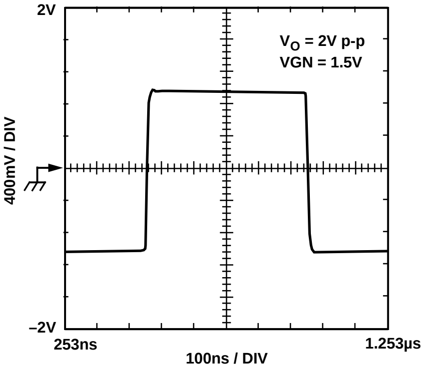


Figure 24. Large Signal Pulse Response

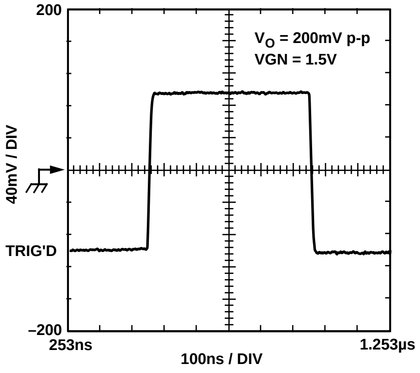


Figure 25. Small Signal Pulse Response

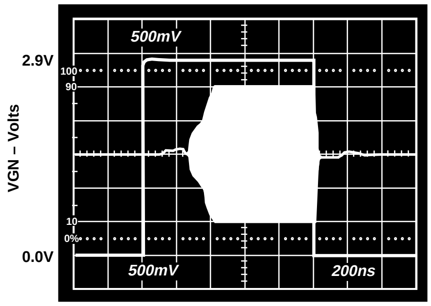


Figure 26. Power-Up/Down Response

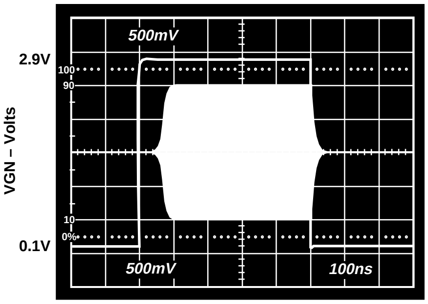


Figure 27. Gain Response

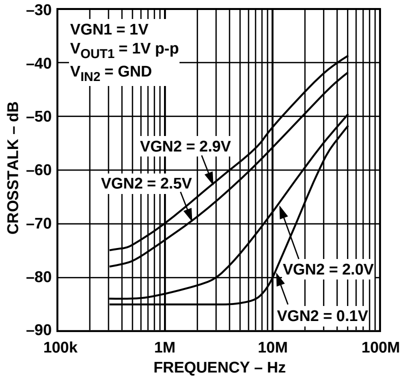


Figure 28. Crosstalk (CH1 to CH2) vs. Frequency

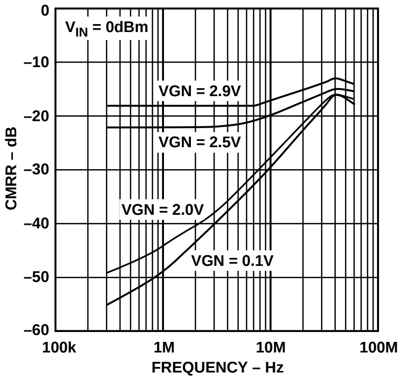


Figure 29. Common-Mode Rejection vs. Frequency

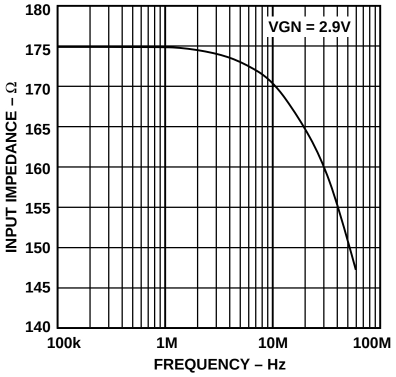


Figure 30. Input Impedance vs. Frequency

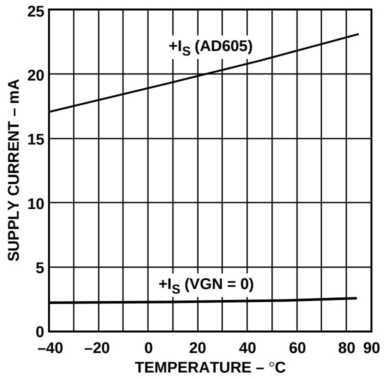


Figure 31. Supply Current (One Channel) vs. Temperature

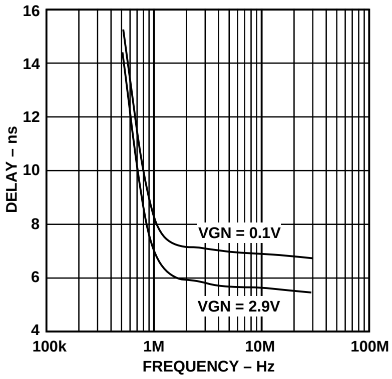


Figure 32. Group Delay vs. Frequency

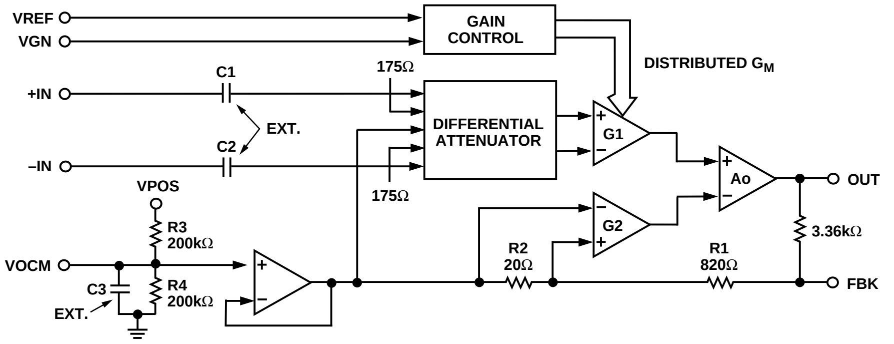


Figure 33. Simplified Block Diagram of a Single Channel of the AD605

THEORY OF OPERATION

The AD605 is a dual channel, low noise variable gain amplifier. Figure 33 shows the simplified block diagram of one channel. Each channel consists of a single-supply X-AMP (hereafter called DSX, Differential Single-supply X-AMP) made up of:

(a) a precision passive attenuator (differential ladder)

(b) a gain control block

(c) a VOCM buffer with supply splitting resistors R3 and R4

(d) an Active Feedback Amplifier[1] (AFA) with gain setting resistors R1 and R2.

The linear-in-dB gain response of the AD605 can generally be described by equation 1:

$$G\ (dB) = (Gain\ Scaling\ (dB/V)) \times (Gain\ Control\ (V)) - (19\ dB - (14\ dB) \times (FB)) \quad (1)$$

where $FB = 0$ if FBK-to-OUT are shorted,
$FB = 1$ if FBK-to-OUT is open.

Each channel provides between –14 dB to +34.4 dB through 0 dB to +48.4 dB of gain depending on the value of the resistance connected between pin FBK and OUT. The center 40 dB of gain is exactly linear-in-dB while the gain error increases at the top and bottom of the range. The gain is set by the gain control voltage (VGN). The VREF input establishes the gain scaling—the useful gain scaling range is between 20 dB/V and 40 dB/V for a VREF voltage of 2.5 V and 1.25 V respectively. For example, if FBK to OUT were shorted and VREF were set to 2.50 V (to establish a gain scaling of 20 dB/V), the gain equation would simplify to:

$$G\ (dB) = (20\ (dB/V)) \times (VGN\ (V)) - 19\ dB \quad (2)$$

The desired gain can then be achieved by setting the unipolar gain control (VGN) to a voltage within its nominal operating range of 0.25 V to 2.65 V (for 20 dB/V gain scaling). The gain is monotonic for a complete gain control range of 0.1 V to 2.9 V. Maximum gain can be achieved at a VGN of 2.9 V.

Since the two channels are identical, only Channel 1 will be used to describe their operation. VREF and VOCM are the only inputs that are shared by the two channels, and since they are normally ac grounds, crosstalk between the two channels is minimized. For highest gain scaling accuracy, VREF should have an external low impedance voltage source. For low accuracy 20 dB/V applications, the VREF input can be decoupled with a capacitor to ground. In this mode the gain scaling will be determined by the midpoint between +VCC and GND, so care should be taken to control the supply voltage to +5 V. The input resistance looking into the VREF pin is 10 kΩ ± 20%.

The AD605 is a single-supply circuit and the VOCM pin is used to establish the dc level of the midpoint of this portion of the circuit. VOCM needs only an external decoupling capacitor to ground to center the midpoint between the supply voltages (+5 V, GND); however if the dc level of the output is important to the user (see APPLICATIONS section for AD9050 example), then VOCM can be specifically set. The input resistance looking into the VOCM pin is 45 kΩ ± 20%.

Differential Ladder (Attenuator)

The attenuator before the fixed gain amplifier is realized by a differential seven-stage R–1.5R resistive ladder network with an untrimmed input resistance of 175 Ω single-ended or 350 Ω differentially. The signal applied at the input of the ladder network (Figure 34) is attenuated by 6.908 dB per tap; thus, the attenuation at the first tap is 6.908 dB, at the second, 13.816 dB, and so on all the way to the last tap where the attenuation is 48.356 dB. A unique circuit technique is used to interpolate continuously between the tap points, thereby providing continuous attenuation from 0 dB to –48.36 dB. One can think of the ladder network together with the interpolation mechanism as a voltage-controlled potentiometer.

Since the DSX is a single-supply circuit, some means of biasing its inputs must be provided. Node MID together with the VOCM buffer performs this function. Without internal biasing, external biasing would be required. If not done carefully, the biasing network can introduce additional noise and offsets. By providing internal biasing, the user is relieved of this task and only needs to ac couple the signal into the DSX. It should be made clear again that the input to the DSX is still fully differential if driven differentially, i.e., pins +IN and –IN see the same signal but with opposite polarity. What changes is the load as seen by the driver; it is 175 Ω when each input is driven single-ended, but 350 Ω when driven differentially. This can be easily explained when thinking of the ladder network as just two 175 Ω resistors connected back-to-back with the middle node, MID, being biased by the VOCM buffer. A differential signal applied between nodes +IN and –IN will result in zero current into node MID, but a single-ended signal applied to either input +IN or –IN while the other input is ac grounded will cause the current delivered by the source to flow into the VOCM buffer via node MID.

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[1] To understand the active-feedback amplifier topology, refer to the AD830 data sheet. The AD830 is a practical implementation of the idea.

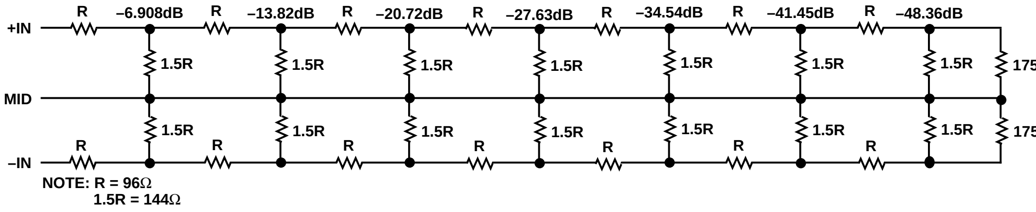


Figure 34. R–1.5R Dual Ladder Network

One feature of the X-AMP architecture is that the output referred noise is constant versus gain over most of the gain range. This can be easily explained by looking at Figure 34 and observing that the tap resistance is equal for all taps after only a few taps away from the inputs. The resistance seen looking into each tap is 54.4 Ω which makes 0.95 nV/$\sqrt{\text{Hz}}$ of Johnson noise spectral density. Since there are two attenuators, the overall noise contribution of the ladder network is $\sqrt{2}$ times 0.95 nV/$\sqrt{\text{Hz}}$ or 1.34 nV/$\sqrt{\text{Hz}}$, a large fraction of the total DSX noise. The rest of the DSX circuit components contribute another 1.20 nV/$\sqrt{\text{Hz}}$ which together with the attenuator produces 1.8 nV/$\sqrt{\text{Hz}}$ of total DSX input referred noise.

AC Coupling

As already mentioned, the DSX is a single single-supply circuit and therefore its inputs need to be ac coupled to accommodate ground-based signals. External capacitors C1 and C2 in Figure 33 level shift the input signal from ground to the dc value established by VOCM (nominal 2.5 V). C1 and C2, together with the 175 Ω looking into each of DSX inputs (+IN and –IN), will act as high-pass filters with corner frequencies depending on the values chosen for C1 and C2. For example, if C1 and C2 are 0.1 µF, then together with the 175 Ω input resistance seen into each side of the differential ladder of the DSX, a –3 dB high-pass corner at 9.1 kHz is formed.

If the DSX output needs to be ground referenced, then another ac coupling capacitor will be required for level shifting. This capacitor will also eliminate any dc offsets contributed by the DSX. With a nominal load of 500 Ω and a 0.1 µF coupling capacitor, this adds a high-pass filter with –3 dB corner frequency at about 3.2 kHz.

The choice for all 3 of these coupling capacitors depends on the application. They should allow the signals of interest to pass unattenuated, while at the same time they can be used to limit the low frequency noise in the system.

Gain Control Interface

The gain-control interface provides an input resistance of approximately 2 MΩ at pin VGN1 and gain scaling factors from 20 dB/V to 40 dB/V for VREF input voltages of 2.5 V to 1.25 V respectively. The gain varies linearly-in-dB for the center 40 dB of gain range, that is for VGN equal to 0.4 V to 2.4 V for the 20 dB/V scale, and 0.25 V to 1.25 V for the 40 dB/V scale. Figure 35 shows the ideal gain curves when the FBK to OUT connection is shorted which are described by the following equations:

$$G\,(20\ dB/V) = 20 \times VGN - 19,\ VREF = 2.500\ V \tag{3}$$

$$G\,(30\ dB/V) = 30 \times VGN - 19,\ VREF = 1.6666\ V \tag{4}$$

$$G\,(40\ dB/V) = 40 \times VGN - 19,\ VREF = 1.250\ V \tag{5}$$

From these equations one can see that all gain curves intercept at the same –19 dB point; this intercept will be 14 dB higher (–5 dB) if the FBK to OUT connection is left open. Outside of the central linear range, the gain starts to deviate from the ideal control law but still provides another 8.4 dB of range. For a given gain scaling one can calculate V_{REF} as shown in Equation (6).

$$V_{REF} = \frac{2.500\,V \times 20\ dB/V}{Gain\ Scale} \tag{6}$$

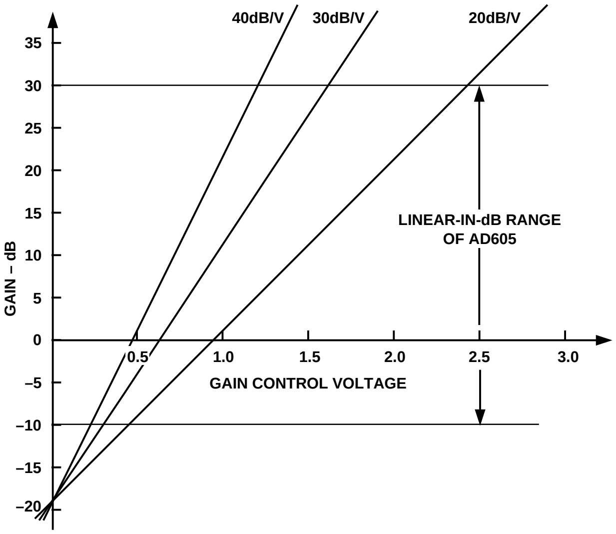


Figure 35. Ideal Gain Curves vs. V_{REF}

Usable gain control voltage ranges are 0.1 V to 2.9 V for 20 dB/V scale and 0.1 V to 1.45 V for the 40 dB/V scale. VGN voltages of less than 0.1 V are not used for gain-control since below 50 mV the channel is powered down. This can be used to conserve power and at the same time gate-off the signal. The supply current for a powered-down channel is 1.9 mA, the response time to power the device on-or-off, is less than 1 µs.

Active Feedback Amplifier (Fixed Gain Amp)

To achieve single supply operation and a fully differential input to the DSX, an active-feedback amplifier (AFA) was utilized. The AFA is basically an op amp with *two* g_m stages; one of the active stages is used in the feedback path (therefore the name), while the other is used as a differential input. Note that the differential input is an open-loop g_m stage which requires that it be highly linear over the expected input signal range. In this design, the g_m stage that senses the voltages on the attenuator is a distributed one, for example, there are as many g_m stages as there are taps on the ladder network. Only a few of them are on at any one time, depending on the gain-control voltage.

The AFA makes a differential input structure possible since one of its inputs (G1) is fully differential; this input is made up of a distributed gm stage. The second input (G2) is used for feedback. The output of G1 will be some function of the voltages sensed on the attenuator taps which is applied to a high-gain amplifier (A0). Because of negative feedback, the differential input to the high-gain amplifier has to be zero, this in turn implies that the differential input voltage to G2 times g_{m2} (the transconductance of G2) has to be equal to the differential input voltage to G1 times g_{m1} (the transconductance of G1). Therefore the overall gain function of the AFA is

$$\frac{V_{OUT}}{V_{ATTEN}} = \frac{gm1}{gm2} \times \frac{R1 \times R2}{R2} \qquad (7)$$

where V_{OUT} is the output voltage, V_{ATTEN} is the effective voltage sensed on the attenuator, (R1 + R2)/R2 = 42, and g_{m1}/g_{m2} = 1.25; the overall gain is thus 52.5 (34.4 dB).

The AFA has additional features: (1) inverting the output signal by switching the positive and negative input to the ladder network, (2) the possibility of using the –IN input as a second signal input, and (3) independent control of the DSX common-mode voltage. Under normal operating conditions it is best to just connect a decoupling capacitor to pin VOCM in which case the common-mode voltage of the DSX is half the supply voltage; this allows for maximum signal swing. Nevertheless, the common-mode voltage can be shifted up or down by directly applying a voltage to VOCM. It can also be used as another signal input, the only limitation being the rather low slew rate of the VOCM buffer.

If the dc level of the output signal is not critical, another coupling capacitor is normally used at the output of the DSX; again this is done for level shifting and to eliminate any dc offsets contributed by the DSX (see AC Coupling section).

The gain range of the DSX is programmable by a resistor connected between pins FBK and OUT. The possible ranges go from –14 dB to +34.4 dB when the pins are shorted together, to 0 dB to +48.4 dB when FBK is left open. Note that for the higher gain range, the bandwidth of the amplifier is reduced by a factor of five to about 8 MHz since the gain increased by 14 dB. This is the case for any constant gain-bandwidth-product amplifier of which the Active Feedback Amplifier is one.

APPLICATIONS

The most basic circuit in Figure 36 shows the connections for one channel of the AD605 with a gain range of –14 dB to +34.4 dB. The signal is applied at Pin 3. The ac coupling capacitors before pins –IN1 and +IN1 should be selected according to the required lower cutoff frequency. In this example the 0.1 µF capacitors together with the 175 Ω seen into each of the DSX input pins provides a –3 dB high pass corner of about 9.1 kHz. The upper cutoff frequency is determined by the amplifier and is 40 MHz.

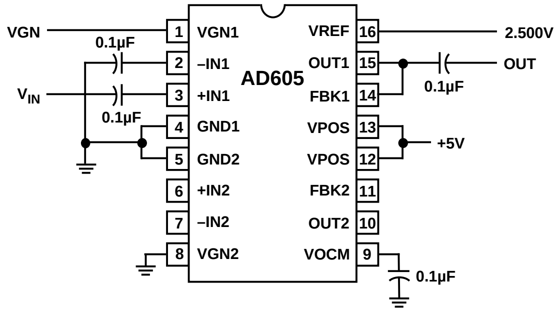


Figure 36. Basic Connections for a Single Channel

As shown here, the output is ac coupled for optimum performance. In the case of connecting to the 10-bit 40 MSPS A/D converter AD9050, ac coupling can be eliminated as long as pin VOCM is biased by the same 3.3 V common-mode voltage as the AD9050.

Pin VREF requires a voltage of 1.25 V to 2.5 V, with between 40 dB/V and 20 dB/V gain scaling respectively. Voltage VGN controls the gain; its nominal operating range is from 0.25 V to 2.65 V for 20 dB/V gain scaling, and 0.125 V to 1.325 V for 40 dB/V scaling. When this pin is taken to ground, the channel will power down and disable its output.

Connecting Two Amplifiers to Double the Gain Range
Figure 37 shows the two channels of the AD605 connected in series to provide a total gain range of 96.8 dB. When R1 and R2 are shorts, the gain range will be from –28 dB to +68.8 dB with a slightly reduced bandwidth of about 30 MHz. The reduction in bandwidth is due to two identical low-pass circuits being connected in series; in the case of two identical single-pole low-pass filters, the bandwidth would be reduced by exactly $\sqrt{2}$. If R1 and R2 are replaced by open circuits, i.e., Pins FBK1 and FBK2 are left unconnected, then the gain range will shift up by 28 dB to 0 dB to +96.8 dB. As already pointed out earlier, the bandwidth of each individual channel will be reduced by a factor of 5 to about 8 MHz since the gain increased by 14 dB. In addition, there is still the $\sqrt{2}$ reduction because of the series connection of the two channels which results in a final bandwidth of the higher gain version of about 6 MHz.

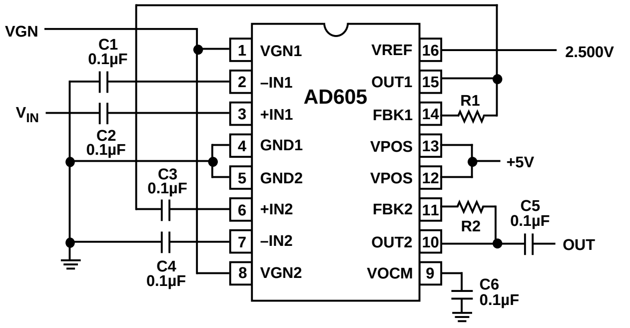


Figure 37. Doubling the Gain Range with Two Amplifiers

Two other easy combinations are possible to provide a gain range of –14 dB to 82.8 dB: (1) make R1 a short and R2 an open, or (2) make R1 an open and R2 a short. The bandwidth for both of these cases will be dominated by the channel that is set to the higher gain and will be about 8 MHz. From a noise standpoint, choice (2) is the better one since by increasing the gain of the first amplifier, the second amplifier's noise will have less of an impact on the total output noise. One further observation regarding noise is that by increasing the gain the output noise will increase proportionally; therefore, there is *no* increase in signal-to-noise ratio. It will actually stay fixed.

It should be noted that by selecting the appropriate values of R1 and R2, any gain range between –28 dB to +68.8 dB and 0 dB to +96.8 dB can be achieved with the circuit in Figure 37. When using any value other than shorts and opens for R1 and R2, the final value of the gain range will depend on external resistors matching on-chip resistors. Since the internal resistors can vary by as much as ±20%, the actual values for a particular gain have to be determined empirically. Note that the two channels within one part will match quite well; therefore, R1 will track R2 in Figure 37.

C3 is not required since the common-mode voltage at Pin OUT1 should be identical to the one at Pins +IN2 and –IN2, but since only 1 mV of offset at the output of the first DSX will introduce an offset of 53 mV when the second DSX is set to the maximum gain of the lowest gain range (+34.4 dB), and 263 mV when set to the maximum gain of the highest gain range (+48.4 dB), it is important to include ac coupling to get the maximum dynamic range at the output of the cascaded amplifiers. C5 is necessary if the output signal needs to be referenced to any common-mode level other than half of the supply as is provided by Pin OUT2.

Figure 38 shows the gain verses VGN for the circuit in Figure 37 at 1 MHz and the lowest gain range (–14 dB to +34.4 dB). Note that the gain scaling is 40 dB/V, double the 20 dB/V of an individual DSX; this is the result of the parallel connection of the gain control inputs, VGN1 and VGN2. One could of course also sequentially increase the gain by first increasing the gain of Channel 1 and then Channel 2. In that case VGN1 and VGN2 will have to be driven from separate voltage sources, for instance two separate DACs. Figure 39 shows the gain error of Figure 38.

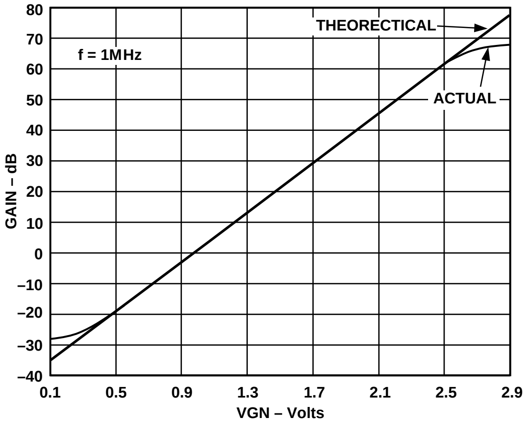


Figure 38. Gain vs. VGN for the Circuit in Figure 37

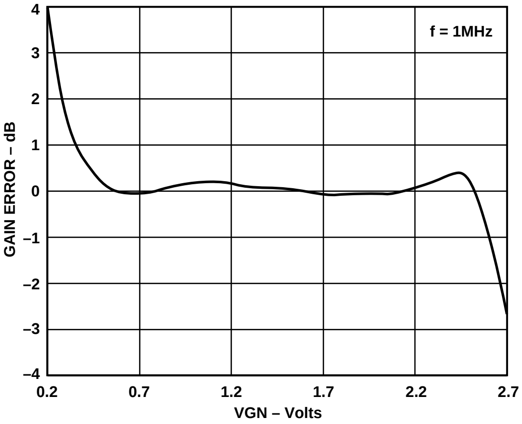
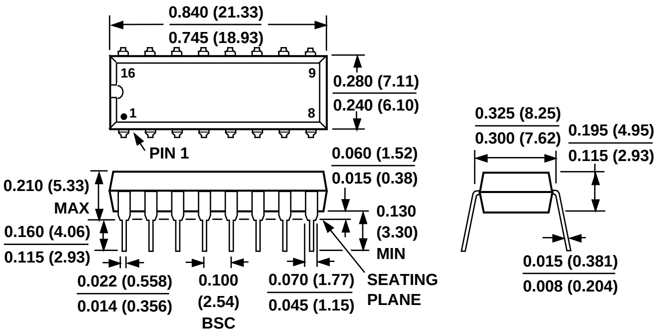


Figure 39. Gain Error vs. VGN for the Circuit in Figure 37

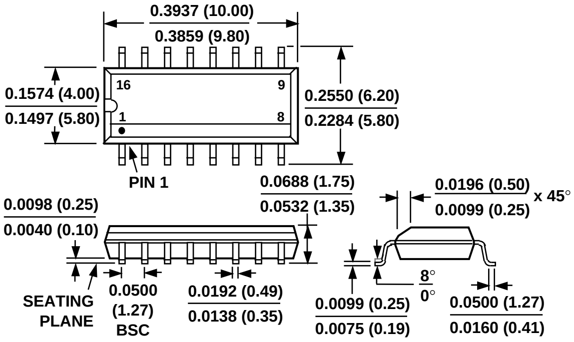
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Pin Plastic DIP
N-16



16-Pin Small Outline IC
R-16



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