

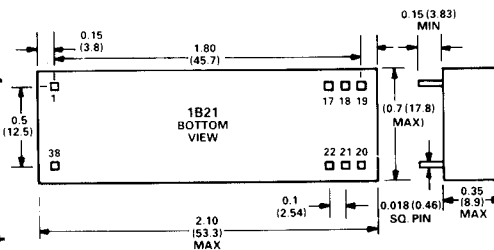


# 1B21 — SPECIFICATIONS (typical at +25°C and $V_S = \pm 15V$ unless otherwise noted)

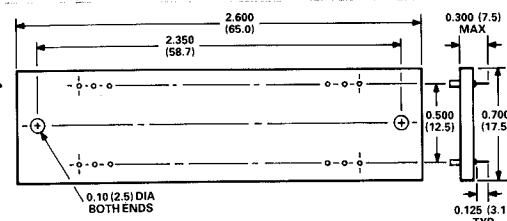
Model	1B21AN
<b>INPUT SPECIFICATIONS</b>	
Input Range	0 to +10V
Full-Scale Input	+1V min to +10V max
Input Bias Current	$\pm 30\text{pA}$ ( $\pm 400\text{pA}$ max)
<b>OUTPUT SPECIFICATIONS</b>	
Current Output Range	4mA to 20mA, 0 to 20mA
Load Compliance at $V_{\text{LOOP}} = 30V$	27V min
Max Output Current @ Input Overload	25mA
Output Noise, 100Hz Bandwidth	1 $\mu\text{A}$ p-p
NONLINEARITY (% of Span)	$\pm 0.02\%$ ( $\pm 0.05\%$ max)
<b>ISOLATION</b>	
CMV, Input to Output Continuous	1500V rms
CMR, @ 60Hz	90dB min
Transient Protection	IEEE-STD 472 (SWC)
<b>ACCURACY</b>	
Warm-Up Time to Rated Performance	5 min
Total Output Error @ +25°C (Untrimmed)	
Offset ( $V_{\text{IN}} = 0V$ ) <sup>1</sup>	$\pm 100\mu\text{A}$
Span ( $V_{\text{IN}} = +10V$ )	$\pm 0.6\%$ FSR
vs. Temperature (-25°C to +85°C)	
Offset <sup>2</sup>	$\pm 300\text{nA}/^\circ\text{C}$
Span	$\pm 50\text{ppm}/^\circ\text{C}$
<b>REFERENCE OUTPUT</b>	
Voltage	+6.4V dc
Output Error	$\pm 1.5\%$ max
Temperature Coefficient	$\pm 20\text{ppm}/^\circ\text{C}$ max
<b>DYNAMIC RESPONSE</b>	
Settling Time to 0.1% of F.S. for 10V Step	9ms
Small Signal Bandwidth	100Hz
<b>POWER SUPPLY</b>	
Input Side	
Operating Voltage	$\pm 15V \pm 5\%$
Quiescent Current	
+15V Supply	10mA
-15V Supply	5mA
Power Supply Rejection	$\pm 0.01\%/V$
Loop Side	
Operating Voltage	+15V to +30V
Maximum Current	25mA
<b>ENVIRONMENTAL</b>	
Temperature Range	
Rated Performance	-25°C to +85°C
Operating	-40°C to +85°C
Storage	-40°C to +85°C
Relative Humidity, Noncondensing	0 to 95% @ +60°C
CASE SIZE	0.7" × 2.1" × 0.35" (17.8 × 53.3 × 8.9)mm

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



## AC1060 MATING SOCKET



## PIN DESIGNATIONS

PIN	FUNCTION
1	OUT HI
17	IN
18	FB
19	REF
20	+15V
21	COM
22	-15V
38	OUT LOW

## NOTES

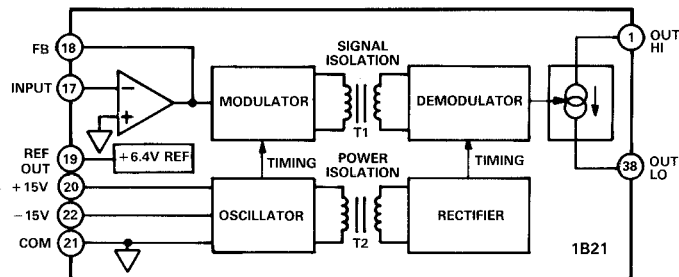
<sup>1</sup>For 0-20mA mode. For 4-20mA mode an additional 60 $\mu\text{A}$  is contributed by the  $\pm 1.5\%$  reference error on the 4mA output.

<sup>2</sup>For a complete discussion of the temperature effects of the offset resistor and reference refer to "Using the 1B21" section.

Specifications subject to change without notice.

**INSIDE THE 1B21**

Referring to the functional block diagram, the ±15V power inputs provide power to both the input side circuitry and the power oscillator. The 25kHz power oscillator provides both the timing information for the signal modulator and drives transformer T2 for the output side power supplies. The secondary winding of T2 is full wave rectified and filtered to create the output side power.



1B21 Functional Block Diagram

The input stage is configured as an inverting amplifier with three user supplied resistors for gain, offset and feedback. The conditioned signal is modulated to generate a square wave with a peak-to-peak amplitude proportional to  $V_{IN}$ . This signal drives the signal transformer T1. An internal reference with a nominal output voltage of +6.4V and tempco of ±20ppm/°C is provided to develop a 4mA offset for 4mA to 20mA current loop applications.

After passing through signal transformer T1, the amplitude modulated signal is demodulated and filtered by a single pole filter. Timing information for the output side is derived from the power transformer T2. The filtered output provides the control signal for the voltage-to-current converter stage. An external power supply is required in series with the load to complete the current loop.

**USING THE 1B21**

**Input Configurations:** The 1B21 has been designed with a flexible input stage for a variety of input and output ranges. The basic interconnection for setting gain and offset is shown in Figure 1. The output of the internal amplifier is constrained to 0 to -5V, which maps into 0 to 20mA across the isolation barrier. Thus to create a 4mA offset at the output, the input amplifier has to be offset by 1V.

For example, for 0 to 20mA operation the transfer function for the input stage is:

$$5/V_{IN} = R_F/R_I$$

and no offset resistor is needed. For 4mA to 20mA operation we get:

$$4/V_{IN} = R_F/R_I$$

which maps the input voltage into a 4V span. To create a 1V offset at the output of the internal amplifier (4mA at the output of the 1B21) a current derived from the reference can be fed into the summing node. The offset resistor (for a 1V output offset) will be given by the equation:  $R_O = 6.4R_F$ . For most applications it is recommended that  $R_F$  be in the  $25k\Omega \pm 20\%$  range. Resistor values for typical input and output ranges are shown in Table I.

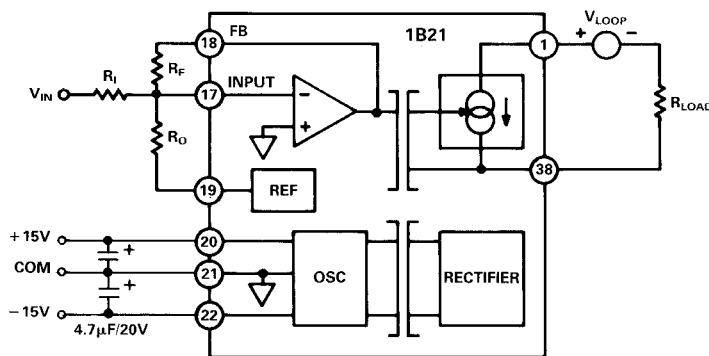


Figure 1. Basic Interconnections

Input Volts	Output mA	$R_I$ kΩ	$R_F$ kΩ	$R_O$ kΩ
0-5	0-20	25	25	Open
0-10	0-20	50	25	Open
0-5	4-20	25	20	128
0-10	4-20	50	20	128
1-5	4-20	25	25	Open

Table I. Resistor Values for Typical Ranges

**Adjustments:** Figure 2 is an example of using potentiometers for trimming gain and offset for a 0-5V input and 0 to 20mA output. The network for offset adjustment keeps the resistors relatively small to minimize noise effects while giving a sensitivity of ±1% of span. For more adjustment range, resistors smaller than 274k can be used. Resistor values from Table I can be substituted for other input and output ranges.

In general, any bipolar voltage can be input to the 1B21 as long as it is offset to meet the 0 to -5V constraint of the modulator and the input signal range is 1V minimum.

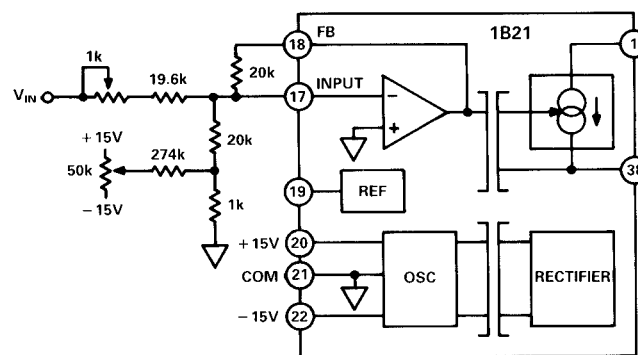


Figure 2. Offset and Span Adjustment

# 1B21

**TC Considerations of External Resistors:** The specifications for gain and offset temperature coefficient (TC) for the 1B21 exclude the effects of external components. The total gain TC for the circuit in Figure 1 is:

$$\text{Gain TC} = 1B21 \text{ Gain TC} + (\text{Tracking TC of } R_F \text{ and } R_I)$$

The offset TC is also affected by the thermal stability of the internal voltage reference and its contribution is:

$$\text{Ref TC} = (V_{REF})(R_F/R_O)(4\text{mA}/V)(\text{TC of } V_{REF} + \text{Tracking TC of } R_F \text{ and } R_O)/1 \times 10^6$$

$$\text{Total Offset TC} = 1B21 \text{ Offset TC} + \text{Ref TC}$$

Specifically using  $R_F$ ,  $R_I$  and  $R_O$  from Case 3 in Table I, with absolute TCs of  $\pm 25\text{ppm}/^\circ\text{C}$  we get:

$$\text{Gain TC} = 50 + (25 + 25) = 100\text{ppm}/^\circ\text{C}$$

$$\begin{aligned} \text{Offset TC} &= 300 + (6.4\text{V})(20\text{k}/128\text{k})(4\text{mA}/V)(20 + 25 + 25)/ \\ &= \pm 580\text{nA}/^\circ\text{C} \end{aligned}$$

Similarly, when using a resistor network with a tracking spec of  $\pm 5\text{ppm}/^\circ\text{C}$ , the total gain TC would be  $\pm 55\text{ppm}/^\circ\text{C}$  and the total offset TC would be  $\pm 400\text{nA}/^\circ\text{C}$ .

## APPLICATIONS

**Output Protection:** In many industrial applications it may be necessary to protect the current output from accidental shorts to ac line voltages in addition to high common-mode voltages and short circuits to ground. The circuit shown in Figure 3 can be used for this purpose. The maximum permissible load resistance will be lowered by the fuse resistance (typically  $8\Omega$ ) when protection circuitry is utilized.

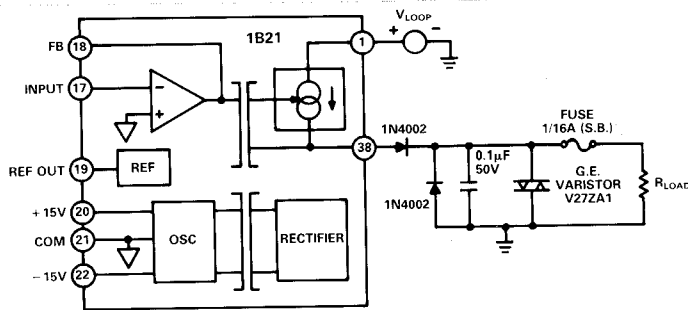


Figure 3. Output Protection Circuitry

**Low Drift Input Network:** Figure 4 shows a configuration suitable for applications where errors have to be minimized over a wide temperature range. A temperature tracking network such as a 50k Beckman (PN 698-3R50KD) can be used to implement both offset and gain for either 0 to 20mA or 4mA to 20mA current loops. For 0-10V signals either IN1 or IN2 can be used for input. For 0-5V signals, jumper IN1 to IN2. Similarly, for 4mA to 20mA operation the 4mA node should be jumpered to OFFSET, while for 0 to 20mA it should be tied to COM.

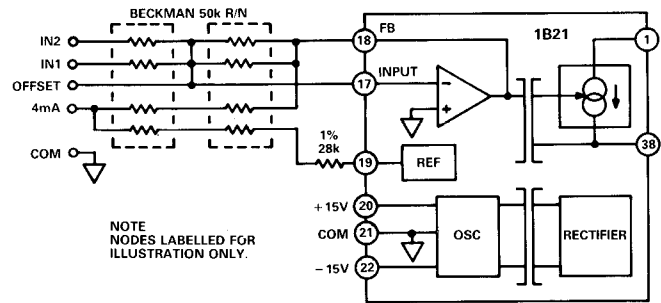


Figure 4. Low Tempco Resistor Network Configuration

**Multiloop Isolation:** Multiple 1B21s can be connected to a single loop supply in parallel as shown in Figure 5. The amperage of the loop supply should be sufficient to drive all the loops at full-scale output.

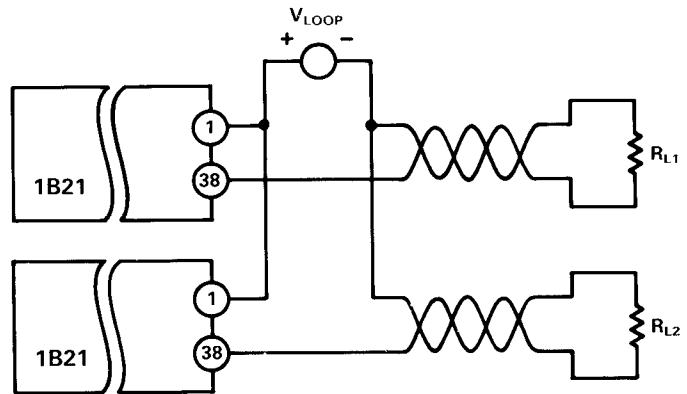


Figure 5. Multiple 1B21s with Single Loop Supply