Micropower, Rail-to-Rail Input and Output Operational Amplifiers

OP196/OP296/OP496

FEATURES
Rail-to-Rail Input and Output Swing
Low Power: 60 μA/Amplifier
Gain Bandwidth Product: 450 kHz
Single-Supply Operation: +3 V to +12 V
Low Offset Voltage: 300 μV max
High Open-Loop Gain: 500 V/mV
Unity-Gain Stable
No Phase Reversal

APPLICATIONS
Battery Monitoring
Sensor Conditioners
Portable Power Supply Control
Portable Instrumentation

GENERAL DESCRIPTION

The OP196 family of CBCMOS operational amplifiers features micropower operation and rail-to-rail input and output ranges.

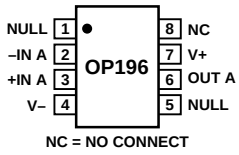
The extremely low power requirements and guaranteed operation from +3 V to +12 V make these amplifiers perfectly suited to monitor battery usage and to control battery charging. Their dynamic performance, including 26 nV/$\sqrt{\text{Hz}}$ voltage noise density, recommends them for battery-powered audio applications. Capacitive loads to 200 pF are handled without oscillation.

The OP196/OP296/OP496 are specified over the HOT extended industrial (–40°C to +125°C) temperature range. +3 V operation is specified over the 0°C to +125°C temperature range.

The single OP196 and the dual OP296 are available in 8-pin plastic DIP and SO-8 surface mount packages. The quad OP496 is available in 14-pin plastic DIP and narrow SO-14 surface mount packages. Check factory for availability of the OP296 and OP496 in TSSOP packages.

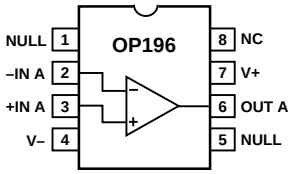
PIN CONFIGURATIONS

8-Lead Narrow-Body SO (S Suffix)



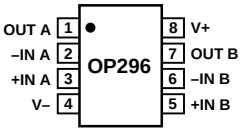
NC = NO CONNECT

8-Lead Epoxy DIP (P Suffix)

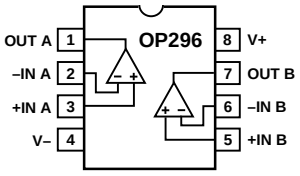


NC = NO CONNECT

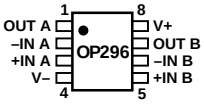
8-Lead Narrow-Body SO (S Suffix)



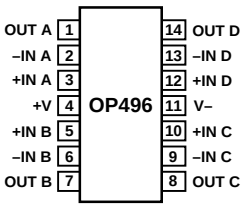
8-Lead Epoxy DIP (P Suffix)



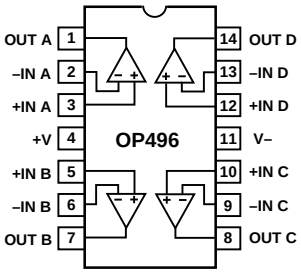
8-Lead TSSOP (RU Suffix)



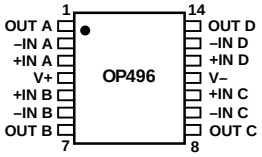
14-Lead Narrow-Body SO (S Suffix)



14-Lead Epoxy DIP (P Suffix)



14-Lead TSSOP (RU Suffix)



REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

OP196/OP296/OP496–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP196G, OP296G, OP496G		35	300	µV
		–40°C ≤ T_A ≤ +125°C			650	µV
		OP296H, OP496H			800	µV
		–40°C ≤ T_A ≤ +125°C			1.2	mV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +125°C		±10	±35	nA
Input Offset Current	I_{OS}			±1.5	±5	nA
		–40°C ≤ T_A ≤ +125°C			±15	nA
Input Voltage Range	V_{CM}		0		+5.0	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5.0 V,				
		–40°C ≤ T_A ≤ +125°C	65			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ,				
		0.30 V ≤ V_{OUT} ≤ 4.7 V,				
		–40°C ≤ T_A ≤ +125°C	150	200		V/mV
Long-Term Offset Voltage	V_{OS}	G Grade, Note 1			550	µV
		H Grade, Note 1			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	G Grade, Note 2		1.5		µV/°C
		H Grade, Note 2		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA	4.85	4.92		V
		I_L = 1 mA	4.30	4.56		V
		I_L = 2 mA		4.1		V
Output Voltage Swing Low	V_{OL}	I_L = –100 µA		36	70	mV
		I_L = –1 mA		350	450	mV
		I_L = –2 mA		750		mV
Output Current	I_{OUT}			±4		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	±2.5 V ≤ V_S ≤ ±6 V,				
		–40°C ≤ T_A ≤ +125°C	85			dB
Supply Current per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞			60	µA
		–40°C ≤ T_A ≤ +125°C		45	80	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =100 kΩ		0.3		V/µs
Gain Bandwidth Product	GBP			350		kHz
Phase Margin	$ø_m$			47		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		26		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.19		pA/√Hz

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +3.0 V, V_{CM} = +1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP196G, OP296G, OP496G		35	300	µV
		$0°C \le T_A \le +125°C$			650	µV
		OP296H, OP496H			800	µV
		$0° \le T_A \le +125°C$			1.2	mV
Input Bias Current	I_B			±10	±35	nA
Input Offset Current	I_{OS}			±1	±5	nA
Input Voltage Range	V_{CM}		0		+3.0	V
Common-Mode Rejection Ratio	CMRR	$0 V \le V_{CM} \le 3.0 V$,				
		$0°C \le T_A \le +125°C$	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ	80	200		V/mV
Long-Term Offset Voltage	V_{OS}	G Grade, Note 1			550	µV
		H Grade, Note 1			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	G Grade, Note 2		1.5		µV/°C
		H Grade, Note 2		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA	2.85			V
Output Voltage Swing Low	V_{OL}	I_L = –100 µA			70	mV
POWER SUPPLY						
Supply Current per Amplifier	I_{SY}	V_{OUT} = 1.5 V, R_L = ∞		40	60	µA
		$0°C \le T_A \le +125°C$			80	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =100 kΩ		0.25		V/µs
Gain Bandwidth Product	GBP			350		kHz
Phase Margin	$ø_m$			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		26		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.19		$pA/\sqrt{Hz}$

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the 0°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS (@ V_S = +12.0 V, V_{CM} = +6 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP196G, OP296G, OP496G		35	300	µV
		0°C ≤ T_A ≤ +125°C			650	µV
		OP296H, OP496H			800	µV
		0° ≤ T_A ≤ +125°C			1.2	mV
Input Bias Current	I_B	–40°C ≤ T_A ≤ +125°C		±10	±35	nA
Input Offset Current	I_{OS}			±1	±5	nA
		–40°C ≤ T_A ≤ +125°C			±15	nA
Input Voltage Range	V_{CM}		0		+12	V
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ +12 V,				
		–40°C ≤ T_A ≤ +125°C	65			dB
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ	300	1000		V/mV
Long-Term Offset Voltage	V_{OS}	G Grade, Note 1			550	µV
		H Grade, Note 1			1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	G Grade, Note 2		1.5		µV/°C
		H Grade, Note 2		2		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 100 µA	11.85			V
		I_L = 1 mA	11.30			V
Output Voltage Swing Low	V_{OL}	I_L = –100 µA			70	mV
		I_L = –1 mA			450	mV
Output Current	I_{OUT}			±4		mA
POWER SUPPLY						
Supply Current per Amplifier	I_{SY}	V_{OUT} = 6 V, R_L = ∞			60	µA
		–40°C ≤ T_A ≤ +125°C			80	µA
Supply Voltage Range	V_S		+3		+12	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =100 kΩ		0.3		V/µs
Gain Bandwidth Product	GBP			450		kHz
Phase Margin	$ø_m$			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.8		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		26		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.19		pA/√Hz

NOTES
[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.
[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}		300	µV max
Input Bias Current	I_B		±35	nA max
Input Offset Current	I_{OS}		±5	nA max
Input Voltage Range[1]	V_{CM}		0 to +5	V min
Common-Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 5 V	60	dB min
Power Supply Rejection Ratio	PSRR	±1.5 V ≤ V_S ≤ ±6 V	80	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 100 kΩ	100	V/mV min
Output Voltage Swing High	V_{OH}	I_L = 100 µA	4.85	V min
Output Voltage Swing Low	V_{OL}	I_L = –100 µA	70	mV max
Supply Current per Amplifier	I_{SY}	V_{OUT} = 2.5 V, R_L = ∞	60	µA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMRR test.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +15 V
Input Voltage[2] . . . . . +15 V
Differential Input Voltage[2] . . . . . +15 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
OP196G, OP296G, OP496G, H . . . . . –40°C to +125°C
Junction Temperature Range
P, S, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

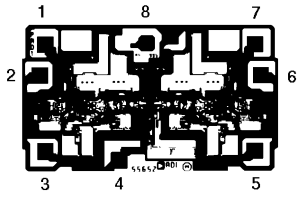
Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
8-Pin TSSOP(RU)	240	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
14-Pin TSSOP (RU)	180	35	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP package; θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

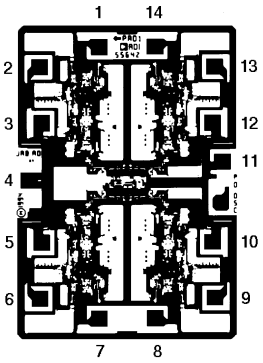
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP196GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP196GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP296GP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP296GS	–40°C to +125°C	8-Pin SOIC	SO-8
OP296HRU	–40°C to +125°C	8-Pin TSSOP	RU-8
OP296GBC	+25°C	DICE	
OP496GP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP496GS	–40°C to +125°C	14-Pin SOIC	SO-14
OP496HRU	–40°C to +125°C	14-Pin TSSOP	RU-14
OP496GBC	+25°C	DICE	

DICE CHARACTERISTICS



OP296 Die Size 0.072 × 0048 inch, 3,456 sq. mils Substrate (Die Backside) Is Connected to V+. Transistor Count, 110.



OP496 Die Size 0.062 × 0.092 inch, 5,704 sq. mils Substrate (Die Backside) Is Connected to V+. Transistor Count, 214.

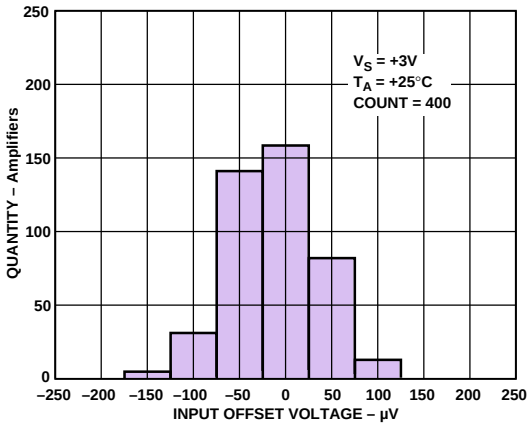


Figure 1. Input Offset Voltage Distribution

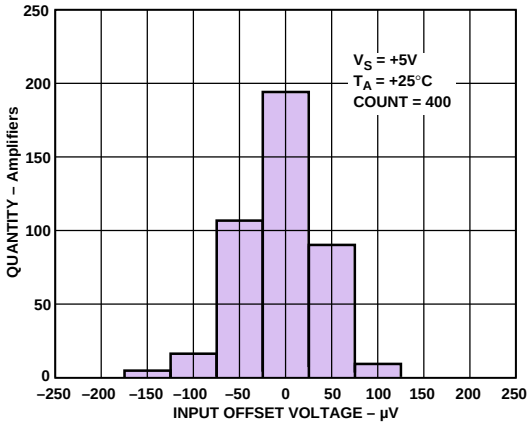


Figure 2. Input Offset Voltage Distribution

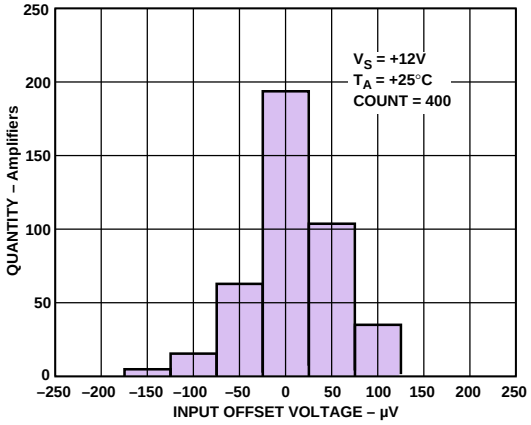


Figure 3. Input Offset Voltage Distribution

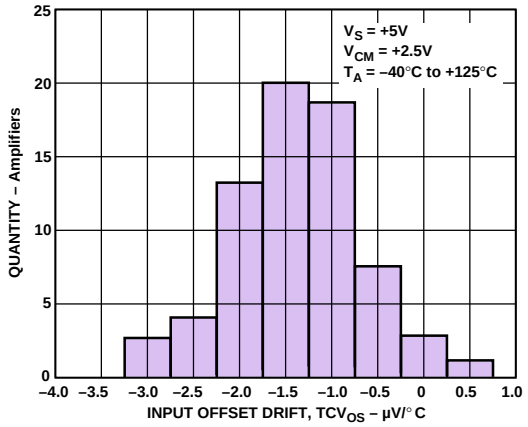


Figure 4. Input Offset Voltage Distribution (TCV_{OS})

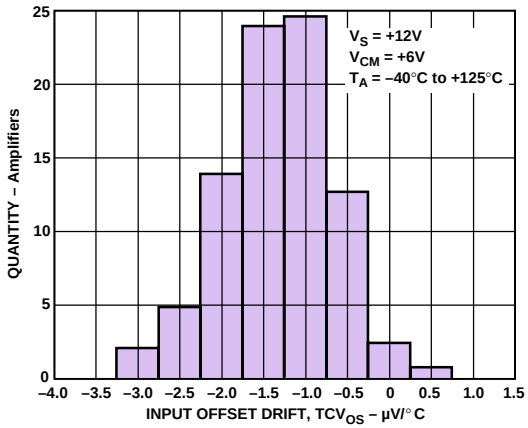


Figure 5. Input Offset Voltage Distribution (TCV_{OS})

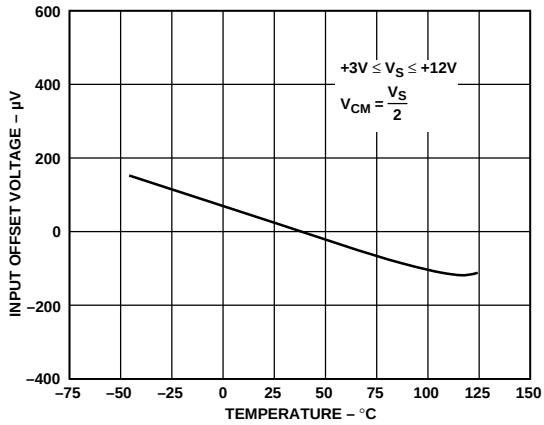


Figure 6. Input Offset Voltage vs. Temperature

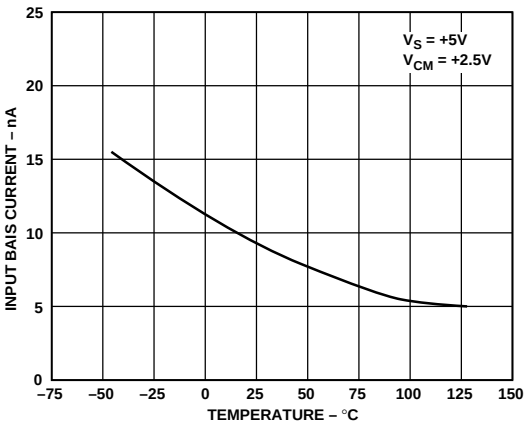


Figure 7. Input Bias Current vs. Temperature

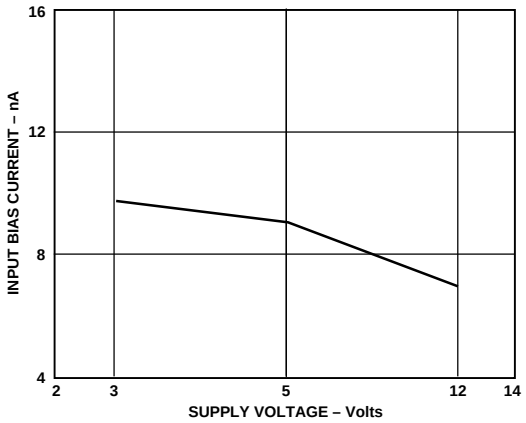


Figure 8. Input Bias Current vs. Supply Voltage

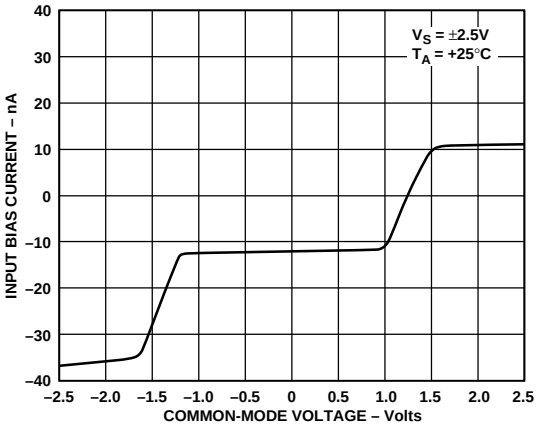


Figure 9. Input Bias Current vs. Common-Mode Voltage

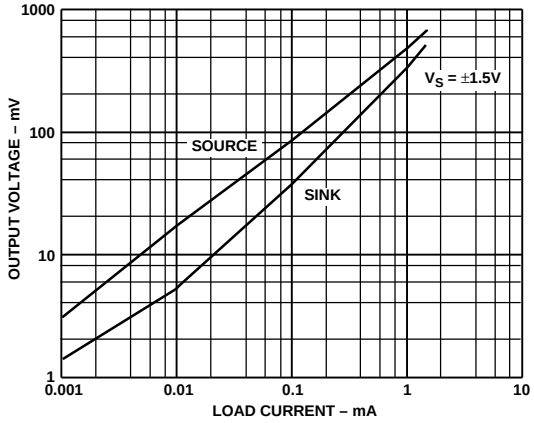


Figure 10. Output Voltage to Supply Rail vs. Load Current

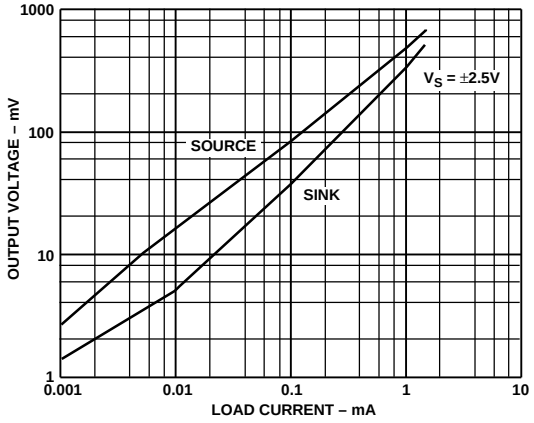


Figure 11. Output Voltage to Supply Rail vs. Load Current

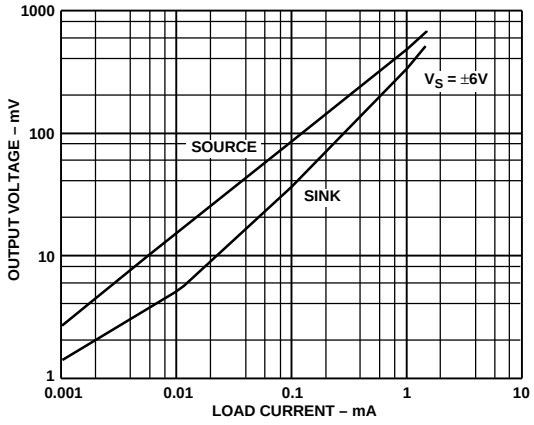


Figure 12. Output Voltage to Supply Rail vs. Load Current

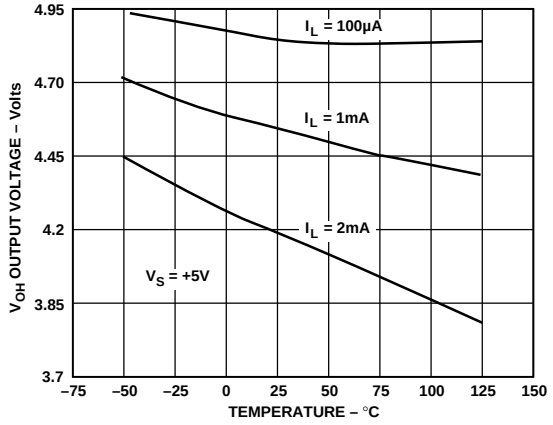


Figure 13. Output Voltage Swing vs. Temperature

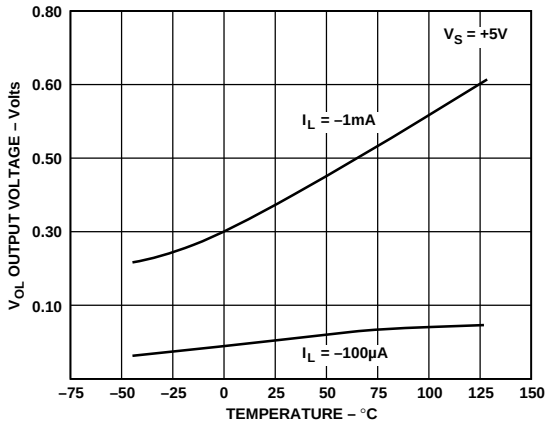


Figure 14. Output Voltage Swing vs. Temperature

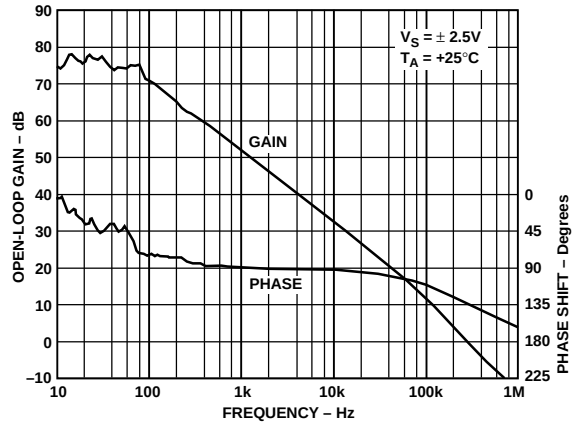


Figure 15. Open-Loop Gain and Phase vs. Frequency (No Load)

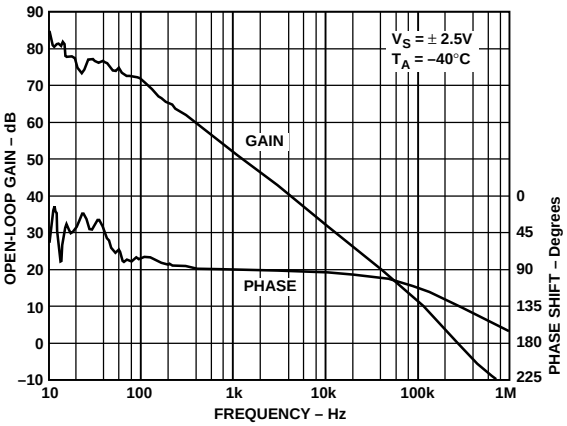


Figure 16. Open-Loop Gain and Phase vs. Frequency (No Load)

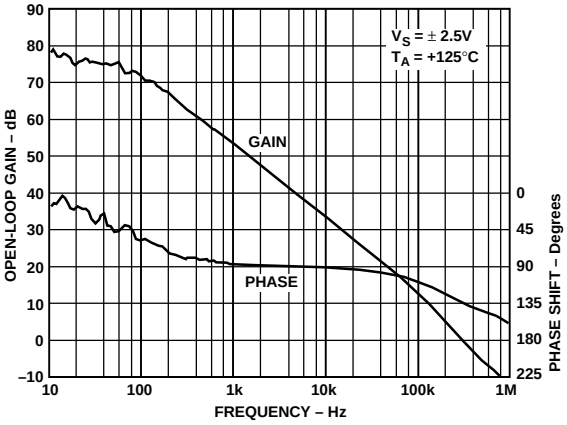


Figure 17. Open-Loop Gain and Phase vs. Frequency (No Load)

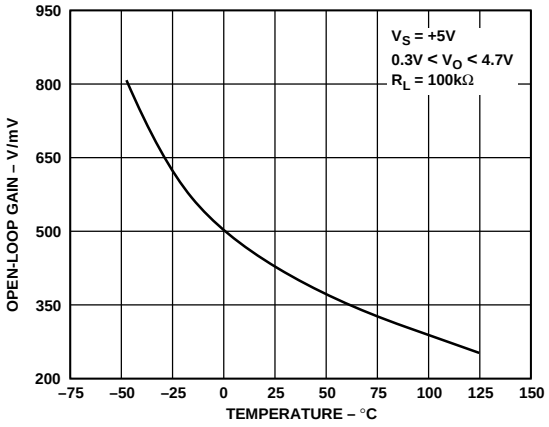


Figure 18. Open-Loop Gain vs. Temperature

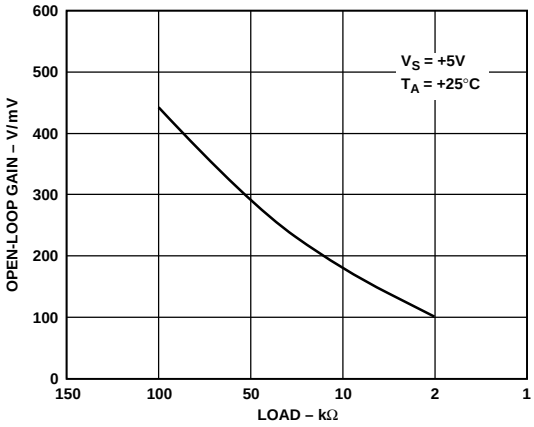


Figure 19. Open Loop Gain vs. Resistive Load

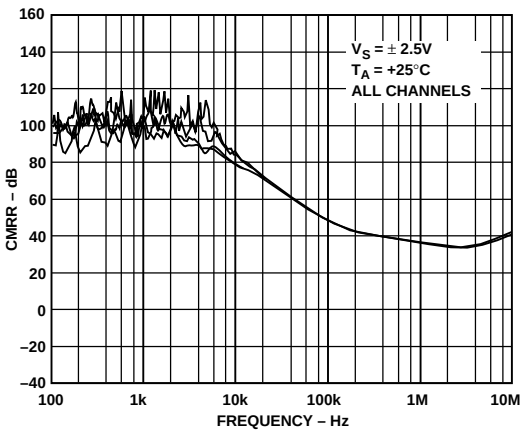


Figure 22. CMRR vs. Frequency

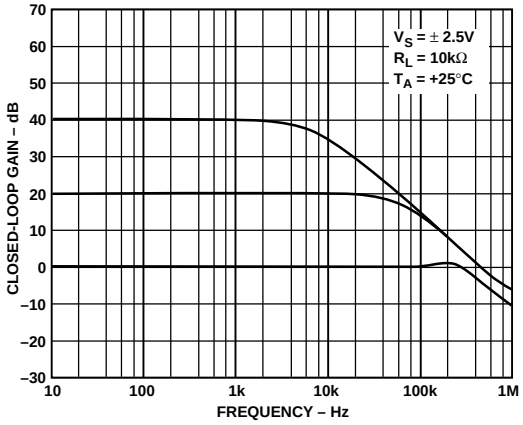


Figure 20. Closed-Loop Gain vs. Frequency

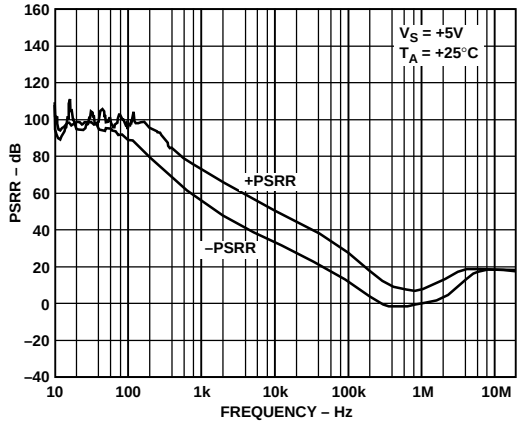


Figure 23. PSRR vs. Frequency

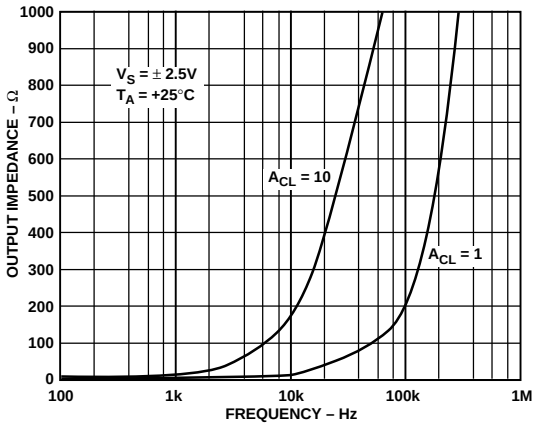


Figure 21. Output Impedance vs. Frequency

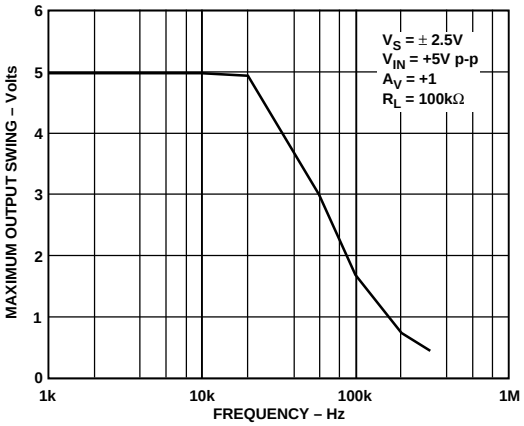


Figure 24. Maximum Output Swing vs. Frequency

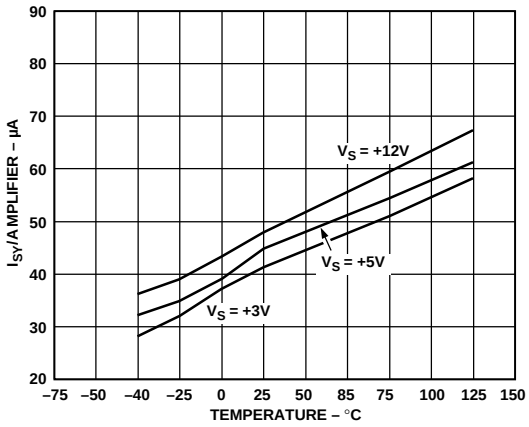


Figure 25. Supply Current/Amplifier vs. Temperature

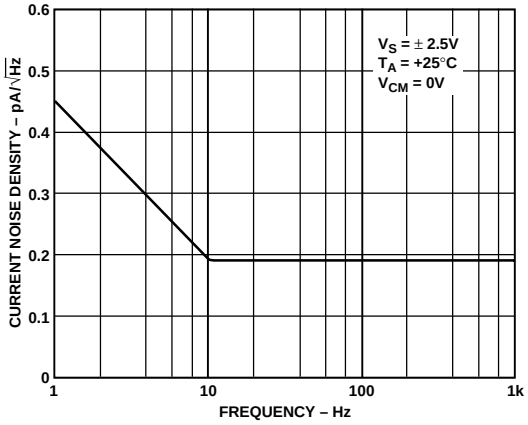


Figure 28. Input Bias Current Noise Density vs. Frequency

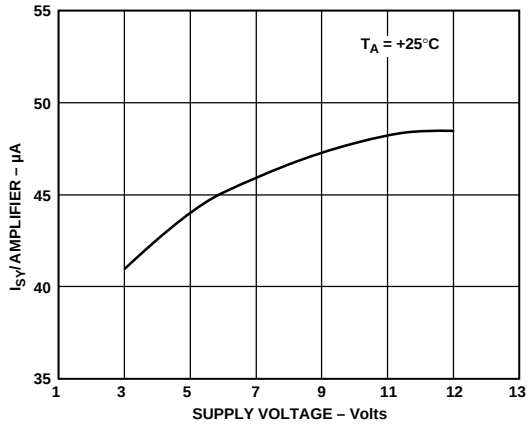


Figure 26. Supply Current/Amplifier vs. Supply Voltage

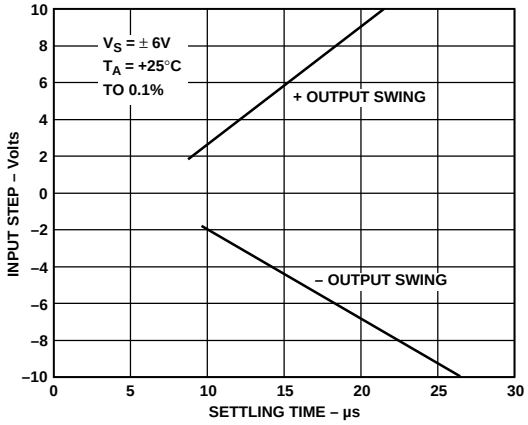


Figure 29. Settling Time to 0.1% vs. Step Size

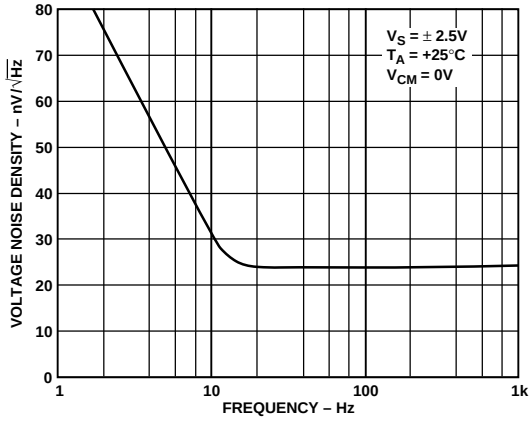


Figure 27. Voltage Noise Density vs. Frequency

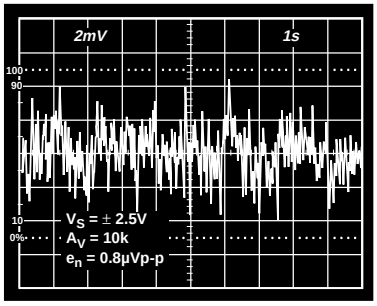


Figure 30. 0.1 Hz to 10 Hz Noise

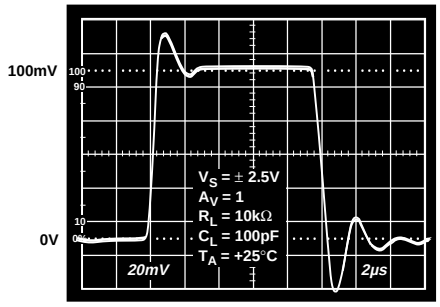


Figure 31. Small Signal Transient Response

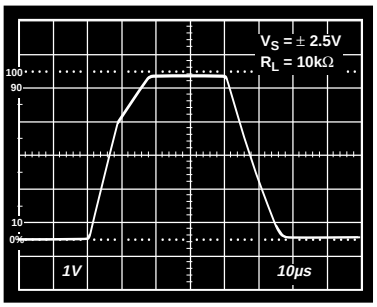


Figure 33. Large Signal Transient Response

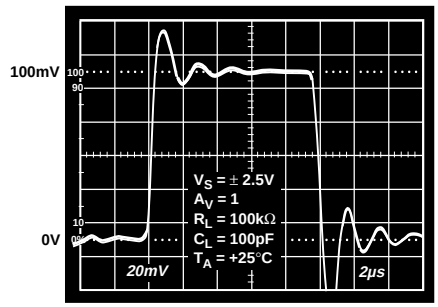


Figure 32. Small Signal Transient Response

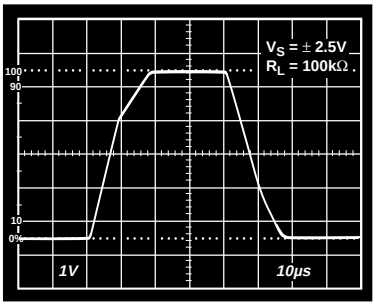


Figure 34. Large Signal Transient Response

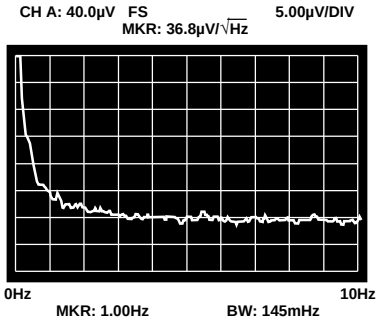


Figure 35. 1/f Noise Corner, $V_S = \pm 15$ V, $A_V = 1{,}000$

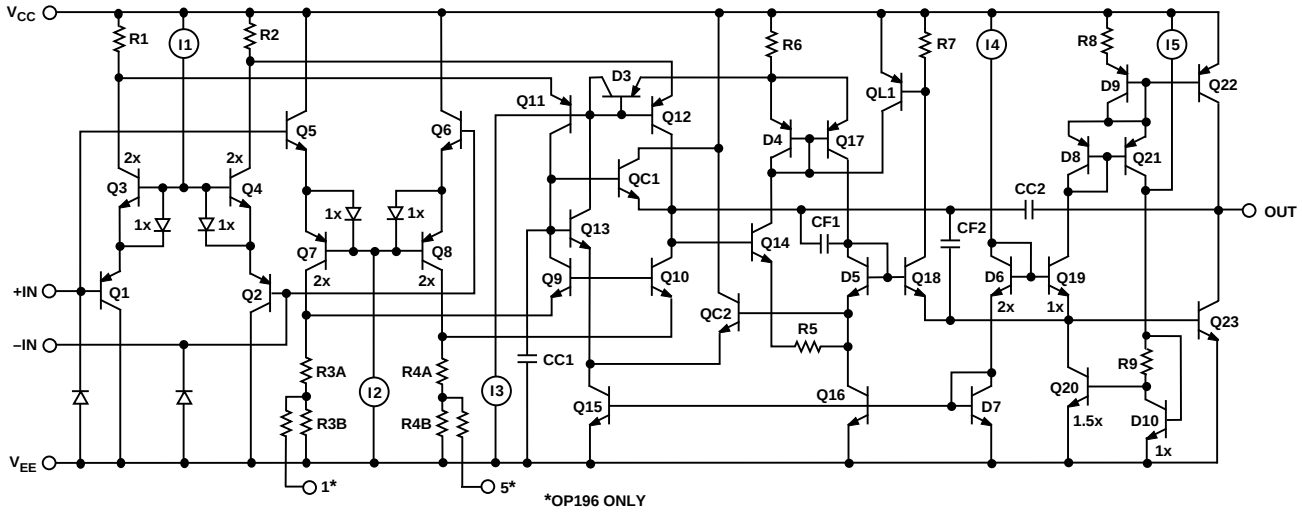


Figure 36. Simplified Schematic

APPLICATIONS INFORMATION

Functional Description

The OP196 family of operational amplifiers are single-supply, micropower, rail-to-rail input and output amplifiers. Input offset voltage (V_{OS}) is only 300 µV maximum, while the output will deliver ±5 mA to a load. Supply current is only 50 µA, while bandwidth is over 450 kHz and slew rate is 0.3 V/µs. Figure 36 is a simplified schematic of the OP196—it displays the novel circuit design techniques used to achieve this performance.

Input Overvoltage Protection

The OPx96 family of op amps uses a composite PNP/NPN input stage. Transistor Q1 in Figure 36 has a collector-base voltage of 0 V if +IN = V_{EE}. If +IN then exceeds V_{EE}, the junction will be forward biased and large diode currents will flow, which may damage the device. The same situation applies to +IN on the base of transistor Q5 being driven above V_{CC}. Therefore, the inverting and noninverting inputs must not be driven above or below either supply rail unless the input current is limited.

Figure 37 shows the input characteristics for the OPx96 family. This photograph was generated with the power supply pins connected to ground and a curve tracer's collector output drive connected to the input. As shown in the figure, when the input voltage exceeds either supply by more than 0.6 V, internal pn-junctions energize and permit current flow from the inputs to the supplies. If the current is not limited, the amplifier may be damaged. To prevent damage, the input current should be limited to no more than 5 mA.

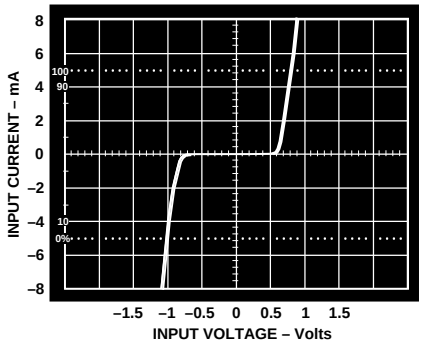


Figure 37. Input Overvoltage I-V Characteristics of the OPx96 Family

Output Phase Reversal

Some other operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these common-mode limited devices, external clamping diodes are required to prevent input signal excursions from exceeding the device's negative supply rail (i.e., GND) and triggering output phase reversal.

The OPx96 family of op amps is free from output phase reversal effects due to its novel input structure. Figure 38 illustrates the performance of the OPx96 op amps when the input is driven beyond the supply rails. As previously mentioned, amplifier input current must be limited if the inputs are driven beyond the supply rails. In the circuit of Figure 38, the source amplitude is ±15 V, while the supply voltage is only ±5 V. In this case, a 2 kΩ source resistor limits the input current to 5 mA.

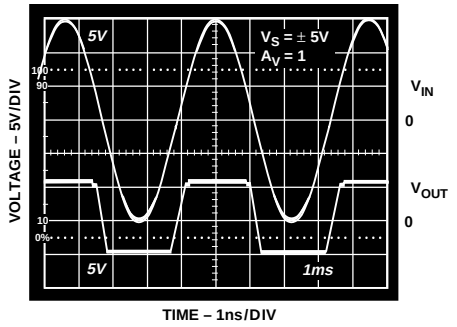


Figure 38. Output Voltage Phase Reversal Behavior

Input Offset Voltage Nulling

The OP196 provides two offset adjust terminals that can be used to null the amplifier's internal V_{OS}. In general, operational amplifier terminals should never be used to adjust system offset voltages. A 100 kΩ potentiometer, connected as shown in Figure 39, is recommended to null the OP196's offset voltage. Offset nulling does not adversely affect TCV_{OS} performance, providing that the trimming potentiometer temperature coefficient does not exceed ±100 ppm/°C.

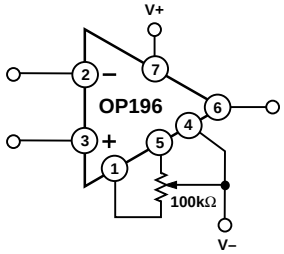
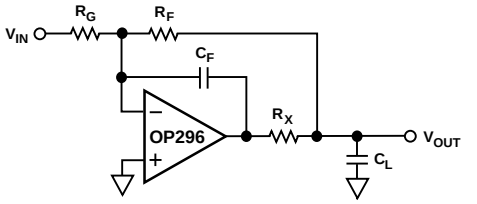


Figure 39. Offset Nulling Circuit

Driving Capacitive Loads

OP196 family amplifiers are unconditionally stable with capacitive loads less than 170 pF. When driving large capacitive loads in unity-gain configurations, an in-the-loop compensation technique is recommended, as illustrated in Figure 40.



$$R_X = \frac{R_O R_G}{R_F} \quad \text{WHERE } R_O = \text{OPEN-LOOP OUTPUT RESISTANCE}$$

$$C_F = \left[1 + \left(\frac{1}{|A_{CL}|}\right)\right]\left(\frac{R_F + R_G}{R_F}\right) C_L R_O$$

Figure 40. In-the-Loop Compensation Technique for Driving Capacitive Loads

A Micropower False-Ground Generator

Some single supply circuits work best when inputs are biased above ground, typically at 1/2 of the supply voltage. In these cases, a false-ground can be created by using a voltage divider buffered by an amplifier. One such circuit is shown in Figure 41.

This circuit will generate a false-ground reference at 1/2 of the supply voltage, while drawing only about 55 µA from a 5 V supply. The circuit includes compensation to allow for a 1 µF

bypass capacitor at the false-ground output. The benefit of a large capacitor is that not only does the false-ground present a very low dc resistance to the load, but its ac impedance is low as well.

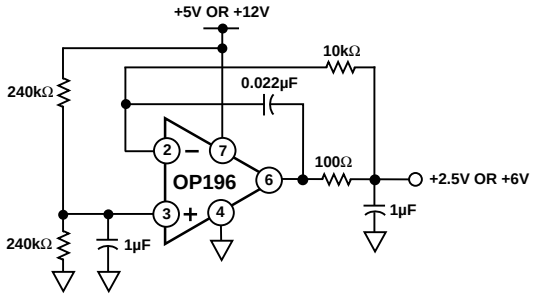


Figure 41. A Micropower False-Ground Generator

Single-Supply Half-Wave and Full-Wave Rectifiers

An OP296, configured as a voltage follower operating from a single supply, can be used as a simple half-wave rectifier in low frequency (<400 Hz) applications. A full-wave rectifier can be configured with a pair of OP296s as illustrated in Figure 42.

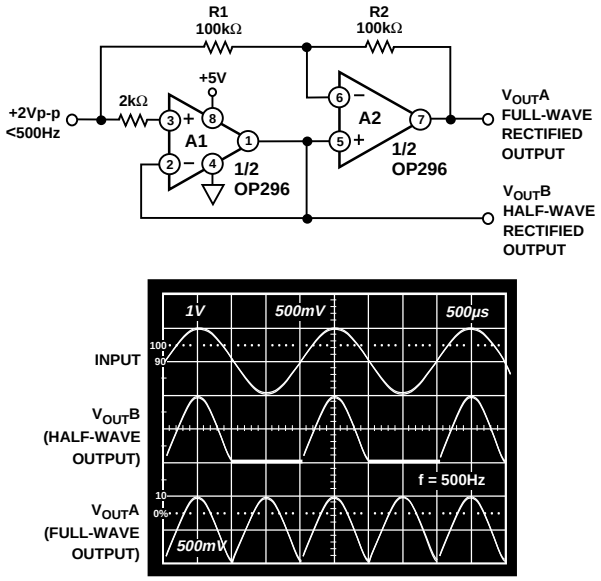


Figure 42. Single-Supply Half-Wave and Full-Wave Rectifiers Using an OP296

The circuit works as follows: When the input signal is above 0 V, the output of amplifier A1 follows the input signal. Since the noninverting input of amplifier A2 is connected to A1's output, op amp loop control forces A2's inverting input to the same potential. The result is that both terminals of R1 are at the same potential and no current flows in R1. Since there is no current flow in R1, the same condition must exist in R2; thus, the output of the circuit tracks the input signal. When the input signal is below 0 V, the output voltage of A1 is forced to 0 V. This condition now forces A2 to operate as an inverting voltage follower because the noninverting terminal of A2 is also at 0 V. The output voltage of $V_{OUT}A$ is then a full-wave rectified version of the input signal. A resistor in series with A1's noninverting input protects the ESD diodes when the input signal goes below ground.

Square Wave Oscillator

The oscillator circuit in Figure 43 demonstrates how a rail-to-rail output swing can reduce the effects of power supply variations on the oscillator's frequency. This feature is especially valuable in battery powered applications, where voltage regulation may not be available. The output frequency remains stable as the supply voltage changes because the RC charging current, which is derived from the rail-to-rail output, is proportional to the supply voltage. Since the Schmitt trigger threshold level is also proportional to supply voltage, the frequency remains relatively independent of supply voltage. For a supply voltage change from 9 V to 5 V, the output frequency only changes about 4 Hz. The slew rate of the amplifier limits the oscillation frequency to a maximum of about 200 Hz at a supply voltage of +5 V.

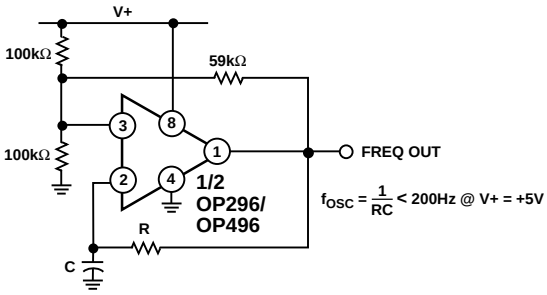


Figure 43. Square Wave Oscillator Has Stable Frequency Regardless of Supply Voltage Changes

A 3 V Low Dropout, Linear Voltage Regulator

Figure 44 shows a simple +3 V voltage regulator design. The regulator can deliver 50 mA load current while allowing a 0.2 V dropout voltage. The OP296's rail-to-rail output swing easily drives the MJE350 pass transistor without requiring special drive circuitry. With no load, its output can swing to less than the pass transistor's base-emitter voltage, turning the device nearly off. At full load, and at low emitter-collector voltages, the transistor beta tends to decrease. The additional base current is easily handled by the OP296 output.

The AD589 provides a 1.235 V reference voltage for the regulator. The OP296, operating with a noninverting gain of 2.43, drives the base of the MJE350 to produce an output voltage of 3.0 V. Since the MJE350 operates in an inverting (common-emitter) mode, the output feedback is applied to the OP296's noninverting input.

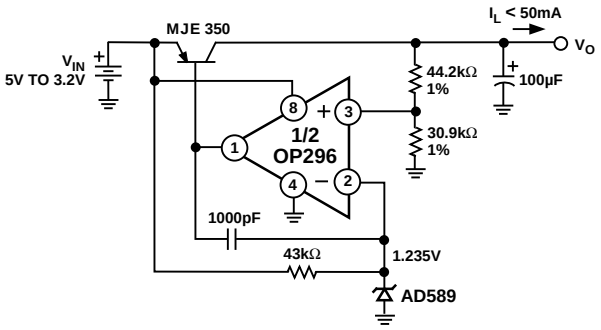


Figure 44. 3 V Low Dropout Voltage Regulator

Figure 45 shows the regulator's recovery characteristics when its output underwent a 20 mA to 50 mA step current change.

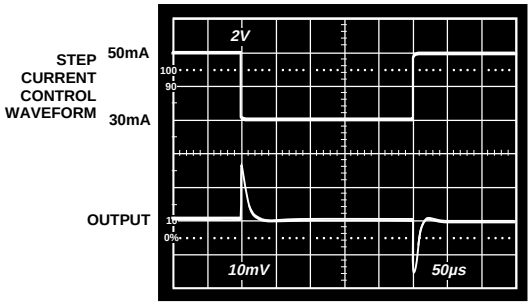


Figure 45. Output Step Load Current Recovery

Buffering a DAC Output

Multichannel TrimDACs (TrimDAC®) such as the AD8801/AD8803, are widely used for digital nulling and similar applications. These DACs have rail-to-rail output swings, with a nominal output resistance of 5 kΩ. If a lower output impedance is required, an OP296 amplifier can be added. Two examples are shown in Figure 45. One amplifier of an OP296 is used as a simple buffer to reduce the output resistance of DAC A. The OP296 provides rail-to-rail output drive while operating down to a 3 V supply and requiring only 50 µA of supply current.

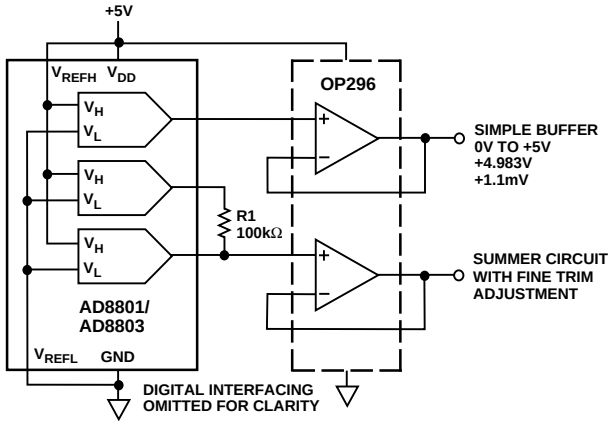


Figure 46. Buffering a TrimDAC Output

The next two DACs, B and C, sum their outputs into the other OP296 amplifier. In this circuit DAC C provides the coarse output voltage setting and DAC B is used for fine adjustment. The insertion of R1 in series with DAC B attenuates its contribution to the voltage sum node at the DAC C output.

A High-Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 47 is an example of a +5 V, single-supply high-side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP296's rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET is used as the feedback element in the circuit to convert the op amp's differential input voltage into a current. This current is then applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by:

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1} \right) \times I_L$$

For the element values shown, the Monitor Output's transfer characteristic is 2.5 V/A.

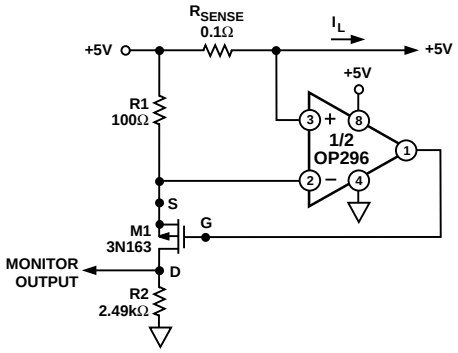


Figure 47. A High-Side Load Current Monitor

A Single-Supply RTD Amplifier

The circuit in Figure 48 uses three op amps on the OP496 to produce a bridge driver for an RTD amplifier while operating from a single +5 V supply. The circuit takes advantage of the OP496's wide output swing to generate a bridge excitation voltage of 3.9 V. An AD589 provides a 1.235 V reference for the bridge current. Op amp A1 drives the bridge to maintain 1.235 V across the parallel combination of the 6.19 kΩ and 2.55 MΩ resistors, which generates a 200 µA current source. This current divides evenly and flows through both halves of the bridge. Thus, 100 µA flows through the RTD to generate an output voltage which is proportional to its resistance. For improved accuracy, a 3-wire RTD is recommended to balance the line resistance in both 100 Ω legs of the bridge.

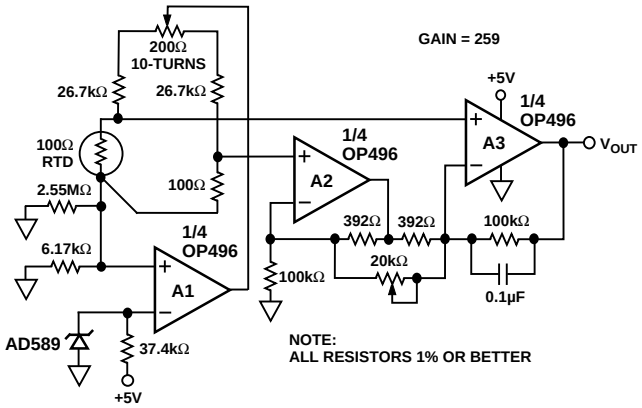


Figure 48. A Single Supply RTD Amplifier

TrimDAC is a registered trademark of Analog Devices Inc.

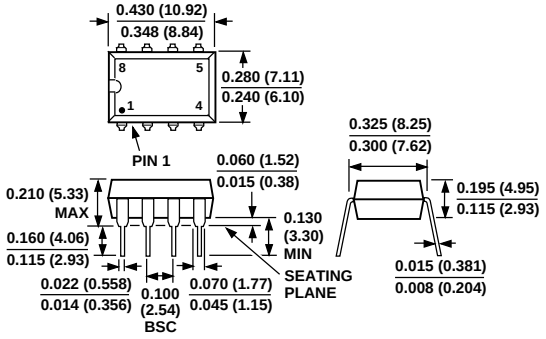
Amplifiers A2 and A3 are configured in a two op amp instrumentation amplifier configuration. For ease of measurement, the IA resistors are chosen to produce a gain of 259, so that each 1°C increase in temperature results in a 10 mV increase in the output voltage. To reduce measurement noise, the bandwidth of the amplifier is limited. A 0.1 µF capacitor, connected in parallel with the 100 kΩ resistor on amplifier A3, creates a pole at 16 Hz.

```
* OP496 SPICE Macro-model          Rev. A, 5/95
*                                  ARG / ADSC
*
* Copyright 1995 by Analog Devices
*
* Refer to "README.DOC" file for License Statement.
* Use of this model indicates your acceptance of the
* terms and provisions in the License Statement.
*
* Node assignments
*                      Noninverting input
*                      |     Inverting input
*                      |     |     Positive supply
*                      |     |     |     Negative supply
*                      |     |     |     |     Output
*                      |     |     |     |     |
.SUBCKT OP496          1     2     99    50    49
*
* INPUT STAGE
*
IREF   21    50    1U
QB1    21    21    99    99    QP    1
QB2    22    21    99    99    QP    1
QB3    4     21    99    99    QP    1.5
QB4    22    22    50    50    QN    2
QB5    11    22    50    50    QN    3
Q1     5     4     7     50    QN    2
Q2     6     4     8     50    QN    2
Q3     4     4     7     50    QN    1
Q4     4     4     8     50    QN    1
Q5     50    1     7     99    QP    2
Q6     50    3     8     99    QP    2
EOS    3     2     POLY(1)     (17,98) 35U   1
Q7     99    1     9     50    QN    2
Q8     99    3     10    50    QN    2
Q9     12    11    9     99    QP    2
Q10    13    11    10    99    QP    2
Q11    11    11    9     99    QP    1
Q12    11    11    10    99    QP    1
R1     99    5     50K
R2     99    6     50K
R3     12    50    50K
R4     13    50    50K
IOS    1     2     0.75N
C10    5     6     3.183P
C11    12    13    3.183P
CIN    1     2     1P
*
* GAIN STAGE
*
EREF   98    0     POLY(2)     (99,0)    (50,0)    0   0.5   0.5
G1     98    15    POLY(2)     (6,5)     (13,12)   0   10U   10U
R10    15    98    251.641MEG
CC     15    49    8P
D1     15    99    DX
D2     50    15    DX
*
* COMMON MODE STAGE
*
ECM    16    98    POLY(2)     (1,98)    (2,98)    0   0.5   0.5
R11    16    17    1MEG
R12    17    98    10
*
* OUTPUT STAGE
*
ISY    99    50    20U
EIN    35    50    POLY(1)     (15,98)   1.42735   1
Q24    37    35    36    50    QN    1
QD4    37    37    38    99    QP    1
Q27    40    37    38    99    QP    1
R5     36    39    150K
R6     99    38    45K
Q26    39    42    50    50    QN    3
QD5    40    40    39    50    QN    1
Q28    41    40    44    50    QN    1
QL1    37    41    99    99    QP    1
R7     99    41    10.7K
I4     99    43    2U
QD7    42    42    50    50    QN    2
QD6    43    43    42    50    QN    2
Q29    47    43    44    50    QN    1
Q30    44    45    50    50    QN    1.5
QD10   45    46    50    50    QN    1
R9     45    46    175
Q31    46    47    48    99    QP    1
QD8    47    47    48    99    QP    1
QD9    48    48    51    99    QP    5
R8     99    51    2.9K
I5     99    46    1U
Q32    49    48    99    99    QP    10
Q33    49    44    50    50    QN    4
.MODEL DX    D()
.MODEL QN    NPN(BF=120VAF=100)
.MODEL QP    PNP(BF=80  VAF=60)
.ENDS
```

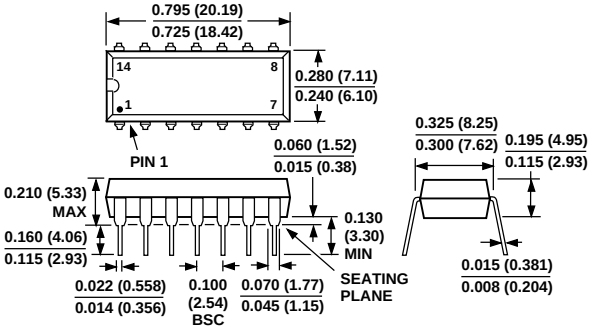
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

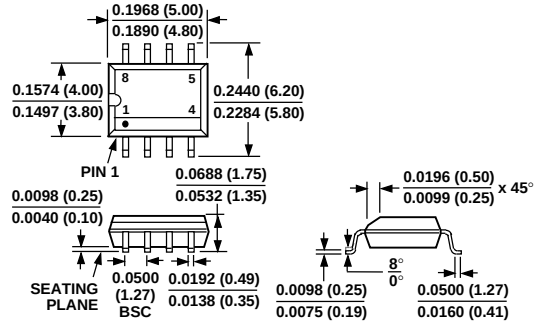
8-Lead Epoxy DIP (P Suffix)



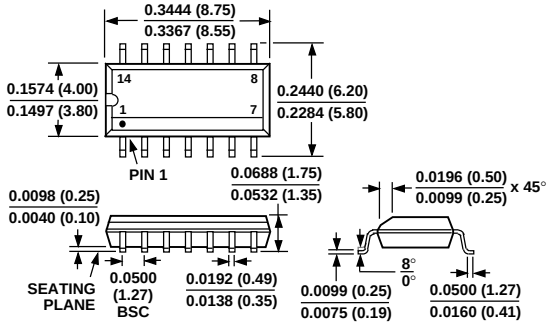
14-Lead Epoxy DIP (P Suffix)



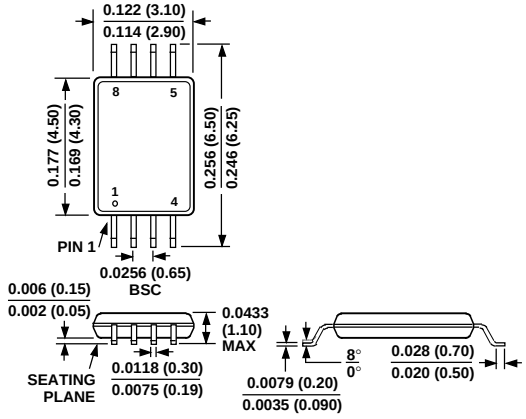
8-Lead SOIC (S Suffix)



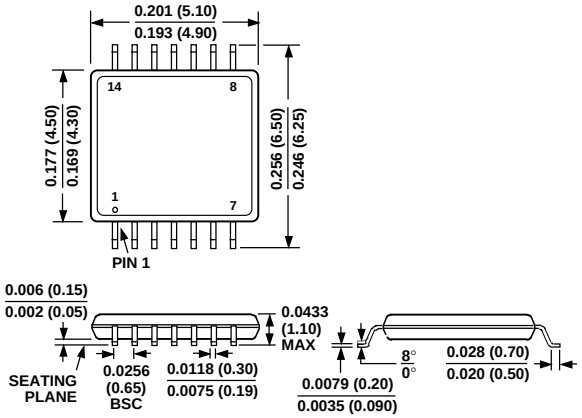
14-Lead Narrow-Body SO (S Suffix)



8-Lead TSSOP (RU Suffix)



14-Lead TSSOP (RU Suffix)



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