# ANALOG DEVICES

# Product Preview

## ADSP-2189L 66 MIPS 16-bit DSP Processor

The information that follows describes the feature set and pin description of the recently announced 66MHz ADSP-2189L.

### DSP Core
*15 ns Instruction Cycle Time (66 MIPS) from 33 Mhz Crystal @ 2.5Volts*
**ADSP-21xx Family Code Compatible, with Instruction Set Extensions Compatible with all ADSP-218x Derivatives**
**Single-Cycle Instruction Execution**
**Single-Cycle Context Switch**
**Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 100-cycle Recovery**
**Low Power IDLE Modes**

### On-Chip Integration
**192K Bytes of On-Chip SRAM, Configured as 16K Words Directly Addressable Program Memory Plus Two 8K Word Overlay Segments 16K Words Directly Addressable Data Memory Plus Four 8K Word Overlay Segments**
**100-Lead TQFP Package**

### System Interface
**Two Double-Buffered Serial Ports (SPORTs) with Automatic Data Buffering and Companding Hardware**

**Selectable 2.5V or 3.3V Level Compatible I/O**
**UART Emulation through Software SPORT Reconfiguration**
**Up to 13 Programmable Flag Pins**
**Up to 6 External Interrupts**

### Mode Selectable DMA Support
**During RESET, the user can choose one of two external interface options:**

**8-Bit DMA for Transparent Program and Data Memory Transfers**
*with*
**Byte Memory Interface for Storage of Data Tables & Program Overlays**
**I/O Memory Interface with 2048 Locations for Parallel Peripheral Support**
**Programmable Memory Strobe & Separate I/O Memory Space for "Glueless" System Design**

*OR*
**16-Bit Internal DMA Port for High-Speed Host Access to Internal Memory and some external addressing capabilities**
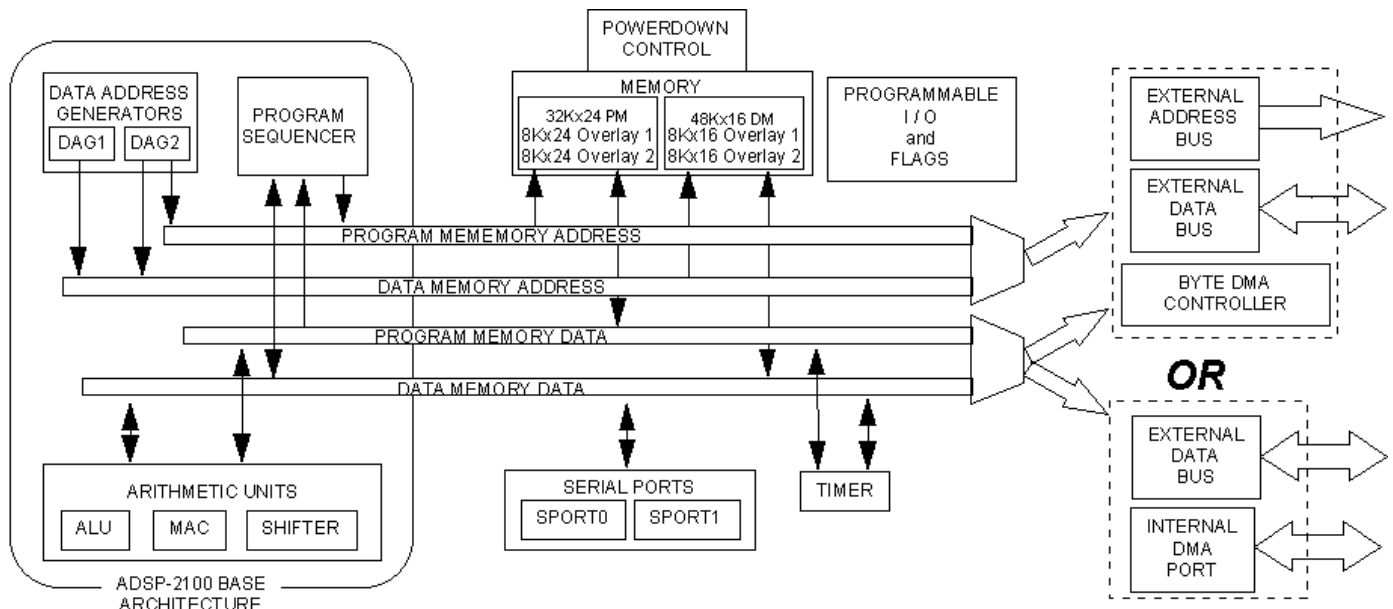


**Functional Block Diagram**

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**Product Description**

The ADSP-2189L processor combines the ADSP-21xx Family processor core with extensive peripheral functionality, including two serial ports, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, an internal DMA port, and on-chip program and data RAM. The on-chip RAM is configured as 16K words plus two 8K word segments of 24-bit program RAM, and 16K words plus four 8K word segments of 16-bit data RAM. Powerdown circuitry is also provided to meet the low power requirements of battery operated equipment. The ADSP-2189L supports the ADSP-2100 family instruction enhancements found in the ADSP-2181, which include bit manipulation operations, ALU constants, result-free ALU operations, multiplier $x^2$ operation, biased rounding, I/O space transfers, and global interrupt masking.

**Pin Descriptions**

The ADSP-2189L will be available in a 100-lead TQFP package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt, and external bus pins have dual, multiplexed functionality. The external bus pins are configured during RESET only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In the cases where pin functionality is re-configurable, the default state is shown in plain text, alternate functionality in *italics*.

| Pin Name(s) | # of Pins | Input/ Output | Function |
|---|---|---|---|
| $\overline{\text{RESET}}$ | 1 | I | Processor Reset Input |
| $\overline{\text{BR}}$ | 1 | I | Bus Request Input |
| $\overline{\text{BG}}$ | 1 | O | Bus Grant Output |
| $\overline{\text{BGH}}$ | 1 | O | Bus Grant Hung Output |
| $\overline{\text{DMS}}$ | 1 | O | Data Memory Select Output |
| $\overline{\text{PMS}}$ | 1 | O | Program Memory Select Output. |
| $\overline{\text{IOMS}}$ | 1 | O | I/O Space Memory Select Output |
| $\overline{\text{BMS}}$ | 1 | O | Byte Memory Select Output |
| $\overline{\text{CMS}}$ | 1 | O | Combined Memory Select Output |
| $\overline{\text{RD}}$ | 1 | O | Memory Read Enable Output |
| $\overline{\text{WR}}$ | 1 | O | Memory Write Enable Output |
| $\overline{\text{IRQ2}}$ <br> *PF7* | 1 | I <br> *I/O* | Edge- or Level-Sensitive Interrupt Request* <br> *Programmable I/O Pin* |
| $\overline{\text{IRQL1}}$, $\overline{\text{IRQL0}}$ <br> *PF6, PF5* | 2 | I <br> *I/O* | Level-Sensitive Interrupt Requests* <br> *Programmable I/O Pins* |
| $\overline{\text{IRQE}}$ <br> *PF4* | 1 | I <br> *I/O* | Edge-Sensitive Interrupt Request* <br> *Programmable I/O Pin* |
| PF3 | 1 | I/O | Programmable I/O Pin |
| Mode C / PF2 | 1 | I / I/O | Mode Select Input - Checked only during RESET <br> Programmable I/O Pin during normal operation |
| Mode B / PF1 | 1 | I / I/O | Mode Select Input - Checked only during RESET <br> Programmable I/O Pin during normal operation |

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| | | | |
|---|---|---|---|
| Mode A / PF0 | 1 | I / I/O | Mode Select Input - Checked only during RESET Programmable I/O Pin |
| CLKIN, XTAL | 2 | I | Clock or Quartz Crystal Input |
| CLKOUT | 1 | O | Processor Clock Output |
| SPORT0 | 5 | I/O | Serial Port I/O Pins |
| SPORT1 *IRQ1:0, FI, FO* | 5 | I/O *I/O* | Serial Port I/O Pins *Edge- or Level-Sensitive Interrupts, Flag In, Flag Out*** |
| PWD | 1 | I | Powerdown Control Input |
| PWDACK | 1 | O | Powerdown Control Output |
| FL0, FL1, FL2 | 3 | O | Output Flags |
| V$_{DD}$ and GND | 16 | I | Power and Ground |
| EZ-Port | 9 | I/O | For emulation use |

\* Interrupt/Flag Pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by an external devices, or set as a programmable flag.

\*\* SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2189L processor can be used in one of two modes, Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during RESET and cannot be changed while the processor is running.

*Full Memory Mode Pins (Mode C = 0)*

| Pin Name(s) | # of Pins | Input/ Output | Function |
|---|---|---|---|
| A13:0 | 14 | O | Address Output Pins for Program, Data, Byte and I/O Spaces |
| D23:0 | 24 | I/O | Data I/O Pins for Program, Data, Byte, and I/O spaces (8 MSBs are also used as Byte Memory addresses). |

*Host Mode Pins (Mode C = 1)*

| Pin Name(s) | # of Pins | Input/ Output | Function |
|---|---|---|---|
| IDMA Address/DATA (IAD15:0) | 16 | I/O | IDMA Port Address/Data Bus |
| A0 | 1 | O | Address pin for external IO, Program, Data, or Byte access |
| D23:8 | 16 | I/O | Data I/O Pins for Program, Data, Byte, and I/O spaces |
| IWR | 1 | I | IDMA Write Enable |
| IRD | 1 | I | IDMA Read Enable |

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| IAL | 1 | I | IDMA Address Latch Pin |
|-----|---|---|------------------------|
| IS | 1 | I | IDMA Select |
| IACK | 1 | O | IDMA Port Acknowledge |
| | | | |

In Host Mode, external peripheral addresses can be decoded using the A0, CMS, PMS, DMS, and IOMS signals.

Overlay Memory Support

The ADSP-2189L increases program and data overlay memory to 4 internal and 2 external 8K word overlay segments. Program and data overlay segments are selected via 4-bit program and data overlay registers as shown below.

*Program/Data Memory Overlay Registers*

| Register Value | Overlay Segment Enabled |
|----------------|-------------------------|
| 0 | Internal Non-Overlay |
| 1 | External Overlay 1 |
| 2 | External Overlay 2 |
| 3 | Reserved |
| 4 | Internal Overlay 1 |
| 5 | Internal Overlay 2 |
| 6 | Internal Overlay 3   [DM Only] |
| 7 | Internal Overlay 4   [DM Only] |
| 8-15 | Reserved |

IDMA transfers to overlay segments are selected by the newly defined IDMA Overlay Register located at DM[0x3FE7]. IDMA Overlay Register bits are implemented as follows.

IDMA Overlay Register bits---    3:0    PM overlay segments
                                 7:4    DM overlay segments
                                 15:8   Reserved-Must be set to zero.

*IDMA Overlay Register*

| Nibble Value | Overlay Segment Enabled |
|--------------|-------------------------|
| 0 | Internal Non-Overlay (Default) |
| 1 | Reserved |
| 2 | Reserved |
| 3 | Reserved |
| 4 | Internal Overlay 1 |
| 5 | Internal Overlay 2 |
| 6 | Internal Overlay 3   [DM Only] |
| 7 | Internal Overlay 4   [DM Only] |
| 8-15 | Reserved |

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The IDMA address latch cycle is controlled via IAD[15] and has been modified to allow a host to write either the IDMA address or a new value to the IDMA Overlay Register.  With IAL and IS\ asserted, IAD[15] = 0 signifies a normal address latch; IAD[15] =1 signifies an IDMA Overlay Register latch cycle.

BDMA transfers to overlay segments are controlled via BDMA overlay bits in the BDMA Control Register. The previously reserved bits 7:4 of the BDMA Control Register are now used to select overlay pages for BDMA transfers.  Overlay pages are selected as follows.

*BDMA Overlay Register*

| Bits 7:4 Value | Overlay Segment Enabled |
|---|---|
| 0 | Internal Non-Overlay (Default) |
| 1 | Reserved |
| 2 | Reserved |
| 3 | Reserved |
| 4 | Internal Overlay 1 |
| 5 | Internal Overlay 2 |
| 6 | Internal Overlay 3   [DM Only] |
| 7 | Internal Overlay 4   [DM Only] |
| 8-15 | Reserved |