NOTICE OF REVISION (NOR)

(See MIL-STD-480 for instructions)
This revision described below has been authorized for the document listed.

DATE (YYMMDD)	Form Approved OMB No. 0704-0188
91/11/18	

1. ORIGINATOR NAME AND ADDRESS	2. CAGE CODE	3. NOR NO.
Defense Electronics Supply Center Dayton, Ohio 45444-5277	67268	5962-R057-92
	4. CAGE CODE	5. DOCUMENT NO.
	67268	5962-89697
6. TITLE OF DOCUMENT Microcircuit, Linear, 16-Bit, Voltage Output DAC, Monolithic Silicon.	7. REVISION LETTER (Current)	(New) A
	8. ECP NO. 5962-89697ECP-01	

9. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

10. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A"
Revisions description column; add "Changes in accordance with NOR 5962-R057-92".
Revisions date column; add "91-11-18".

Sheet 4: Table I; Resolution, RES, change minimum limit from -16 BITS to 16 BITS and delete maximum limit of +16 BITS. V_{REF+} range, V_{REF+}, add footnote "11/" in test column. V_{REF-} range, V_{REF-}, add footnote "11/" in test column.

Sheet 5: Table I; Output voltage swing, V_{SWING}, add footnote "11/" in test column. Input voltage high level, V_{IH}, change Group A subgroups from "1, 2, 3" to "7, 8". Input voltage low level, V_{IL}, change Group A subgroups from "1, 2, 3" to "7, 8".

Sheet 7: Table I; Add footnote "11/ If not tested, guaranteed to the limits specified in table I herein."

Sheet 15: Table II; Final electrical test parameters, add subgroups "7, 8".

11. THIS SECTION FOR GOVERNMENT USE ONLY

a. CHECK ONE

[X] EXISTING DOCUMENT SUPPLEMENTED BY THIS NOR MAY BE USED IN MANUFACTURE.

[ ] REVISED DOCUMENT MUST BE RECEIVED BEFORE MANUFACTURER MAY INCORPORATE THIS CHANGE.

[ ] CUSTODIAN OF MASTER DOCUMENT SHALL MAKE ABOVE REVISION AND FURNISH REVISED DOCUMENT TO:

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT DESC-ECS	SIGNATURE AND TITLE BRANCH CHIEF	DATE (YYMMDD) 91/11/18
12. ACTIVITY ACCOMPLISHING REVISION DESC-ECS	REVISION COMPLETED (Signature) Sandra Rooney	DATE (YYMMDD) 91/11/18

DD Form 1695, JUL 88 Previous editions are obsolete.

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV																							
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17						

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Rick C. Office

CHECKED BY
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APPROVED BY

DRAWING APPROVAL DATE
03 APRIL 1990

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 16-BIT, VOLTAGE OUTPUT DAC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89697

SHEET 1 OF 17

DESC FORM 193
SEP 87

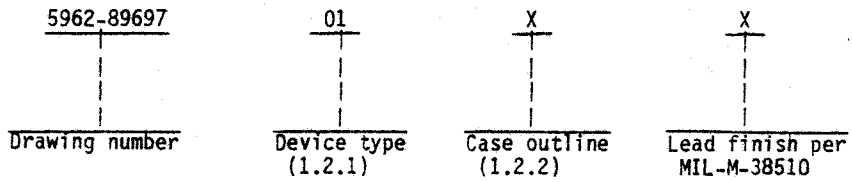
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1650

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD7846	L^2CMOS 16-bit voltage output DAC

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), leadless chip carrier package

1.3 Absolute maximum ratings.

Positive supply voltage to DGND (V_{DD})	-0.3 V dc to +17 V dc
Positive logic supply voltage to DGND (V_{CC})	-0.3 V dc to +7.0 V dc
Negative supply voltage to DGND (V_{SS})	+0.3 V dc to -17 V dc
V_{REF+} to DGND	±25 V dc
V_{REF-} to DGND	±25 V dc
V_{OUT} to DGND	±25 V dc 1/
R_{IN} to DGND	±25 V dc
Logic input voltage to DGND	-0.3 V dc to V_{CC} +0.3 V dc
Logic output voltage to DGND	-0.3 V dc to V_{CC} +0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation to 75°C (P_D)	1000 mW 2/
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Negative supply voltage (V_{SS})	-14.25 V dc to -15.75 V dc
Positive supply voltage (V_{DD})	+14.25 V dc to +15.75 V dc
Positive logic supply voltage (V_{CC})	+4.75 V dc to +5.25 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ V_{OUT} may be shorted to DGND, V_{DD}, V_{SS}, V_{CC} provided that the power dissipation of the package is not exceed.
2/ Derates above T_A = +75°C at 10 mW/°C.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Output voltage ranges. The output voltage ranges shall be as specified on figure 3.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 4.

3.2.5 Switching characteristics. The switching characteristics shall be as specified on figure 5.

3.2.6 Load circuits. The load circuits shall be as specified on figure 6.

3.2.7 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Resolution	RES		1,2,3	-16	+16	BITS
Relative accuracy	R_A	Unipolar output 2/	1,2,3	-16	+16	LSB
Differential nonlinearity 3/	DNL		1,2,3	-1	+1	
Gain error 4/	A_E		1	-16	+16	
			2,3	-24	+24	
Offset error	O_E		1	-16	+16	
			2,3	-24	+24	
Relative accuracy	R_A	Bipolar output 5/	1,2,3	-8	+8	LSB
Differential nonlinearity 3/	DNL		1,2,3	-1	+1	
Gain error 4/	A_E		1	-8	+8	
			2,3	-16	+16	
Offset error 4/	O_E		1	-8	+8	
			2,3	-16	+16	
Bipolar zero error	BIP_e		1	-8	+8	
			2,3	-16	+16	
Reference input resistance	R_{REFIN}	Resistance from V_{REF-} to V_{REF+}	1,2,3	20	40	kΩ
V_{REF+} range	V_{REF+}		1,2,3	V_{SS} +6.0	V_{DD} -6.0	V
V_{REF-} range	V_{REF-}		1,2,3	V_{SS} +6.0	V_{DD} -6.0	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Output voltage swing	V_{SWING}		1,2,3	V_{SS} +4.0	V_{DD} -3.0	V
Input voltage high level	V_{IH}		1,2,3	2.4		V
Input voltage low level	V_{IL}		1,2,3		0.8	V
Digital input current	I_{IN}		1,2,3		±10	µA
Output voltage high level	V_{OH}	I_{SOURCE} = 400 µA	1,2,3	4.0		V
Output voltage low level	V_{OL}	I_{SINK} = 1.6 mA	1,2,3		0.4	V
Floating state leakage current	I_{LKG}	DB0-DB15 = 0 to V_{CC} V	1,2,3		±10	µA
Positive power supply current	I_{DD}	V_{OUT} unloaded 6/	1,2,3		5.0	mA
Negative power supply current	I_{SS}		1,2,3		5.0	
Positive logic supply current	I_{CC}		1,2,3		1.0	
Power supply sensitivity 7/	PSS		1,2,3		2.0	LSB/V
Floating state output capacitance	C_{OUT}	See 4.3.1b	4		10	pF
Digital input capacitance	C_{IN}	See 4.3.1b	4		10	pF
Functional test		See 4.3.1c	7,8			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_A < +125°C$ Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
R/$\overline{W}$ to $\overline{CS}$ setup time	t_1	See figure 5 8/	9	40		ns
			10,11	50		
$\overline{CS}$ pulse width (write cycle)	t_2		9	150		
			10,11	190		
R/$\overline{W}$ to $\overline{CS}$ hold time	t_3		9	40		
			10,11	50		
Data setup time	t_4		9	110		
			10,11	120		
Data hold time	t_5		9,10,11	0		
Data access time 9/	t_6		9		230	
			10,11		320	
Bus relinquish 10/	t_7		9	10	80	
			10,11	10	90	
$\overline{CLR}$ setup time	t_8		9,10,11	20		
$\overline{CLR}$ pulse width	t_9		9,10,11	150		
$\overline{CLR}$ hold time	t_{10}		9,10,11	0		
$\overline{LDAC}$ pulse width	t_{11}		9	80		
			10,11	100		
$\overline{CS}$ pulse width (read cycle)	t_{12}		9	240		
			10,11	330		

See footnotes on next page.

1/ Unless otherwise specified, 14.25 V dc $\leq V_{DD} \leq$ 15.75 V dc, -14.25 V dc $\leq V_{SS} \leq$ -15.75 V dc and 4.75 V dc $\leq V_{CC} \leq$ 5.25 V dc. V_{OUT} loaded with 3 kΩ, 1000 pF to 0 V. V_{REF+} = +5.0 V dc, R_{IN} connected to 0 V.

2/ V_{REF-} = 0 V, V_{OUT} = 0 V to 10 V, 1 LSB = 153 μV.

3/ Monotonicity is guaranteed over full temperature range.

4/ V_{OUT}load = 10 MΩ.

5/ V_{REF} = -5.0 V, V_{OUT} = -10 V to +10 V, 1 LSB = 305 μV.

6/ The device is functional with a power supply of ±12 V.

7/ Sensitivity of gain error, offset error and bipolar zero error to V_{DD}, V_{SS} variations.

8/ All input control signals are specified with $t_R = t_F$ = 5.0 ns (10 percent to 90 percent of +5.0 V) and timed from a voltage level of 1.6 V.

9/ t_6 is measured with the load circuits for access time on figure 6 and defined as the time required for an output to cross 0.8 V or 2.4 V.

10/ t_7 is defined as the time required for an output to change 0.5 V when loaded with the circuits for bus relinquish time on figure 6.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.7 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Device type	01
Case outlines	X and 3
Terminal number	Terminal symbol
1	DB2
2	DB1
3	DB0
4	V_{DD}
5	V_{OUT}
6	R_{IN}
7	V_{REF+}
8	V_{REF-}
9	V_{SS}
10	DB15
11	DB14
12	DB13
13	DB12
14	DB11
15	DB10
16	DB9
17	DB8
18	DB7
19	DB6
20	DGND
21	V_{CC}
22	$R/\overline{W}$
23	$\overline{CS}$
24	$\overline{CLR}$
25	$\overline{LDAC}$
26	DB5
27	DB4
28	DB3

FIGURE 1. Terminal connections.

$\overline{CS}$	R/$\overline{W}$	$\overline{LDAC}$	$\overline{CLR}$	Function
1	X	X	X	3-State DAC I/O latch in high-Z state
0	0	X	X	DAC I/O latch loaded with DB15-DB0
0	1	X	X	Contents of DAC I/O latch available on DB15-DB0
X	X	0	1	Contents of DAC I/O latch transferred to DAC latch
X	0	X	0	DAC latch loaded with 000 ... 000
X	1	X	0	DAC latch loaded with 100 ... 000

0 = Low
1 = High
X = Don't care

FIGURE 2. Truth table.

Output range	V_{REF+}	V_{REF-}	R_{IN}
0 V to +5.0 V	+5.0 V	0 V	V_{OUT}
0 V to +10 V	+5.0 V	0 V	0 V
+5.0 V to -5.0 V	+5.0 V	-5.0 V	V_{OUT}
+5.0 V to -5.0 V	+5.0 V	0 V	+5.0 V
+10 V to -10 V	+5.0 V	-5.0 V	0 V

FIGURE 3. Output voltage ranges.

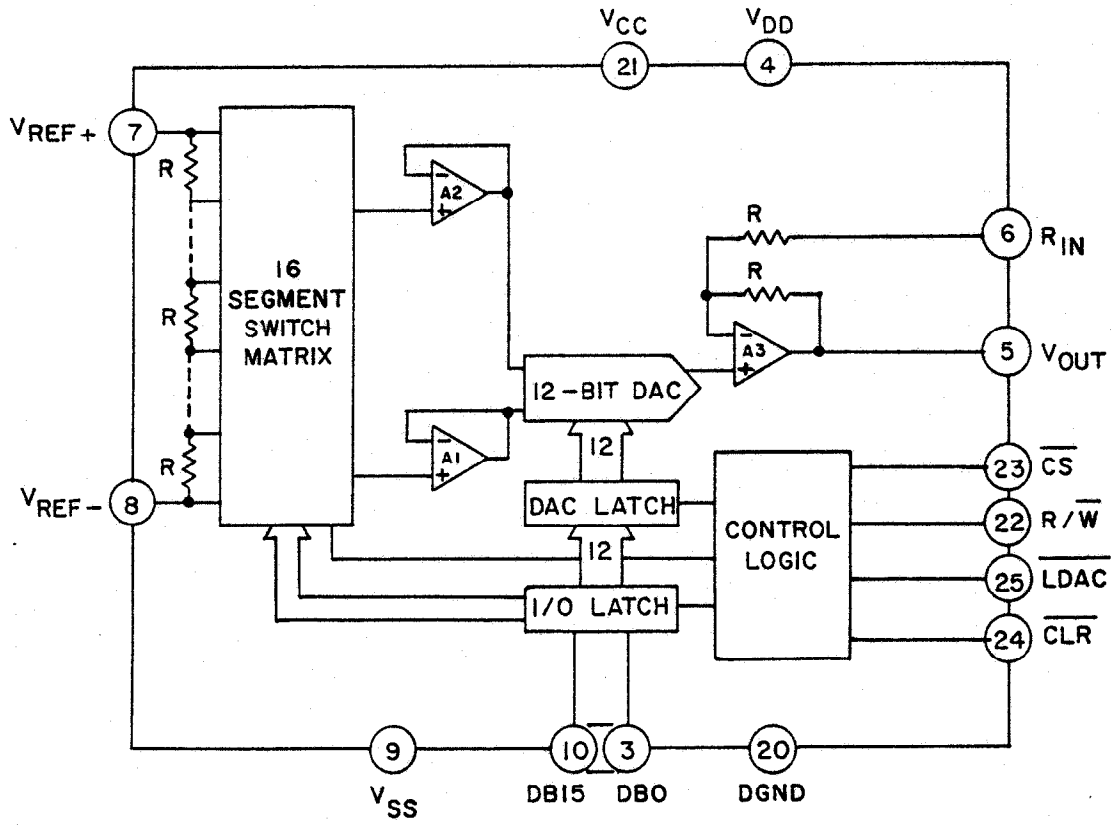


FIGURE 4. Logic diagram.

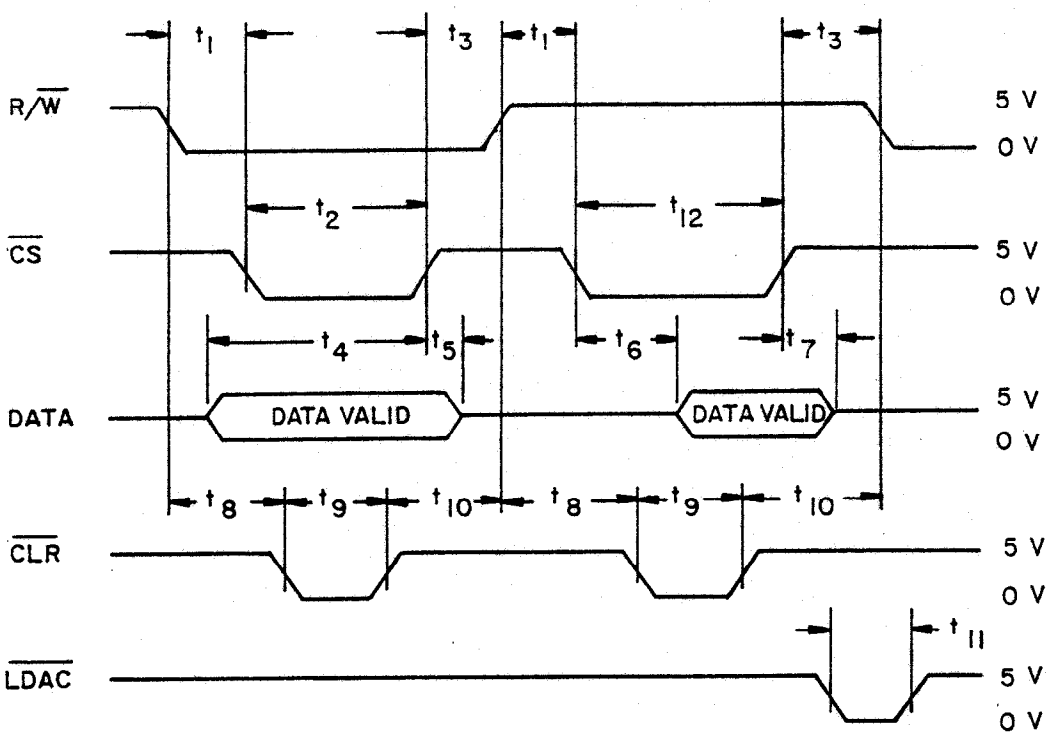
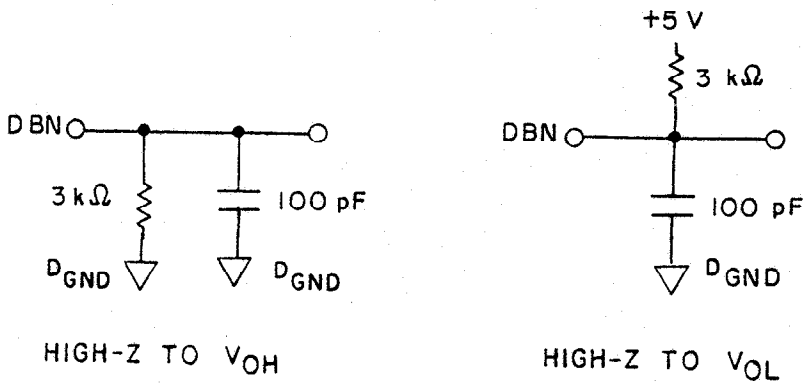


FIGURE 5. Switching characteristics.

Load circuits for access time (t_6)



Load circuits for bus relinquish time (t_7)

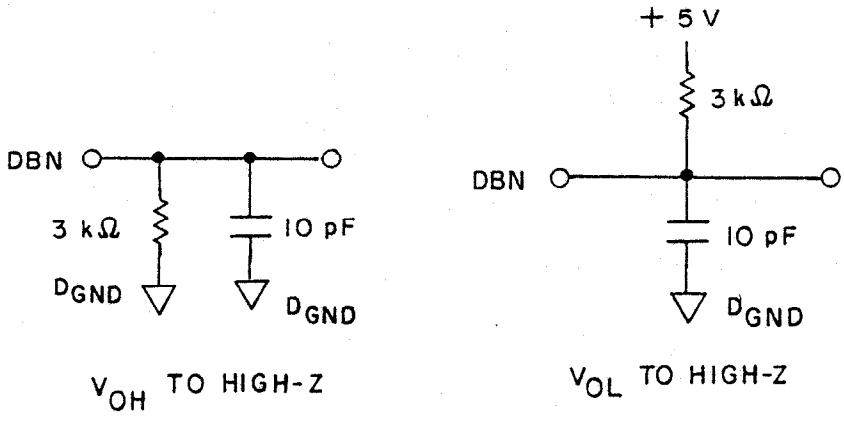


FIGURE 6. Load circuits.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

c. Subgroups 7 and 8 testing shall be sufficient to verify the truth table.

d. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3
Group A test requirements (method 5005)	1,2,3,7,8,9, 10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.
** Subgroups 10 and 11 are guaranteed, but not tested to the limits specified in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronic Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordiantion and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Pin description. The pin description is as follows:

Pin	Description
DB2-DB0	Data I/O pins. DB0 is LSB.
V_{DD}	Positive supply for analog circuitry. This is a +15 V nominal.
V_{OUT}	DAC output voltage pin.
R_{IN}	Input to summing resistor of DAC output amplifier. This is used to select output voltage ranges. See figure 2.
V_{REF+}	V_{REF+} input. The DAC is specified for V_{REF+} = +5.0 V.
V_{REF-}	V_{REF-} input. For unipolar operation connect V_{REF-} to 0 V and for bipolar operation connect it to -5.0 V. The device is specified for both conditions.
V_{SS}	Negative supply for analog circuitry. This is -15 V nominal.
DB15-DB6	Data I/O pins. DB15 is MSB.
DGND	Ground pin for logic circuitry.
V_{CC}	Positive supply for logic circuitry. This is +5.0 V nominal.
R/$\overline{W}$	R/$\overline{W}$ input. This can be used to load data to the DAC or to read back the DAC latch contents.
$\overline{CS}$	Chip select input. This selects the device.
$\overline{CLR}$	Clear input. The DAC can be cleared to 000... 000 or 100...000. See figure 2.
$\overline{LDAC}$	Asynchronous load input to DAC.
DB5-DB3	Data I/O pins.

6.7 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this documents.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8969701XX	24355	AD7846SQ/883B
5962-89697013X	24355	AD7846SE/883B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
24355	Analog Devices Route 1 Industrial Park P.O. Box 9106 Norwood, MA 02062 Point of contact: 181 Ballardvale Street Wilmington, MA 01887-1024