NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
95-01-25	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	67268	5962-R060-95
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-91690**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
Microcircuit, Linear, 12-Bit A/D Converter with Microprocessor Interface, Monolithic Silicon.	a. CURRENT C	b. NEW D	No registered users

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "D".
Revisions description column; add "Changes in accordance with NOR 5962-R060-95".
Revisions date column; add "95-01-25".
Revision level block; add "D".
Rev status of sheets; For sheets 1 and 10, add "D".

Sheet 10: Figure 1, Terminal connections; Terminal symbol columns, Change column for device types "01 and 02" to device types "01, 02, and 04". Change column for device types "03 and 04" to device type "03".
Revision level block; add "D".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DESC-ELDS	Michael A. Frye

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Microelectronics Branch	Michael A. Frye	95-01-25

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)
DESC-ELDS	Sandra Rooney	95-01-25

DD Form 1695, APR 92 Previous editions are obsolete

NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE (YYMMDD)	Form Approved OMB No. 0704-0188
95-01-17	

2. PROCURING ACTIVITY NO.	
3. DODAAC	

4. ORIGINATOR	b. ADDRESS (Street, City, State, Zip Code)	5. CAGE CODE	6. NOR NO.
	Defense Electronics Supply Center 1507 Wilmington Pike Dayton, OH 45444-5270	67268	5962-R017-95
a. TYPED NAME (First, Middle Initial, Last)		7. CAGE CODE 67268	8. DOCUMENT NO. **5962-91690**

9. TITLE OF DOCUMENT	10. REVISION LETTER		11. ECP NO.
Microcircuit, Linear, 12-Bit A/D converter with microprocessor interface, Monolithic Silicon.	a. CURRENT B	b. NEW C	No registered users

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "C".
Revisions description column; add "Changes in accordance with NOR 5962-R017-95".
Revisions date column; add "95-01-17".
Revision level block; add "C".
Rev status of sheets; For sheets 1 and 6, add "C".

Sheet 6: Table I, Internal reference voltage test, V_{REF}; For device type 04, change minimum limit from "9.97 V" to "9.9 V" and change maximum limit from "10.03 V" to "10.1 V".
Revision level block; add "C".

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT	c. TYPED NAME (First, Middle Initial, Last)
DESC-ELDS	Michael A. Frye

d. TITLE	e. SIGNATURE	f. DATE SIGNED (YYMMDD)
Chief, Microelectronics Branch	Michael A. Frye	95-01-17

15a. ACTIVITY ACCOMPLISHING REVISION	b. REVISION COMPLETED (Signature)	c. DATE SIGNED (YYMMDD)
DESC-ELDS	Sandra Rooney	95-01-17

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
B	Redrawn with changes. Add device type 04. Add vendor CAGE 33256	94-09-01	M.A. Frye

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	B	B	B	B	B														
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS															
REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Sandra Rooney

CHECKED BY
Charles E. Besore

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-05-14

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 12-BIT A/D CONVERTER WITH MICROPROCESSOR INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-91690**

SHEET 1 OF 19

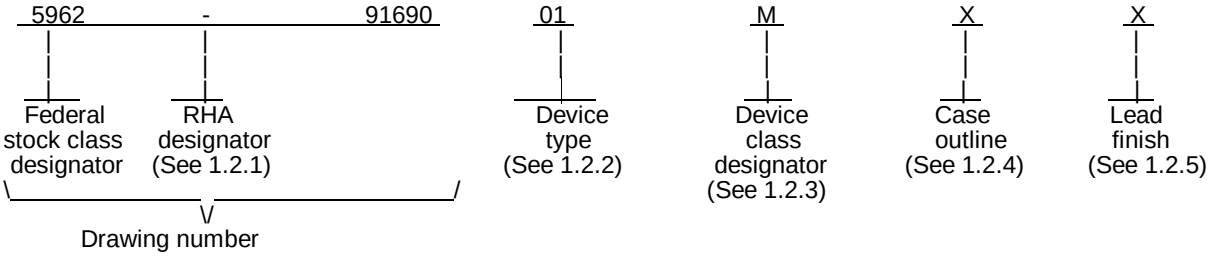
DESC FORM 193
JUL 94

5962-E396-94

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	674ZA	High performance, 12-bit A/D converter with microprocessor interface and S/H
02	674ZB	Medium performance, 12-bit A/D converter with microprocessor interface and S/H
03	674BT	12-bit A/D converter with microprocessor interface
04	674AT	12-bit A/D converter with microprocessor interface

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line
3	CQCC1-N28	28	square chip carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for classes M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

V_{CC} to digital common	0 V dc to +16.5 V dc
V_{EE} to digital common 2/	0 V dc to -16.5 V dc
V_{LOGIC} to digital common	0 V dc to +7 V dc
Analog common to digital common:	
Device types 01 and 02	-0.5 V dc to +1 V dc
Device type 03	±1 V dc
Control inputs (CE, CS, Ao, 12/8, R/C) to digital common	-0.5 V dc to V_{LOGIC} + 0.5 V dc
Analog inputs (REF IN, BIP OFF, 10 V_{IN}) to analog common	±16.5 V dc
20 V_{IN} analog input voltage to analog common	±24 V dc
$V_{REF\ OUT}$ momentary short to V_{CC}	Indefinite short to common
Power dissipation (P_D):	
Device types 01 and 02 (T_A = +25°C)	1000 mW
Device type 03 (T_A = +25°C)	470 mW
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature	-65°C to +150°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Device types 01 and 02 case X	48°C/W
Device type 03 case X	60°C/W
Device type 04 case X	50°C/W
Case 3	48°C/W

1.4 Recommended operating conditions.

Logic supply voltage (V_{LOGIC})	+4.5 V dc to +5.5 V dc
Positive supply voltage (V_{CC})	+11.4 V dc to +16.5 V dc
Negative supply voltage (V_{EE}) 2/	-11.4 V dc to -16.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-973	-	Configuration Management.
MIL-STD-1835	-	Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ V_{EE} is not required for operation of devices 01 and 02, and 04.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for classes M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block or logic diagram. The block or logic diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are described in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current from V_{LOGIC} 2/	I_{LOGIC}	Three-state outputs	1, 2, 3	01,02 04		+1.0	mA
				03		+7.0	
Power supply current from V_{CC} 2/	I_{CC}		1, 2, 3	01,02 04		+9.0	
				03		+7.0	
Power supply current from V_{EE}	I_{EE}		1, 2, 3	03	-14		
Resolution			1	All	12		Bits
Integral linearity error	ILE	Unipolar 10 V span Bipolar 20 V span	2, 3	All	-0.5	+0.5	LSB
				All	-1.0	+1.0	
Differential linearity error (minimum resolution for which no missing codes are guaranteed)	DLE		1, 2, 3	All	12		Bits
Unipolar offset voltage error	V_{IO}	10 V span	1	All	-2.0	+2.0	LSB
Unipolar offset voltage ddrift	$\frac{\Delta V_{IO}}{\Delta T}$	10 V span Using internal reference	2, 3	All	-1.0	+1.0	
Bipolar zero offset error	B_Z	20 V span	1	01,02 04	-4.0	+4.0	
				03	-3.0	+3.0	
Bipolar zero offset drift	$\frac{\Delta B_Z}{\Delta T}$	20 V span Using internal reference	2, 3	02,03 04	-2.0	+2.0	
				01	-1.0	+1.0	
Gain error	A_E	Bipolar 20 V span 50Ω resistor from REF OUT to REF IN	1	01,02 04			%FSR
				03			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Gain error drift	$\frac{\Delta A_E}{\Delta T}$	Bipolar 20V span Using internal reference	2, 3	01		12.5	ppm/°C
				02,04		25.0	
				03		17.5	
Power supply sensitivity to V_{CC} 3/ 4/	+PSS1		1, 2, 3	All	-1.0	+1.0	LSB
Power supply sensitivity to V_{LOGIC} 3/ 5/	+PSS2		1, 2, 3	All	-0.5	+0.5	
Power supply sensitivity to V_{EE} 3/ 6/	-PSS3		1, 2, 3	03	-1.0	+1.0	
Input impedence 2/	Z_{IN}	10 V span	1, 2, 3	01,02 04	3.75	6.25	kΩ
				03	3.0	7.0	
		20 V span	1, 2, 3	01,02 04	15	25	
				03	6	14	
Internal reference voltage 7	V_{REF}	I_{REFOUT} = 2 mA	1, 2, 3	01,02 04	9.97	10.03	V
				03	9.9	10.1	
Logic input high voltage (CE, $\overline{CS}$, 12/8, R/$\overline{C}$, A_0) 2/ 8/	V_{IH}	Logic "1"	1, 2, 3	All	+2.0	+5.5	V
Logic input low voltage (CE, $\overline{CS}$, 12/8, R/$\overline{C}$, A_0) 2/ 8/	V_{IL}	Logic "0"	1, 2, 3	All	-0.5	+0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logic input current 2/	$I_{IN(LOG)}$	0 to +5.5 V input	1, 2, 3	01,02		+1.0	µA
				04	-20	+20	
		0 to + 5.0 V input		03	-10	+10	
Logic low output voltage 2/ (DB11-DB0)	V_{OL}	Logic "0" I_{sink} = 1.6 mA	1, 2, 3	All		+0.4	V
Logic high output voltage 2/ (DB11-DB0)	V_{OH}	Logic "1" I_{source} = 500 µA	1, 2, 3	All	+2.4		V
Three-state output leakage current	I_Z	High-Z state (DB11 - DB0 only) $V_{applied}$ = 5.0 V	1, 2, 3	01,02	-5.0	+5.0	µA
				03	-10	+10	
				04	-20	+20	
Functional tests 2/		See section 4.4.1b	7, 8	All			
Low R/$\overline{C}$ pulse width 9/	t_{HRL}	See figure 4	9, 10, 11	All	50		ns
STS delay from R/$\overline{C}$	t_{DS}			01,02 04		200	
				03		225	
Data valid after R/$\overline{C}$ low 11/	t_{HDR}			All	25		
STS delay after data valid	t_{HS}			01,02 04	300	1000	
				03	30	600	
High R/$\overline{C}$ pulse width 9/	t_{HRH}			All	150		
Data access time 12/	t_{DDR}					150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
STS delay from CE 10/	t_{DSC}	See figure 5	1, 2, 3	01,02		200	ns
				03		225	
CE pulse width 9/	t_{HEC}			All	50		
$\overline{CS}$ to CE setup	t_{SSC}				50		
Conversion time 13/	t_C	8-bit cycle, see figure 5	9, 10, 11	All	6	10	µs
		12-bit cycle, see figure 5			9	15	
$\overline{CS}$ low during CE	tHSC	See figure 5	9, 10, 11	All	50		
R/$\overline{C}$ to CE setup	t_{SRC}				50		
R/$\overline{C}$ low during CE high	t_{HRC}				50		
A_0 to CE setup	t_{SAC}				0		
A_0 valid during CE high	t_{HAC}				50		
Access time (from CE) 12/	t_{DD}	See figure 6	9, 10, 11	All		150	ns
Data valid after CE low 11/	t_{HD}			01,02 04	25		
			11	03	15		
			9, 10		25		
Output float delay 11/	t_{HL}		9, 10, 11	All		150	
$\overline{CS}$ to CE setup	t_{SSR}			All	50		
R/$\overline{C}$ to CE setup	t_{SRR}			All	0		
Sample and hold 14/ acquisition time	t_{acq}	T_A = +25°C	9	01,02 04	1.2	2.0	µs
A_0 to CE setup	t_{SAR}	See figure 6	9, 10, 11	All	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ V_{CC} = +15 V, V_{LOGIC} = +5 V, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{CS}$ valid after CE low	t_{HSR}	See figure 6	9, 10, 11	All	0		ns
R/$\overline{C}$ high after CE low	t_{HRR}			All	0		
A_0 valid after CE low	t_{HAR}			All	50		

1/ 12/$\overline{8}$ connected to V_{LOGIC}, Ao and $\overline{CS}$ at logic "0", CE at logic "1". 10 V unipolar: 50Ω registor pin 8 to pin 10, 50Ω resistor pin 12 to ground. Analog input connected to pin 13. 20 V bipolar: 50Ω resistor pin 8 to pin 12, 50 resistor pin 8 to pin 10. Analog input connected to pin 14. Unless otherwise noted, these conditions apply.

2/ Device types are tested to the conditions stated in table I, but are guaranteed to the specified limits for the following variations in the supply voltage ranges. V_{LOGIC} = +5 V to ±5%, V_{CC} = +12 V ±5% and +15V to ±10%, V_{EE} = -12 V ±5% and -15 V ±10%. (V_{EE} not required for operation of devices 01, 02, and 04). For device type 03, V_{LOGIC} = +5 V to ±10%.

3/ Maximum change in full scale calibration due to supply voltage shifts. Full scale calibration to be measured at minimum and maximum voltage settings for each individual supply.

4/ $+13.5\ V \le V_{CC} \le +16.5\ V$, V_{LOGIC} = 5 V, V_{EE} = -15 V and $+11.4\ V \le V_{CC} \le +12.6\ V$, V_{LOGIC} = 5 V, V_{EE} = -12 V. (V_{EE} not required for operation of devices 01, 02 and 04).

5/ $4.5\ V \le V_{LOGIC} \le 5.5\ V$, V_{CC} = 15V, V_{EE} = -15V. (V_{EE} not required for operation of devices 01, 02, and 04).

6/ $-16.5\ V \le V_{EE} \le -13.5\ V$, V_{LOGIC} = 5 V, V_{CC} = +15 V and $-12.6\ V \le V_{EE} \le -11.4\ V$, V_{LOGIC} = 5 V, V_{CC} = +12 V.

7/ Reference should be buffered for operation on ±12 V supplies. External load should not change during conversion.

8/ For devices types 01, 02, and 04, 12/$\overline{8}$ is not TTL compatible, must be hard-wired to V_{LOGIC} or digital common.

9/ Pulse width is measured at the Schottky TTL input logic threshold voltage (1.3 V).

10/ t_{DS} and t_{DSC} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V) to when the STS output reaches 2.4 V. No external loading is applied to STS.

11/ t_{HDR}, t_{HD}, and t_{HL} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output voltage has moved 0.5 V in the direction of its final high impedance output voltage. Each individual data bit (DBO - DB11) is measured for both logic one to "high Z" and logic zero to "high Z" transitions. External loading is as shown on figure 7.

12/ t_{DDR} and t_{DD} are measured from the point when the input signal crosses the Schottky TTL logic threshold voltage (1.3 V), to when the output crosses either 2.4 V for a logic one, or 0.4 V for a logic zero. Each individual data bit (DBO - DB11) is measured for both "high Z" to logic zero transitions. External loading is as shown on figure 8.

13/ t_C is measured as the time from when the STS line crosses the 1.0 V level, going positive, to when it crosses the 1.0 V level going negative. No external loading is applied to STS.

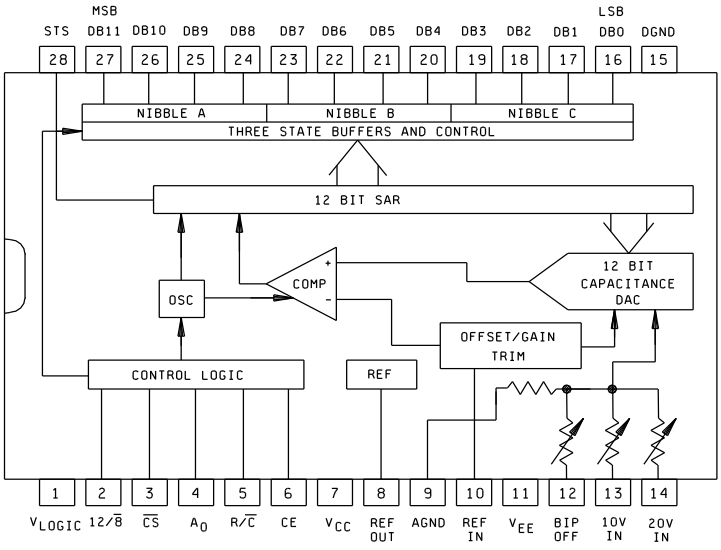
14/ Guaranteed by design.

Device types	01 and 02	03 and 04
Case outlines	X and 3	X
Terminal number	Terminal symbol	
1	+5 V supply (V_{LOGIC})	+5 V supply (V_{LOGIC})
2	Data mode select (12/$\overline{8}$)	Data mode select (12/$\overline{8}$)
3	Chip select ($\overline{CS}$)	Chip select ($\overline{CS}$)
4	Byte address/short cycle (A_O)	Byte address/short cycle (A_O)
5	Read/convert (R/$\overline{C}$)	Read/convert (R/$\overline{C}$)
6	Chip enable (CE)	Chip enable (CE)
7	+12 V/+15 V supply (V_{CC})	+12 V/+15 V supply (V_{CC})
8	+10 V reference (REF OUT)	+10 V reference (REF OUT)
9	Analog common (AGND)	Analog common (AGND)
10	Reference input (REF IN)	Reference input (REF IN)
11	-12 V/-15 V supply (V_{EE})	-12 V/-15 V supply (V_{EE})
12	Bipolar offset (BIP OFF)	Bipolar offset (BIP OFF)
13	10 V span input (10 V_{IN})	10 V span input (10 V_{IN})
14	20 V span input (20 V_{IN})	20 V span input (20 V_{IN})
15	Digital common (DGND)	Digital common (DGND)
16	DB0 (LSB)	DB0 (LSB)
17	DB1	DB1
18	DB2	DB2
19	DB3	DB3
20	DB4	DB4
21	DB5	DB5
22	DB6	DB6
23	DB7	DB7
24	DB8	DB8
25	DB9	DB9
26	DB10	DB10
27	DB11 (MSB)	DB11 (MSB)
28	Status (STS)	Status (STS)

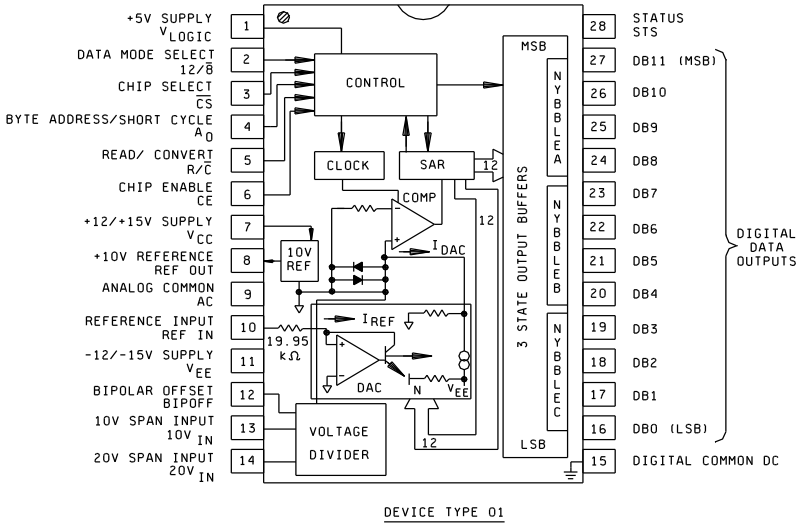
FIGURE 1. Terminal connections.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-bit conversion
1	0	0	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit parallel output
1	0	1	0	0	Enable 8 most significant bits
1	0	1	0	1	Enable 4 LSBs + 4 trailing zeros

FIGURE 2. Truth table.

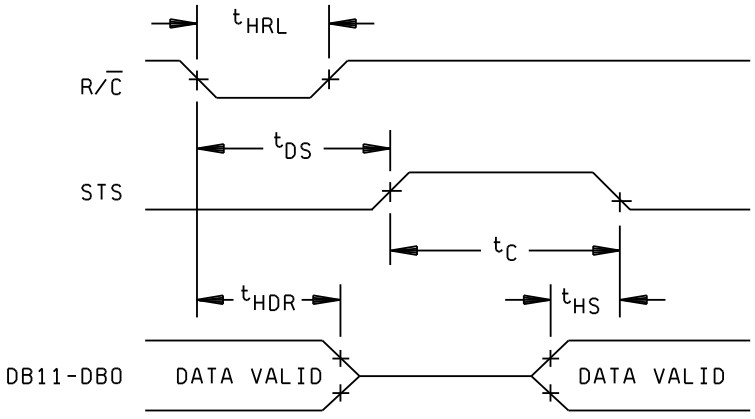


Device types 01, 02, and 04

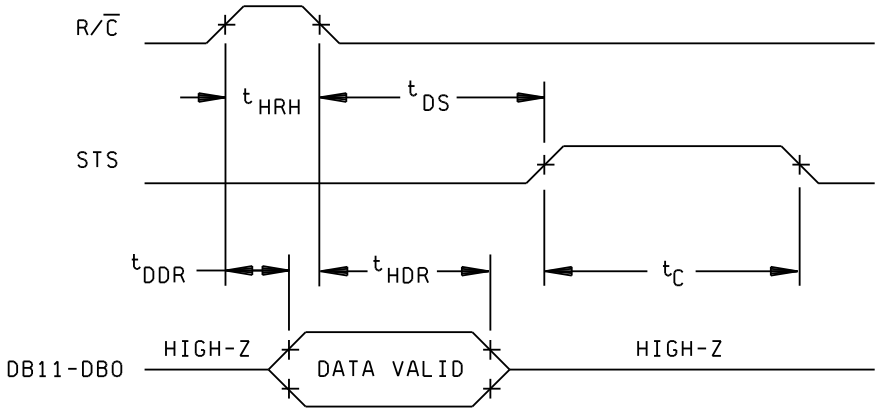


DEVICE TYPE 01

FIGURE 3. Block diagram.



LOW PULSE FOR R/$\overline{C}$-OUTPUTS ENABLED
AFTER CONVERSION



HIGH PULSE FOR R/$\overline{C}$-OUTPUTS ENABLED WHILE
R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

FIGURE 4. High/low pulse for R/C.

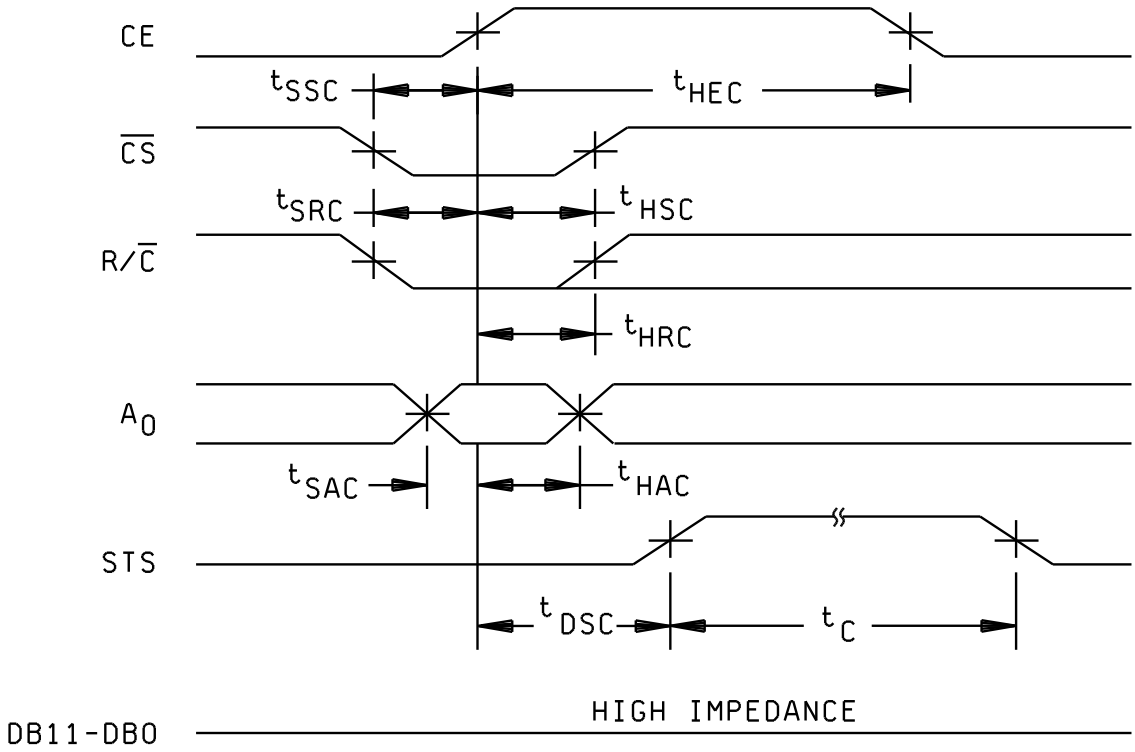


FIGURE 5. Convert start diagram.

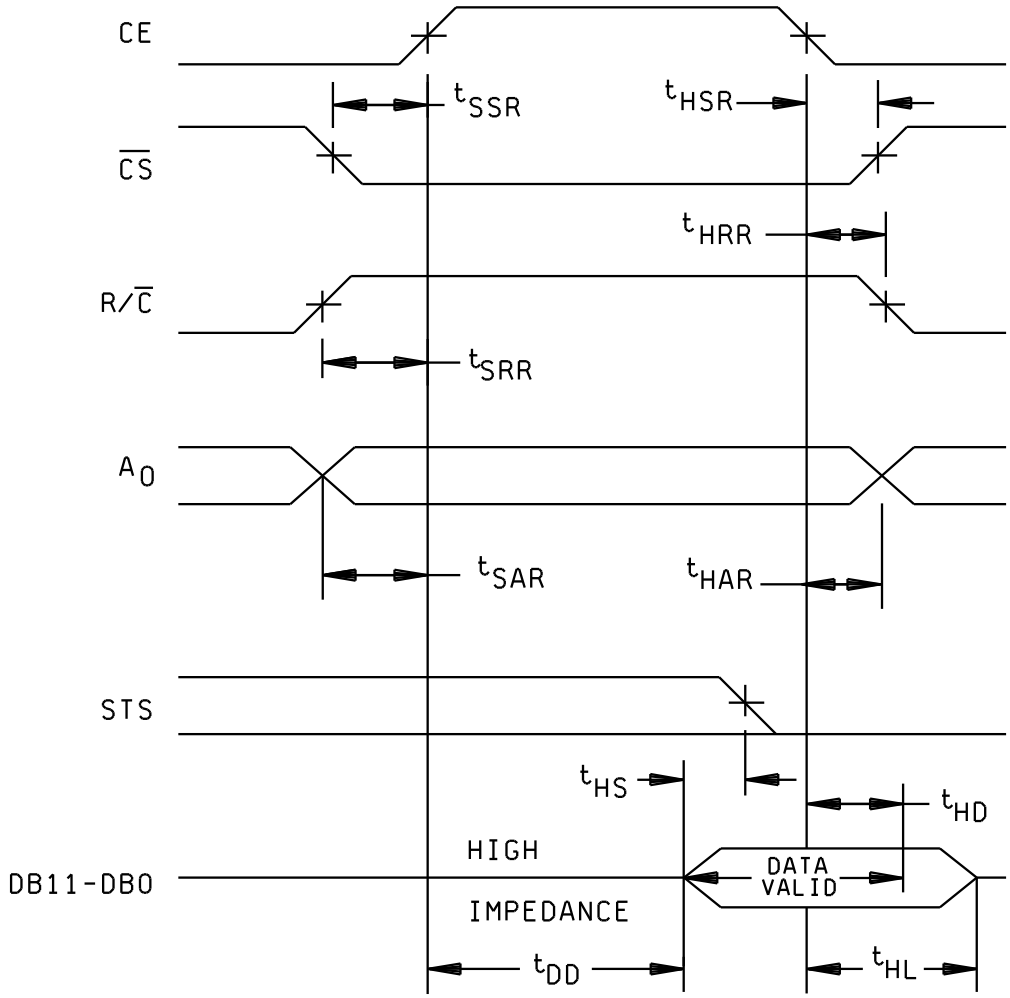


FIGURE 6. Read cycle timing.

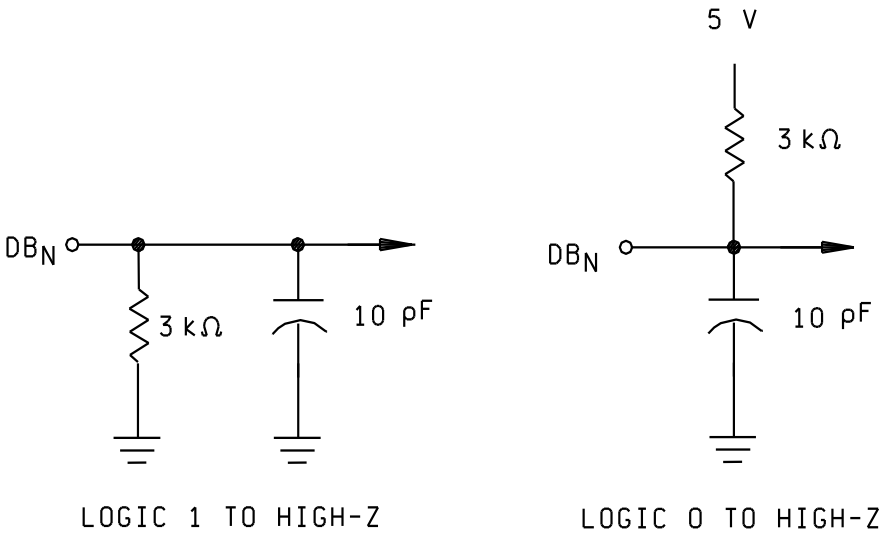


FIGURE 7. Load circuit for output float delay test.

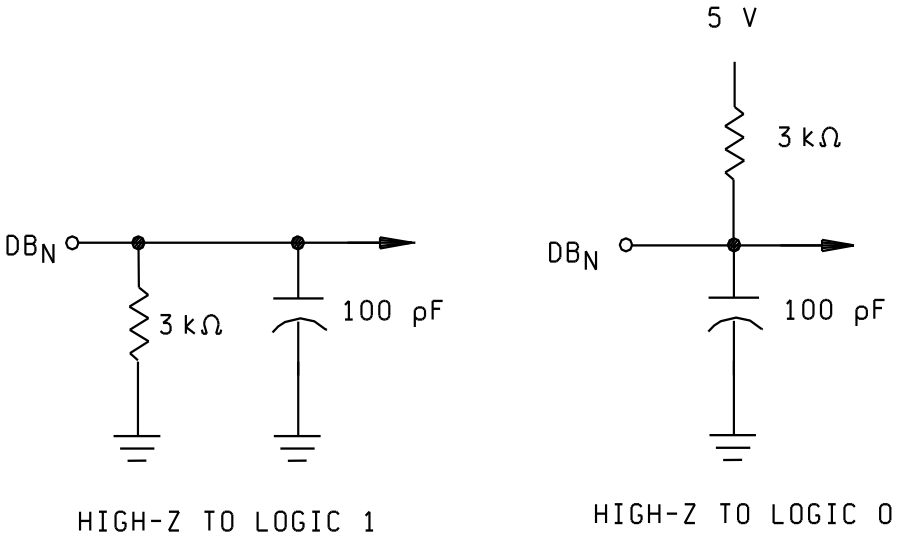


FIGURE 8. Load circuit for access time test.

3.8 Notification of change for device class M. For device class M, DESC, DESC's agent, and the change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M. Device classes M devices covered by this drawing shall be in microcuiruit group number 93 (see MIL-M-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-M-38535. The burn-in test shall be submitted to DESC-ECS with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in acccordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3, 1/	1,2,3 1/	1,2,3, 2/
Group A test requirements (see 4.4)	1,2,3,7 8,9,10,11 2/	1,2,3,7, 8,9,10,11 2/	1,2,3,7, 8,9,10,11 2/
Group C end-point electrical parameters (see 4.4)	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shallbe as specified in table II herein.

4.4.2.1 Additional criteria for device classes M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device class Q shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38535, appendix A, for RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure, to the subgroups specified in table II herein..

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the threemajor microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXXX(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXXX(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXXX(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECS and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-09-01

Approved sources of supply for SMD 5962-91690 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standard microcircuit drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification PIN
5962-9169001MXX 5962-9169001M3X	0H9K9 0H9K9	HADC674ZAMD/883 HADC674ZAMC/883	M38510/14005BXX ---
5962-9169002MXX 5962-9169002M3X	0H9K9 0H9K9	HADC674ZBMD/883 HADC674ZBMC/883	M38510/14006BXX ---
5962-9169003MXX 5962-9169003M3X	24355 24355	AD674BTD/883B AD674BTE/883B	M38510/14006BXX ---
5962-9169004MXX	33256	SP674AT/B	M38510/14006BXX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0H9K9	Signal Processing Technologies, Incorporated 1510 Quail Lake Loop Colorado Springs, CO 80906
24355	Analog Devices 804 Woburn Street Wilmington, MA 01887
33256	Sipex Corporation 22 Linnell Circle Billerica, MA 01821-3985