ANALOG DEVICES

Precision Sample-and-Hold with 16-Channel Multiplexer

AD1362/883B

1.1 Scope.

This specification covers the detail requirements for a hybrid multiplexer and track and hold amplifier combination.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD1362SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-32E

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{IN}, Signal	$\pm V_S$
Positive Supply Voltage	+17V
Negative Supply Voltage	−17V
Logic Supply Voltage (V_{DD})	+5.5V
Signal Inputs	$\pm V_S$
Input Fault Current	±20mA
Logic Inputs	$+V_{DD}$
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{jc} = 7°C/W
θ_{ja} = 40°C/W

REV. A

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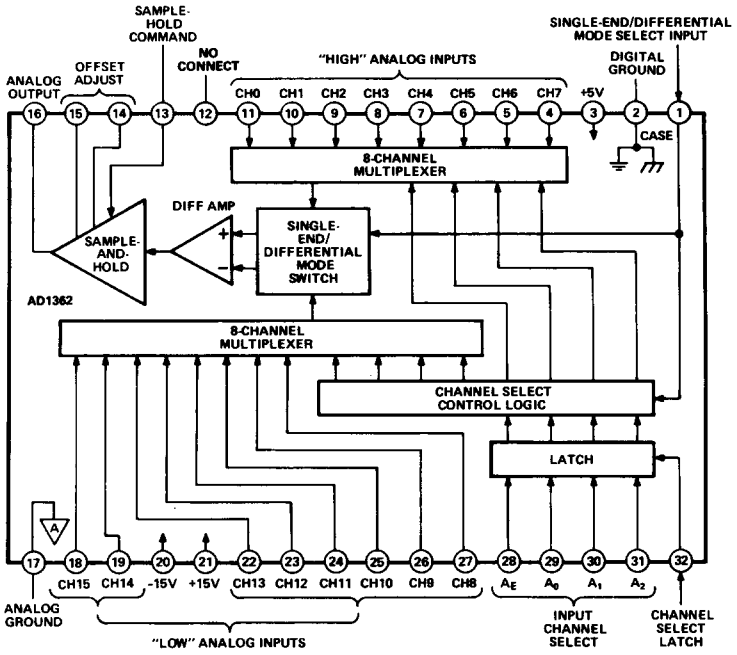
AD1362/883B – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Positive Supply Current	I_{CC}	–1	23			30	No Load, Grounded	mA max
Negative Supply Current	I_{EE}	–1	23			30	Inputs Track Mode	mA max
Logic Supply Current	I_{LOGIC}	–1	23			40		mA max
Output Offset Voltage	V_{OS}	–1	4.0	4.0			All Inputs Shorted to Analog Common Track Mode	± mV max
Channel-to-Channel Offset	$V_{OS\text{-}CC}$	–1	2.5			2.5		± mV max
Common-Mode Rejection Ratio	CMRR	–1	70			70	20V pk-pk max @ 1kHz on Diff Inputs	dB min
Input Bias Current	I_B	–1	1			50		± nA max
Gain Error, FS	A_E	–1	0.02	0.02				± % FSR
Crosstalk, CH-CH	V_{CT}	–1	2.0			2.0	± 10V max on Adjacent Channels	– mV max
Droop Rate	V_{DRP}	–1	2.0			2.0		mV/ms max
T/H Offset Pedestal	SH_{OS}	–1	15			15	V_{IN} = 0V	± mV max
Linearity Error	LE	–1	0.005				± 10V Input max	% FSR max
Number of Inputs	CH_N	–1	16	16			Electrically Selectable Diff/SE	
Offset TC	TCV_{OS}	–1	1.5		1.5		V_{IN} = 0V	± ppm/°C max
Gain TC	TCA_E	–1	2.0		2.0		$\pm V_{IN}$ = ± 10V	± ppm/°C max
Input Fault Current	I_F	–1	20				$\pm V_{IN}$ = ± 15V	mA max
Noise Error	EN	–1	0.5				0.1 to 10MHz	mV pk-pk max
Noise Error Over Temperature	EN	–1	1				0.1 to 10MHz –55°C to +125°C	mV pk-pk max
Aperture Delay	t_{AD}	–1	100				50ns typ	ns max
Aperture Uncertainty	t_{AU}	–1	500				100ps typ	ps max
Acquisition Time	t_{ACQ}	–1	18				20V Step to 0.01% (10µs typ)	µs max
Feedthrough in Hold Mode	FT	–1	–70				20V pk-pk @ 1kHz	dB max
Digital Inputs (28-31)	V_{LOGIC}	–1	1				TTL Compatible	LSTTL Loads max
Digital Input (Pin 1)	D_{INCH}	–1	3				CMOS Compatible	TTL Loads max
T/H Input (Pin 13)	D_{INTH}	–1	2				TTL Compatible	TTL Load max
Latch Input (Pin 32)	D_{INLCH}	–1	8				TTL Compatible	LSTTL Loads max
Power Dissipation	P_D	–1	800				No Load	mW max

NOTE.
[1]T_A = +25°C and V_{CC} = ± 15V, V_{DD} = +5V unless otherwise noted.

Table 1.

3.2.1 Functional Block Diagram and Terminal Assignments.

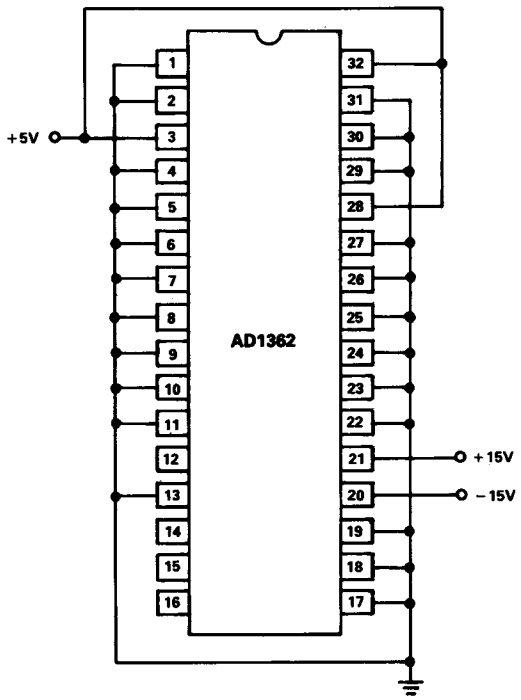


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



5.0 Input Range.

The analog input range is ±10V FS as specified in Table 1. When ±12V supplies are used, the linear input range must be limited to ±5V FS max. Unused channels must be terminated at analog common or thru a resistive load to a stable voltage.

5.1 Offset Adjust.

The offset error is adjustable to zero using the circuit shown in Figure 1. The offset voltage of the AD1362 may be adjusted at either the Analog Input or ADC sections. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 1 is recommended. Under normal conditions all calibration is performed at the ADC section.

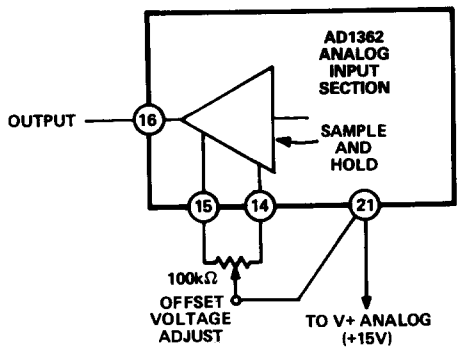


Figure 1. Analog Input Section Offset Voltage Adjustment

5.2 Digital Control Signals.

Single-Ended/Differential Mode Control

The AD1362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to Pin 1 of the Analog Input Section:

"0": Single-Ended (SE) (16 channels)
"1": Differential (DIFF) (8 channels)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels. It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table 2 is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Pins 28-31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS			ON CHANNEL (Pin Number)		
				Differential	
A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0 (11)	None	
0	0	1	1 (10)	None	
0	1	0	2 (9)	None	
0	1	1	3 (8)	None	
1	0	0	4 (7)	None	
1	0	1	5 (6)	None	
1	1	0	6 (5)	None	
1	1	1	7 (4)	None	
0	0	0	8 (27)	0 (11)	0 (27)
0	0	1	9 (26)	1 (10)	1 (26)
0	1	0	10 (25)	2 (9)	2 (25)
0	1	1	11 (24)	3 (8)	3 (24)
1	0	0	12 (23)	4 (7)	5 (23)
1	0	1	13 (22)	5 (6)	5 (22)
1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	15 (18)	7 (4)	7 (18)

Table 2. Input Channel Addressing Truth Table

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD1362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (Pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered). This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Pin 13) is normally connected to the Status output (Pin 20) from an analog-to-digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Pin 17) and Digital Ground (Pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD1362 as possible. The lid is connected to Analog Ground to provide electrostatic shielding. If the grounds are not tied common on the same card with the AD1362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes. This will protect the AD1362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the

key grounding card should be removed from the overall system. The device will operate properly with as much as ±20mV between grounds, however this difference will be reflected directly as an input offset voltage.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Hold Capacitor

An internal 1500pF hold capacitor is included within the AD1362. Applications upgrading from the AD362, in which Pin 12 is the connection for an external hold capacitor, do not require removal of this capacitor since Pin 12 is not connected internally in the AD1362.

5.3 System Timing & Operation.

Interfacing to Popular Analog-to-Digital Converters

The AD1362 has been designed to interface directly to most analog-to-digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

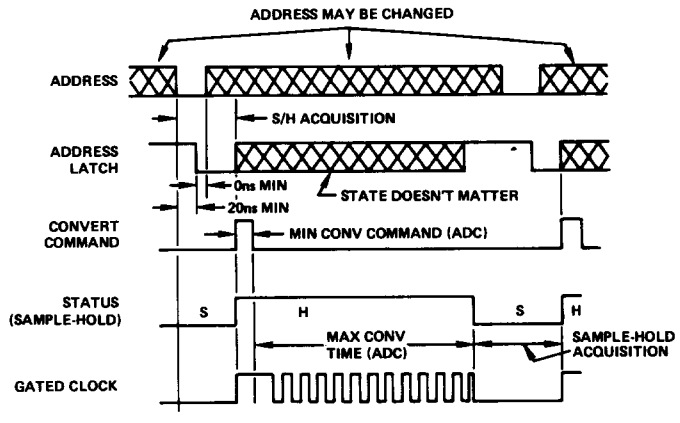


Figure 2. DAS Timing Diagram

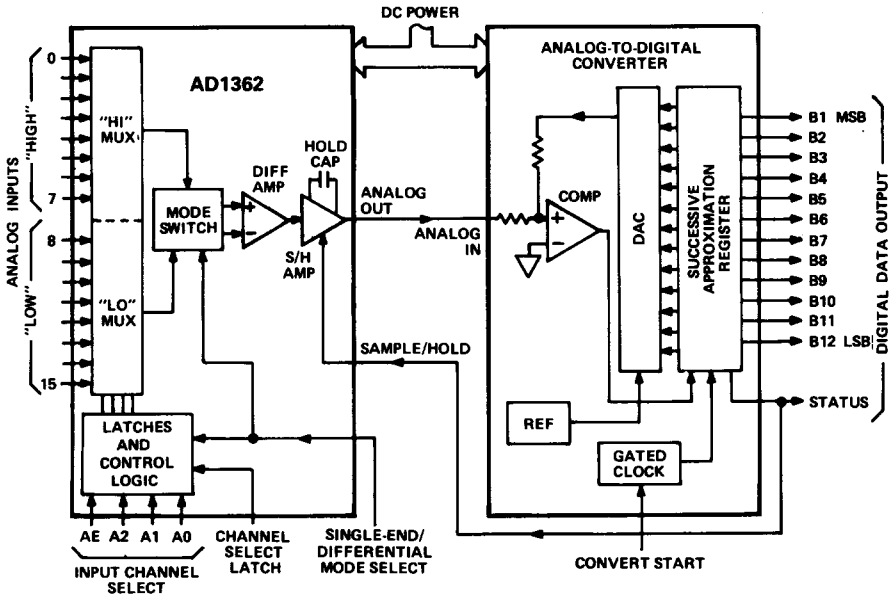


Figure 3. AD1362 with ADC as a Complete Data Acquisition

Figure 2 is a timing diagram for the AD1362 connected as shown in Figure 3 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12-bit type such as the AD573.

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data), the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.