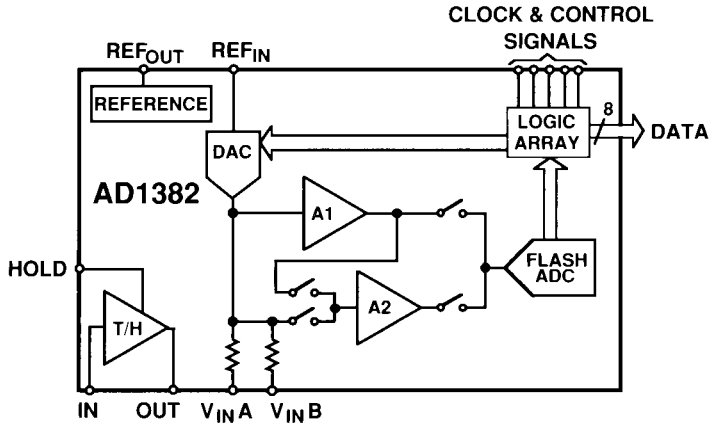
16-Bit 500 kHz Sampling ADC

AD1382

PRODUCT FEATURES
Single Package
16-Bit Resolution
500 kHz Sampling Rate
SNR 90 dB @ 100 kHz (min)
THD −88 dB @ 100 kHz (min)
0.0015% FSR INL (typ)
±5, ±10 V Bipolar Input
Zero Offset Autocalibration

APPLICATIONS
Medical Imaging
CAT
Magnetic Resonance
Vibration Analysis
Parametric Measurement Unit (ATE)
Waveform/Transient Recorders
Analytical Instruments
Sonar
Radar

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1382 is a complete 500 kHz, 16-bit, sampling analog-to-digital converter contained in a single package. This high resolution, high speed converter offers outstanding noise and distortion performance along with excellent INL and DNL performance, all in a single dual-in-line package.

The AD1382 guarantees outstanding noise and distortion performance for both ±5 V and ±10 V input ranges. The AD1382 architecture includes a low noise and low distortion track/hold with a three-pass digitally corrected subranging ADC. Precision thin film resistors and a new proprietary DAC provide for outstanding dynamic and static performance. Output data is multiplexed over an eight-bit CMOS/TTL compatible data bus.

The AD1382 uses four power supplies, ±5 V and ±15 V, and an external 10 MHz clock. Power dissipation is nominally 2.8 W. Two user selectable bipolar input ranges, ±5 V and ±10 V are provided. Careful attention to grounding and a single package make it easy to design PCBs to achieve specified performance.

This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD1382-SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, V_{DD} = +5 V, V_{SS} = −5 V, 10 MHz External Clock, 5 Minute Warm-up, unless otherwise noted)

Parameter	AD1382KD Min	Typ	Max	Units
RESOLUTION	16			Bits
ANALOG INPUT				
Input Ranges		±5, ±10		V
Input Impedance	2.45	2.5	2.55	kΩ
TRANSFER CHARACTERISTICS				
(Combined ADC/Track/Hold)				
Integral Nonlinearity[1]		±0.0015		% FSR[2]
Differential Nonlinearity[1]		±0.0006	±0.0015	% FSR
Missing Codes			None	
Gain Error[3]		±0.07	±0.15	% FSR
Bipolar Zero[3]		±0.03	±0.10	% FSR
PSRR		±0.006	±0.10	% FSR/V
Noise[4]		55		μV RMS
DYNAMIC CHARACTERISTICS				
±5 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	93		dB
f = 100 kHz	90	92		dB
f = 200 kHz	88	91		dB
Peak Distortion				
f = 5 kHz	−90	−98		dB
f = 100 kHz	−88	−93		dB
f = 200 kHz	−82	−85		dB
Total Harmonic Distortion[6]				
f = 5 kHz	−90	−96		dB
f = 100 kHz	−88	−92		dB
f = 200 kHz	−82	−85		dB
DYNAMIC CHARACTERISTICS				
±10 V FSR, V_{IN} = −0.4 dB				
Sample Rate			500	kHz
Signal-to-Noise Ratio[5]				
f = 5 kHz	90	95		dB
f = 100 kHz	90	94		dB
f = 200 kHz	88	93		dB
Peak Distortion				
f = 5 kHz	−90	−98		dB
f = 100 kHz	−80	−87		dB
f = 200 kHz	−74	−81		dB
Total Harmonic Distortion[6]				
f = 5 kHz	−90	−96		dB
f = 100 kHz	−80	−87		dB
f = 200 kHz	−74	−81		dB
DIGITAL INPUTS[9]				
Input Voltage				
V_{IL}			0.8	V
V_{IH}	2.0			V
Input Current			±200	μA
Input Capacitance		2		pF
Start Command				
Setup Time, t_{SCS}	10	3		ns
Hold Time, t_{SCH}	10	0		ns
Autozero				
Setup Time, t_{AZS}	10	0		ns
Hold Time, t_{AZH}	20	6		ns
Clock				
Frequency	2.5		10	MHz
Duty Cycle	40		60	%

Parameter	AD1382KD Min	Typ	Max	Units
DIGITAL INPUTS (Continued)				
Aperture Delay[7]		7		ns
DIGITAL OUTPUTS[8, 9]				
Output Voltage				
V_{OL} @ I_{OL} = 3.2 mA		0.2	0.4	V
V_{OH} @ I_{OH} = −3.2 mA	2.4	4.5		V
Output Capacitance		10		pF
Leakage, Outputs Disabled			±200	μA
Data Valid				
Setup Time, t_{DVS}	75	150		ns
Hold Time, t_{DVH}	25	50		ns
Hold Command Time, t_H		1300		ns
Hold Command Delay, t_{HD}		6		ns
Data Strobe Pulse Width, t_{DS}		200		ns
Data Strobe Delay, t_{DSD}		1650		ns
OUTPUT CODING	Complementary Offset Binary or Complementary Twos Complement			
PERFORMANCE OVER TEMPERATURE[8, 10]				
Operating Temperature Range	0		70	°C
Specified Temperature Range	10		40	°C
Missing Codes			None	
Gain Drift		8	15	ppm/°C
Offset Drift		5	15	ppm/°C
Differential Linearity		0.3		ppm/°C
INTERNAL REFERENCE				
Voltage	9.990		10.010	V
Current	2	10		mA
POWER REQUIREMENTS				
Operating Range				
$\pm V_S$	14.25		15.75	V
$+V_{DD}$	4.75		5.25	V
$-V_{SS}$	−5.25		−4.75	V
Current Drains				
$+V_S$		50	73	mA
$-V_S$		45	65	mA
$+V_{DD}$		115	160	mA
$-V_{SS}$		160	200	mA
Power Dissipation		2.8	3.9	Watts

NOTES
[1]Integral linearity is inferred from FFT. Differential linearity is derived from histogram.
[2]FSR, full-scale range.
[3]Adjustable to zero.
[4]Noise based on small signal FFT excluding quantization noise.
[5]SNR fundamental to noise minus harmonics 2–9.
[6]THD includes harmonics 2–9 of the fundamental.
[7]Aperture delay is the time from the rising edge on the Hold Command Input to the opening of the switch in the Track/Hold.
[8]Guaranteed but not 100% production tested.
[9]Timing based on 10 MHz clock. Refer to Figures 13 and 14.
[10]Case to ambient temperature is assumed to be 30°C. The AD1382 case temperature will stabilize about 30°C above ambient while operating in free air without a heat sink. Factory calibration is done in this condition. See the application section for further information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to AGND . . . . . 18 V
$-V_S$ to AGND . . . . . −18 V
V_{DD} to PGND . . . . . 7 V
V_{SS} to PGND . . . . . −7 V
AGND to PGND . . . . . ±0.3 V
Analog Inputs . . . . . $\pm V_S$
Digital Inputs . . . . . −0.3 V to V_{DD} + 0.3 V
Output Short Circuit Duration
  Reference Output . . . . . Indefinite
  Track/Hold Output . . . . . 1 sec
  Digital Outputs . . . . . 1 sec for Any One Output
Ambient Temperature (Operating) . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD1382 PIN CONNECTIONS

The AD1382 is housed in a 48-pin bottom-brazed ceramic bathtub package. The pinout is as follows:

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK IN	48	V_{DD2} (+5 V POWER)
2	POWER GROUND	47	POWER GROUND
3	B1/B9 MSB	46	V_{SS2} (−5 V POWER)
4	B2/B10	45	AUTOZERO
5	B3/B11	44	B1 SELECT
6	B4/B12	43	POWER GROUND
7	B5/B13	42	POWER GROUND
8	B6/B14	41	DNC
9	B7/B15	40	GAIN ADJUST
10	B8/B16 LSB	39	+10 V REFERENCE OUT
11	V_{DD1} (+5 V SIGNAL)	38	$-V_{S1}$ (−15 V)
12	POWER GROUND	37	SIGNAL GROUND
13	V_{SS1} (−5 V SIGNAL)	36	$+V_{S1}$ (+15 V)
14	SIGNAL GROUND	35	SIGNAL GROUND
15	DATA STROBE	34	DNC
16	HI/LO BYTE SELECT	33	DNC
17	OE DATA ENABLE	32	+10 V REFERENCE IN
18	START CONVERT	31	V_{IN} B
19	HOLD COMMAND OUT	30	V_{IN} A
20	SIGNAL GROUND	29	OFFSET ADJUST
21	$+V_{S2}$ (+15 V)	28	DNC
22	HOLD COMMAND IN	27	TRACK/HOLD OUTPUT
23	$-V_{S2}$ (−15 V)	26	SIGNAL GROUND
24	POWER GROUND	25	TRACK/HOLD INPUT

DNC = DO NOT CONNECT

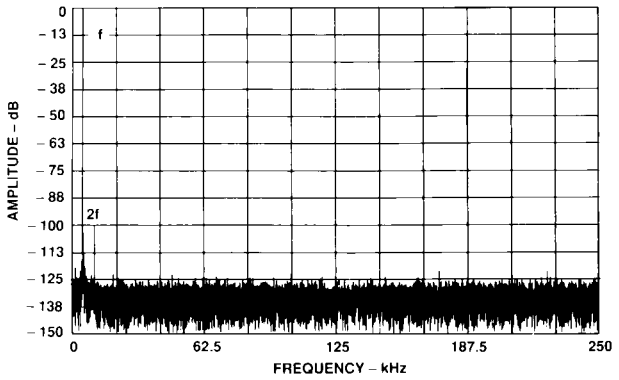
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

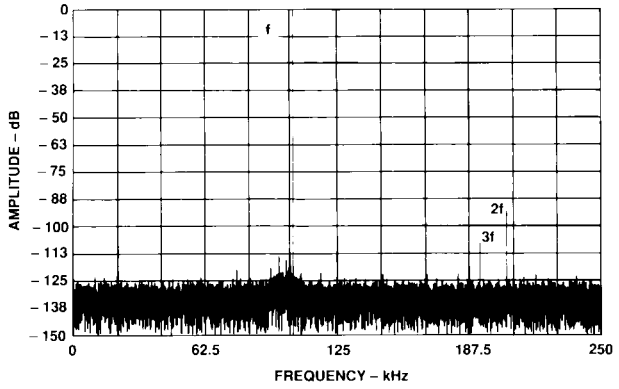
Model	Temperature Range	Package Option*
AD1382KD	10°C to 40°C Ambient (40°C to 70°C Case)	DH-48A

*DH-48A = Hermetic Ceramic DIP. For outline information see Package Information section.



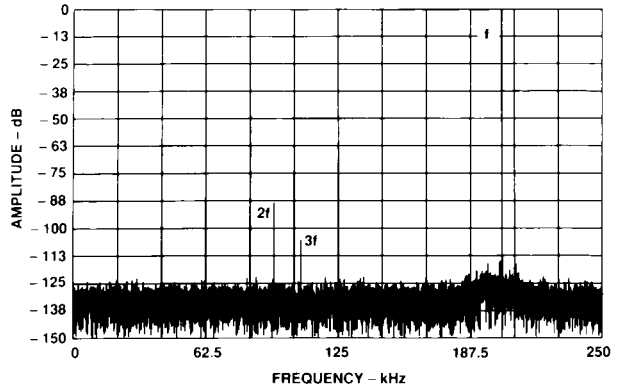
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	5.279410kHz
INPUT AMPLITUDE	–0.3dB
2nd HARMONIC	–99.8dB
3rd HARMONIC	–116.9dB
4th HARMONIC	–117.1dB
SNR	93.1dB
THD	–99.2dB

Figure 1. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



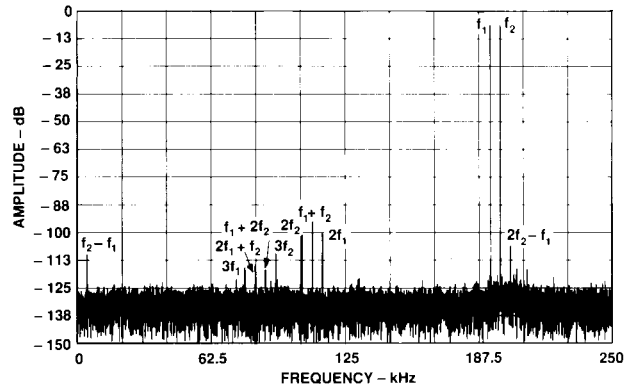
SAMPLE RATE	500.000kHz
INPUT FREQUENCY	102.50855kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–93.0dB
3rd HARMONIC	–107.4dB
4th HARMONIC	–115.6dB
SNR	92.5dB
THD	–92.7dB

Figure 2. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



SAMPLE RATE	500.000kHz
INPUT FREQUENCY	202.54516kHz
INPUT AMPLITUDE	–0.4dB
2nd HARMONIC	–88.2dB
3rd HARMONIC	–104.7dB
4th HARMONIC	–112.4dB
SNR	91.5dB
THD	–88.0dB

Figure 3. Full-Scale Sine Wave Power Spectral Density, ±5 V Scale, 16384-Point FFT



f_1 FREQUENCY	192.77954kHz		
f_1 AMPLITUDE	–6.1dB		
f_2 FREQUENCY	197.54028kHz		
f_2 AMPLITUDE	–6.0dB		
$f_2 - f_1$	–110.2dB	$f_2 + 2f_1$	–116.0dB
$f_2 + f_1$	–94.9dB	$2f_1$	–100.8dB
$2f_2 - f_1$	–106.0dB	$2f_2$	–101.2dB
$2f_1 - f_2$	–128.0dB	$3f_1$	–117.2dB
$f_1 + 2f_2$	–116.8dB	$3f_2$	–109.6dB

Figure 4. Intermodulation Performance, ±5 V Scale, 16384-Point FFT, 500 kHz Sample Rate

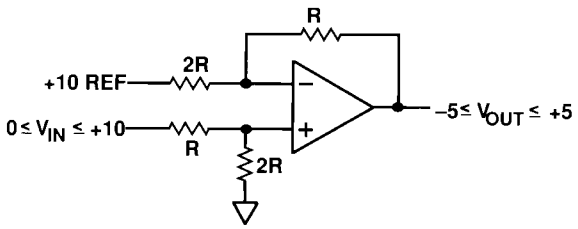


Figure 19. Unipolar-to-Bipolar Conversion (Low Input Impedance)

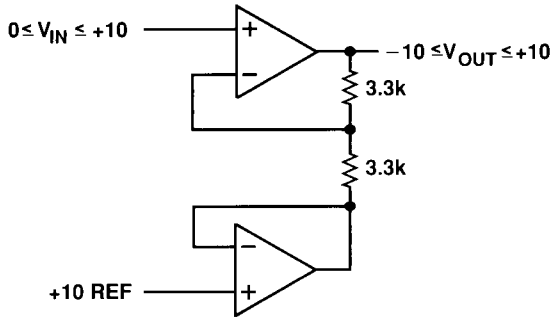


Figure 20. High Input Impedance Unipolar-to-Bipolar Conversion Circuit

Sample Board Layout

Figures 22–27 show the layout of an evaluation board for the AD1382. This layout incorporates the grounding, power distribution, and interface concepts described in previous sections. This 4-layer layout makes extensive use of ground and power planes and provides optimal AD1382 performance.

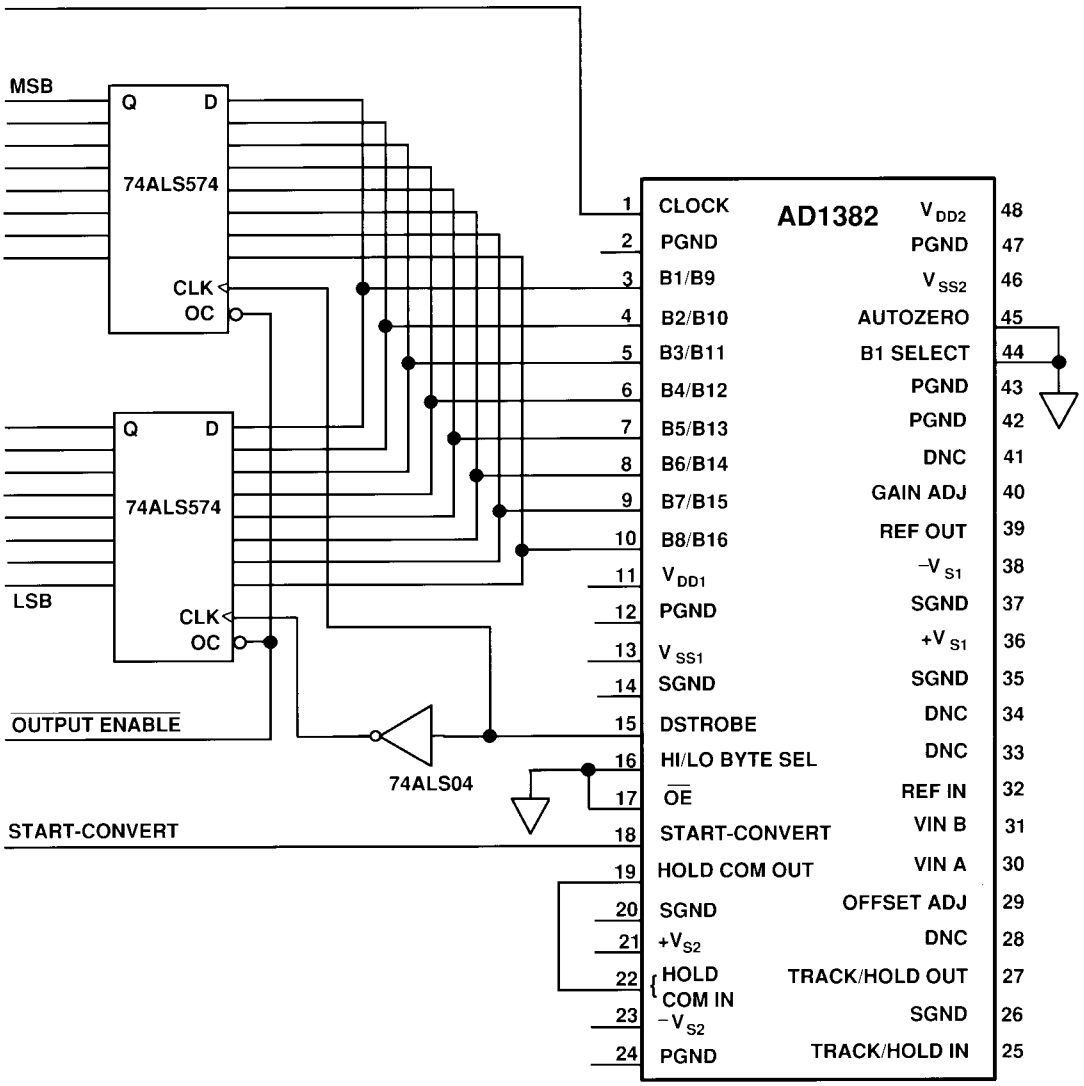


Figure 21. Basic AD1382 Digital Interface (16-Bit 2s Complement Data, Autozero Not Used)

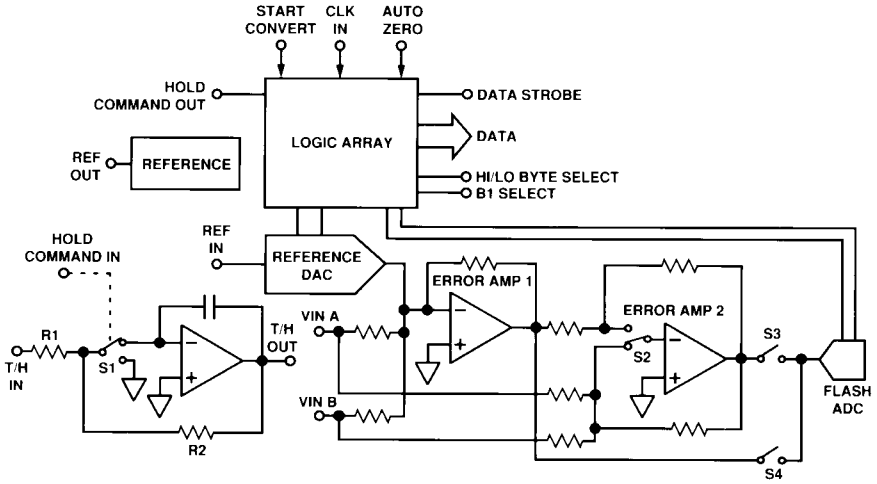


Figure 9. AD1382 Functional Block Diagram

THEORY OF OPERATION

The AD1382 performs conversions using a three-pass subranging technique. This proven circuit concept, implemented with state of the art components, allows the ADC, track-hold, and a low noise reference to fit into a single hermetic package, simplifying the task of board design. The T/H and ADC portions of the AD1382 are distinct circuits with inputs and outputs available on separate pins. This functional division allows greatest application flexibility. The AD1382's major functional blocks are shown in Figure 9.

The T/H uses a low noise high performance hybrid amplifier and high speed analog switches to achieve precision performance. It operates as an inverting amplifier during Track mode. Summing junction switch S1 disconnects the analog input to place the circuit into Hold mode; the amplifier's output stays constant because the dc path to its inverting input is broken. S1 also grounds the junction of R1 and R2 to minimize signal feedthrough. Pedestal is independent of the analog input level because all switching is done near ground. This ensures very low nonlinearity and distortion.

A precision reference DAC and an 8-bit flash ADC form the heart of the AD1382's subranging design. High speed amplifiers combine the analog input and DAC output to produce the voltages encoded by the flash ADC during each pass. A logic array provides all necessary timing, control, and computation.

The first rising clock edge after Start Convert goes high begins the conversion (provided the previous conversion is complete). The Hold Command goes high and switches the T/H into hold. The held signal from the T/H goes through S2, S3, and Error Amp 2 to the flash ADC. During this pass Error Amp 2 actually attenuates the ADC input to keep the voltage within the flash ADC's input range. The flash ADC is strobed after a 100 ns settling period. The 8-bit result is saved in the logic array and is routed to the MSBs of the reference DAC.

Error Amp 1 amplifies the difference between the reference DAC output and the held input signal during the second pass. S4 routes this error signal to the flash ADC, which is strobed a second time after Error Amp 1 has settled. The new 8-bit result is used to correct the previous result, increasing the accuracy of this intermediate answer to 13-bit precision. Following this the reference DAC is updated.

Both error amplifiers are active during the third pass. S2 is switched, allowing Error Amp 2 to amplify Error Amp 1's output. S3 now brings Error Amp 2's output to the flash ADC. The flash ADC is strobed a final time after the DAC and both error amplifiers have settled. The logic array combines the data from the third flash conversion with the earlier 13-bit word to produce the final 16-bit result. The T/H is returned to track mode, and Error Amp 2 is reconnected as an attenuator 50 ns after the completion of the third flash conversion to prepare for the next conversion.

The output data are placed on the data bus in two 8-bit bytes to be read by the host system. The Data Strobe output synchronizes the data transfer by providing a rising edge for the first byte and a falling edge for the second byte. The Hi/Lo Byte Select input allows the user to choose which data byte is presented first. B1 Select sets the polarity of the MSB to provide either twos complement or offset binary data.

CONNECTION AND OPERATION OF THE AD1382

Analog Input

The analog input should be connected to the Track/Hold Input (Pin 25). Two pin programmable operating ranges are available: ±5 V and ±10 V. Connect the Track/Hold Output to V_{IN} A and/or V_{IN} B as follows:

Desired Scale	Connect V_{IN} A to	Connect V_{IN} B to
±5 V	Track/Hold Output	Track/Hold Output
±10 V	Track/Hold Output	Analog Signal GND

Harmonic distortion is lower when using the ±5 V range, while noise is lower when using the ±10 V range.

The AD1382's noise and distortion performance exceed the capability of most signal sources. Maintaining this performance at the system level requires attention to every detail of grounding, bypassing, and signal sources. A low impedance high bandwidth signal source is essential to achieve low distortion. Few monolithic amplifiers exist which can maintain signal fidelity at levels comparable with the AD1382's performance, even at low frequencies. High bandwidth means increased noise and decreased SNR. See *Testing the AD1382* for techniques of achieving the lowest possible noise and distortion.

Grounding

Proper treatment of the AD1382's power and ground connections is vital to achieve the best possible system performance. The ideal grounding arrangement is to have a single, solid, low impedance ground plane beneath the device to which all ground and supply bypassing connections are made. This results in the lowest possible ground noise and minimizes undesired interactions between the sensitive circuits inside the AD1382. Aperture uncertainty, for example, can be degraded by noise in Power Ground because the Hold Command signals are referenced to this ground. The digital interface between the AD1382 and the rest of the user's system is also critical. The following discussion will help in obtaining optimal performance. These guidelines are general and apply equally well to other high performance analog and digital circuits.

The AD1382 must connect to three other parts of the system: the input signal(s), the power supplies, and the digital interface. The system designer must determine the magnitude and type of ground currents and whether they are constant or dynamic. A system block diagram is a valuable aid to understanding how grounds should be connected for good performance. Figure 10 shows recommended ground connections for the AD1382 in a typical system.

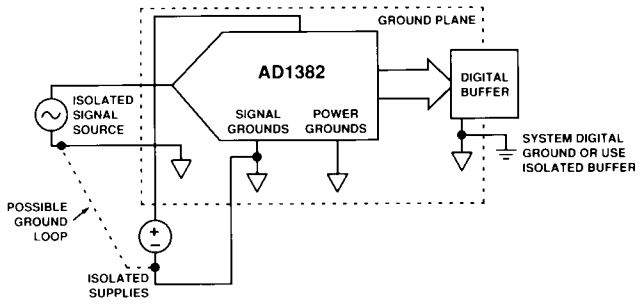


Figure 10. AD1382 Grounding

The AD1382 has a net ground current of about 40 mA. Most of this flows in the power grounds. There are also substantial dynamic currents in the power grounds. The signal grounds have primarily low level static (dc) currents. Signal and power grounds are separated inside the hybrid because the resistance and inductance inherent in thick-film construction would cause interactions between ground currents, leading to poor performance. (Remember that an LSB can be as small as 156 μV.)

Care must be taken to prevent the AD1382's ground currents from flowing in the signal ground between the signal source and the AD1382 if this ground has significant resistance. This is not usually a problem if the signal source is located on the same board as the AD1382 because the resistance can be made very low through the use of a ground plane.

The signal source's ground and supply currents must be considered when the source and ADC share common power supplies. A ground loop formed by the AD1382, the signal source, and the power supplies can cause significant errors.

The connection between the AD1382's ground plane and the system's digital ground is best made away from the AD1382. This will prevent noisy system ground currents from passing through critical parts of the ADC. In a very noisy environment it may be wise to isolate the entire analog circuit. Figure 10 shows the required isolation provided by a digital buffer. The buffer can then drive resistive and/or capacitive loads without compromising ground at the ADC. Using separate isolated supplies for the ADC and signal source will result in a single-point connection between system digital ground and the ADC's ground plane at the digital buffer.

Power Supplies and Bypassing

The AD1382 has four sets of power supply pins. These are:

±5 V Analog	(V_{DD1}/V_{SS1})
±15 V	($+V_{S1}/-V_{S1}$)
±15 V	($+V_{S2}/-V_{S2}$)
±5 V Power	(V_{DD2}/V_{SS2})

A single source may be used to supply like voltages (e.g., V_{DD1}, V_{DD2} from the same +5 V supply). Each of the four ±5 V supply pins should have a distinct low impedance connection to a well-bypassed central source node. This is required because each pin draws large transient currents. These dynamic currents, if passed through a common supply path, would introduce crosstalk and increase the AD1382's apparent noise. The two sets of ±15 V supplies need not be split in this fashion.

Every AD1382 supply pin should be bypassed to the ground plane with a high quality ceramic capacitor of 0.01 μF to 0.1 μF. This capacitor should be located as close as possible to the AD1382 to minimize lead lengths. Each V_{DD} and V_{SS} pin must also be bypassed to the ground plane with a 10 μF solid tantalum bypass capacitor located close to the AD1382. Ten microfarad bypass capacitors for $\pm V_{S2}$ (Pins 21 and 23) are also necessary. These power distribution concepts are shown in Figure 11.

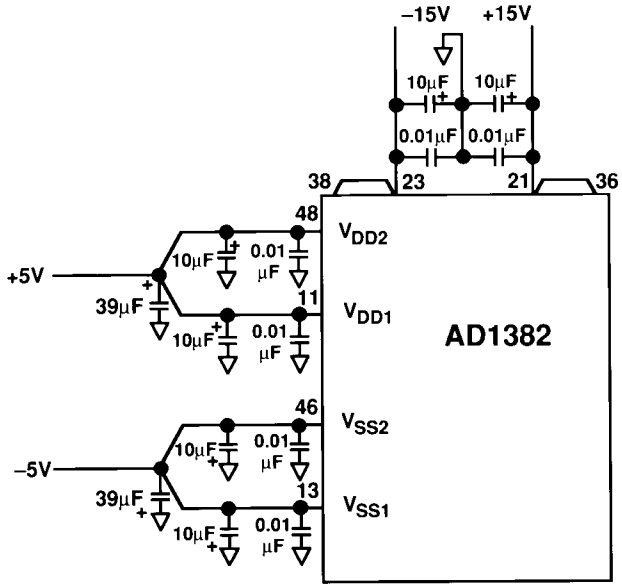


Figure 11. Recommended AD1382 Supply Distribution. All 10 μF and 0.01 μF Capacitors Must Be Located Close to the AD1382. Make All Ground Connections to Groundplane

All power supplies should be of the linear type. Switching power supplies are not recommended as they can introduce considerable high frequency noise into sensitive analog signal paths, degrading the AD1382's apparent performance.

Supply pins of equivalent voltage should not be allowed to differ by more than 0.3 V.

If separate ground planes are used for Signal and Power Ground, the supplies should be bypassed as follows:

Supply	Bypass to
±5 V Analog	Signal Ground
±15 V ($+V_{S1}/-V_{S1}$)	Signal Ground
±15 V ($+V_{S2}/-V_{S2}$)	Power Ground
±5 V Power	Power Ground

Care is also required when using a +5 V powered crystal oscillator to provide the AD1382's clock signal. These devices produce considerable supply noise and proper bypassing is essential. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low pass filtering of transients produced by the oscillator.

Reference

The AD1382 has an excellent internal reference with a typical temperature coefficient of 5 ppm/°C. The Reference Out (Pin 39) is normally connected to Reference In (Pin 32). An external reference may be connected to the reference input if desired. The reference input pin requires negligible current. The reference input voltage should not exceed +11 V and must remain more positive than −0.3 V. The reference output requires no bypassing and should not be capacitively loaded. If an external reference is used, it must have low noise to avoid degrading the signal to noise ratio of the AD1382.

The reference output can source up to 2 mA of static (dc) current without affecting the performance of the AD1382.

DIGITAL INTERFACES

10 MHz Clock

The AD1382 requires a stable external clock. A 10 MHz clock provides a sample rate of 500 kilosamples per second. Since the ADC operates synchronously with this clock, clock phase noise will appear as jitter in the aperture time. Lower clock frequencies may be used, and the sample rate will be reduced proportionately.

Standard TTL and CMOS crystal oscillator modules may be used successfully to generate the required 10 MHz clock signal. These oscillators often create considerable power supply transient noise. The oscillator should be bypassed with both ceramic and solid tantalum capacitors using minimum lead lengths. A 10 Ω resistor in series with the +5 V supply provides additional isolation and low-pass filtering of transients produced by the oscillator. See Figure 12.

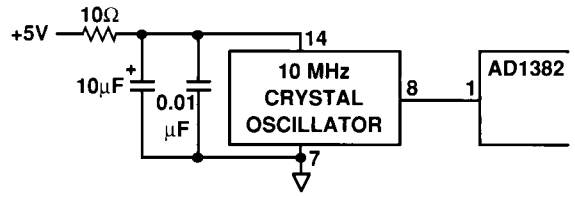


Figure 12. Isolating Clock Noise. Bypass Capacitors Should Be Located Close to the Oscillator

START CONVERT (Pin 18)

Synchronous Operation

The Start Convert signal acts like the data input of a flip-flop. A conversion begins on the first rising clock edge after Start Convert goes high (provided setup time requirements are met). This edge drives Hold Command Out high, switching the T/H into Hold mode. Hold Command Out (Pin 19) should be connected to Hold Command In (Pin 22) for synchronous operation. Continuous conversions at a 500 kHz rate may be obtained by holding Start Convert high. The 10 MHz clock may be divided down and used to drive the Start Convert input when a lower conversion rate is desired. This will provide clock-synchronized conversions at the lower rate. Synchronous conversion timing is shown in Figures 13 and 14.

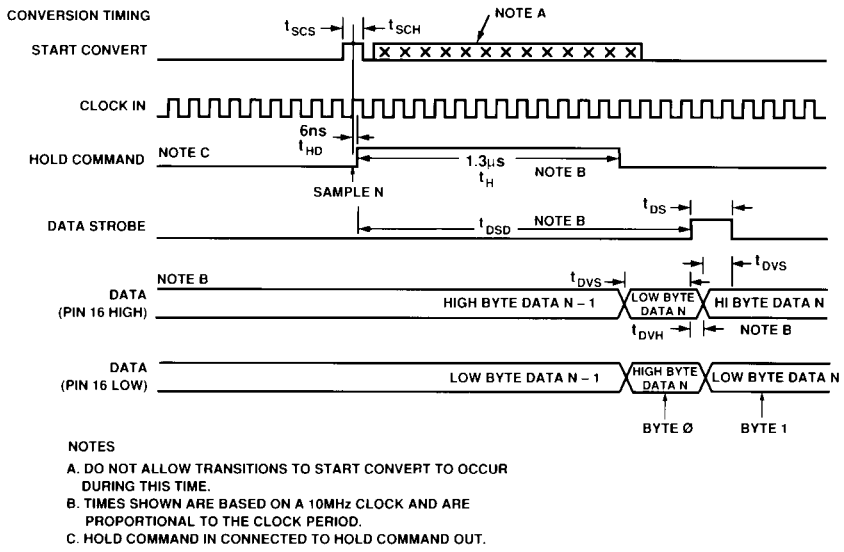


Figure 13. Start-Convert Controlled Conversion Timing

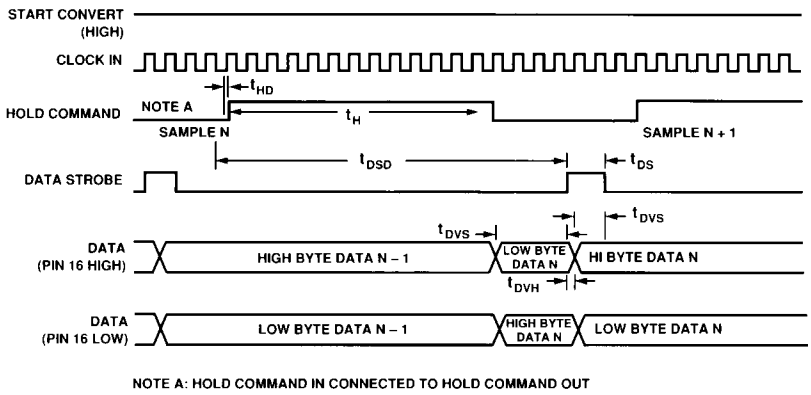


Figure 14. Free Running Conversion Timing

Start Convert may also be used as a gate to capture data only in a time window. The rising and falling edges of Start Convert define the beginning and end of the window during which conversions are desired.

Some restrictions apply to the timing of Start Convert. Transitions on the Start Convert pin should be limited to the 700 ns interval before the rising edge of Hold Command Out and to the 100 ns period after this edge. This minimizes coupling between Start Convert and sensitive internal circuit nodes.

Asynchronous Operation

In synchronous operation the T/H is placed into Hold mode by the first rising clock edge after Start Convert goes high. This mode of operation provides maximum rejection of system clock noise. Some applications may require the AD1382 to operate asynchronously, that is, with the Start Convert input directly controlling the track-to-hold transition. This may be achieved using a 2-input OR gate connected as shown in Figure 15. The rising edge of Start Convert places the T/H into Hold mode; the A/D conversion cycle begins with the first rising clock edge after the Start Convert transition, and Start Convert must remain high during at least one rising clock edge in order to begin the conversion. The width of Start Convert should be either less than 150 ns or greater than 1400 ns to minimize coupling between the falling edge of Start Convert and sensitive internal nodes. In asynchronous operation the T/H will remain in Hold mode as long either Hold Command Out or Start Convert is high. System timing requires careful scrutiny to ensure that the T/H has a minimum of 700 ns for signal acquisition before another conversion begins. The minimum width of Start Convert is 20 ns, the sum of t_{SCS} and t_{SCH}, the minimum setup and hold times.

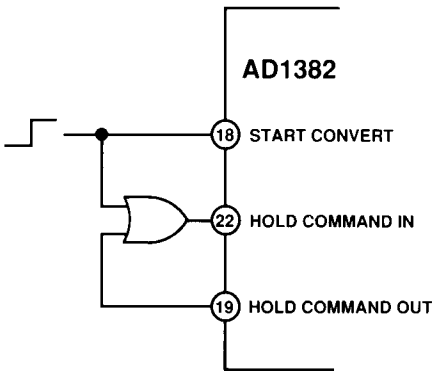


Figure 15. Connecting the AD1382 to Sample the Input Signal Asynchronously from the Clock

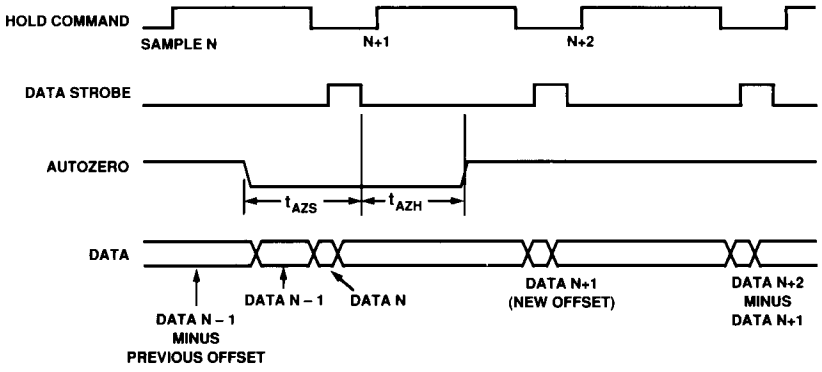


Figure 16. Autozero Cycle Operation

Output Data

The output data are multiplexed in two bytes onto an 8-bit data bus. Data are guaranteed to be stable at the time of the edges of Data Strobe (Pin 15). Hi/Lo Byte Select (Pin 16) controls which byte is presented first. If Hi/Lo Byte Select is high, then BYTE0 is B9–B16 and BYTE1 is B1–B8. The order of the data bytes is interchanged when Hi/Lo Byte Select is low. BYTE 0 and BYTE 1 are defined in the timing diagram Figure 13. B1 is the most significant bit of the reconstructed 16-bit data.

B1 SELECT (Pin 44) determines whether data is presented in complementary twos complement or complementary offset binary form. Complementary twos complement data is provided when B1 Select is LOW. $\overline{OE}$ may be used to place the data bus into a high impedance state.

The arithmetic unit in the AD1382 saturates at all 0s or all 1s if the input range is exceeded.

AUTOZERO (Pin 45)

The Autozero function may be used to digitally correct internal offsets in the Track/Hold and ADC as well as external offsets. To use Autozero the Track/Hold input must be connected to a zero reference prior to the zeroing conversion. This connection is external to the AD1382 and must be provided by the user; the resistance of this connection is not critical but should be less than 1000 Ω. An Autozero cycle forces the AD1382's digital output to indicate exactly zero when its input is at the zero point, nominally 0 V. (This assumes that the twos complement data format is used. Autozero forces the digital output to mid-scale when the selected data format is offset binary.) Autozero operates by storing the digital result of a zeroing conversion and subtracting it from all subsequent conversion results. This reduces the maximum nonsaturating input of the AD1382 a small amount at one end of its range depending on the magnitude and polarity of the offset.

The Autozero feature is enabled by driving the Autozero Input (Pin 45) low at the time of a falling edge at the Data Strobe output. Offset data will be stored on the first falling edge of Data Strobe after Autozero is brought high; the offset data are also available on the AD1382's data bus during this Data Strobe pulse. Autozero operation is illustrated in Figure 16. All subsequent A/D conversions will be digitally corrected by the offset term as long as Autozero remains high. The offset register is cleared when Autozero goes low and the contents of the data output registers will revert to their uncorrected value. Figure 17 shows Autozero timing requirements. Autozero cannot be activated until the first conversion after powerup has been completed.

The Autozero feature may be disabled by keeping Autozero low.

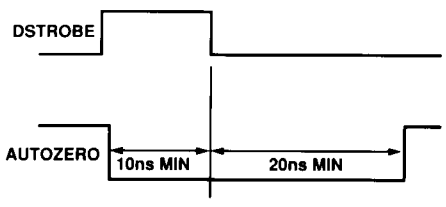


Figure 17. Autozero Setup and Hold Times

GAIN ADJUST (Pin 40)

The internal reference of the AD1382 may be adjusted by varying the voltage applied to the Gain Adjust pin. The input impedance of this pin is nominally 20 kΩ, with a tolerance of ±20%. A change of 1 V on Pin 40 will change the reference voltage by about 10 mV. The reference may be adjusted by ±150 mV without degrading the AD1382's performance. The simplest method of implementing the gain adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Gain Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Gain Adjust pin.

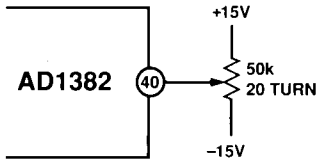


Figure 18a. AD1382 Gain Adjust Circuit

OFFSET ADJUST (Pin 29)

The ADC's offset voltage may be adjusted by means of a voltage applied to the Offset Adjust pin. The nominal adjustment sensitivity is 0.005% FSR/V. The input impedance is 20 kΩ with a ±20% tolerance. The simplest way to implement the offset adjust is to connect a potentiometer between the ±15 V supplies, with the wiper connected to the Offset Adjust pin. Care should be taken to ensure that noise does not enter the ADC through the Offset Adjust pin.

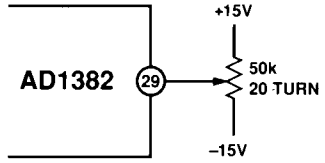


Figure 18b. AD1382 Offset Adjust Circuit

APPLICATIONS

Mounting and Thermal Considerations

Although the AD1382 will operate over a wide temperature range, best performance is obtained by maintaining the case temperature between 40°C and 70°C. This can usually be achieved without a heat sink provided there is a moderate amount of air flow. Under these conditions the case temperature will rise about 20°C. Performance will degrade gradually outside the specified temperature range due to linearity drift in the reference DAC.

System thermal analysis or experimental evidence may show that a heat sink is necessary. A thin heat transfer plate can be mounted under the package to conduct heat into the ground plane. This plate may be made of metal or from an elastomeric heat conducting material. Elastomeric materials will conform to the board and to the AD1382 package to improve heat transfer while reducing mechanical stress. They also have the advantage of not requiring thermally conductive grease.

Testing the AD1382

It is difficult to test the AD1382 with ordinary test methods because of the part's very low distortion and noise. The number of output codes and the nature of the analog to digital conversion make static tests of performance especially cumbersome. Subranging converters with error correction circuitry can have flaws at any place in their transfer function and all codes must be exercised for a complete test.

Histograms provide a convenient way to measure all codes in a modest amount of time. Even histograms can be slow, though, when 20 million conversions (40 seconds) may be required to achieve statistically valid results.

Distortion and dynamic range tests based on FFTs are the most powerful tests. They quantify noise and nonlinearity as a function of input frequency. From them one can infer qualitative integral and differential nonlinearity performance while determining the ADC's specific dynamic performance. FFTs are especially useful for systems which require excellent dynamic response, such as magnetic resonance imaging. They also uncover performance problems that don't show up in static tests of linearity.

The difficulty in doing FFT tests stems from the requirement for ultra pure sine wave inputs at various frequencies over the operating bandwidth of the ADC. Even the best available generators are not capable of supplying signals with sufficiently low noise and low distortion for testing the AD1382. Few generators permit phase-locking to the ADC clock. Phase-locking makes it possible to obtain an integral number of cycles of the input sine wave within the FFT data window, which in turn eliminates the need for windowing functions and the spectral spreading they cause.

The best generator currently available for this purpose is the Brüel and Kjær Model 1051 (or 1049). This generator provides a programmable output frequency up to 250 kHz with better than 0.001 Hz resolution. The generator's distortion performance at frequencies below 20 kHz is better than the AD1382 but degrades at 100 kHz and higher. Noise is a problem at all frequencies, being about −85 dB over the AD1382's bandwidth. Both noise and distortion can be reduced to acceptable levels with filters. Passive filters with narrow bandwidth will reduce harmonic distortion to less than −100 dB. Inductors wound on large pot cores with air gaps can be made quite linear, and with careful winding will provide low loss and low capacitance. Such filters will reduce noise to negligible levels outside their pass band to provide a much better view of actual ADC performance. The effect of aperture jitter, for example, cannot be observed without a filter.

The FFTs shown in Figures 1–8 were produced using these methods. These tests are done as a normal part of production testing to guarantee the dynamic performance of the AD1382.

High Impedance Inputs

Using the AD1382 in multiplexed applications requires buffering the part's 2.5 kΩ input impedance to eliminate the distorting effects of nonlinear multiplexer on-resistance. The choice of buffer amplifier depends on the nature of the input signals.

"Static" Applications

Amplifier noise, CMRR linearity, and settling time are of primary importance when the inputs are low frequency or DC. This is the case in a CAT scan imager, for example, when signals are produced by integrating photocurrents. Noise limits ultimate system resolution. The AD1382 has a typical input-referred noise of 55 μV rms. Buffer noise must be added to this in a root-sum-squares fashion to determine total system noise. A buffer amplifier which adds noise of 18 μV rms, for example, will result in a system noise level of $(18^2+55^2)^{1/2}$ = 58 μV rms, a negligible increase. Detailed system noise calculations require knowledge of the buffer's noise spectral density and equivalent noise bandwidth. The AD1382's equivalent noise bandwidth is 2.2 MHz. *Low Noise Electronic Design* (C.D. Motchenbacher and F.C. Fitchen, John Wiley and Sons, New York, 1973) provides excellent discussions of noise analysis and calculations.

Buffer amplifier CMRR produces an apparent gain error as long as the value of CMRR is independent of signal level. The size of this "gain error" is directly related to the actual value of CMRR; an amplifier with 60 dB CMRR will create an apparent gain error of 0.1%. The precise value of CMRR is not critical as long as it remains constant with signal level. Any variation in CMRR with input level will introduce nonlinearity. The smaller the value of CMRR (in dB), the more critical variations in this value become. An amplifier with CMRR ranging from 100 dB to 110 dB over the range of −10 V to +10 V will produce negligible nonlinearity, while an amplifier whose CMRR varies from 60 dB to 70 dB over the same range would be completely unacceptable.

Buffer settling time will affect the system's throughput. The system sample rate can be maintained at 500 kHz provided the buffer's settling time is less than about 1.7 microseconds. The input channel should be switched just after the AD1382's SHA enters Hold mode as indicated by a rising edge at Hold Command In (Pin 22).

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Dynamic applications complicate the choice of buffer amplifier. The amplifier's harmonic distortion performance now becomes as important as its noise, CMRR linearity, and settling behavior. Few manufacturers specify amplifier THD in the noninverting configuration. These specifications, when available, seldom address signals greater than 10 V p–p or at frequencies above 1 kHz. It may be necessary to characterize candidate amplifiers from several vendors to find the best fit to the particular amplitude and frequency requirements of a particular application. Such evaluations are easily performed using a spectrum analyzer. A notch filter tuned to the fundamental frequency greatly improves measurement resolution. It is also possible to use the AD1382 as the measuring device by performing FFTs on the output data. Refer to the discussion of signal sources in *Testing the AD1382*.

Unipolar Operation

The AD1382 does not provide a direct unipolar input capability. Unipolar inputs can be achieved using the circuits of Figures 19 and 20. The circuit in Figure 19 is suitable when a low input impedance is acceptable. Multiplexed applications should use the circuit of Figure 20. The discussions under High Impedance Inputs also apply to amplifier selection for unipolar operation.

Data Bus Interface

The AD1382's data outputs are CMOS 4 mA drivers and are not intended to be connected directly to a system data bus. Charging and discharging a capacitive data bus creates large supply transients and ground spikes which can interfere with the AD1382's operation and result in erroneous data. Registers and/or buffers should be used to isolate the AD1382 from the bus. Buffering devices should be located close to the AD1382 to minimize the capacitive load presented to the converter's data outputs. Control will be simplified by permanently grounding the AD1382's $\overline{OE}$ input when using buffers. A schematic of a typical 16-bit bus interface is shown in Figure 21.

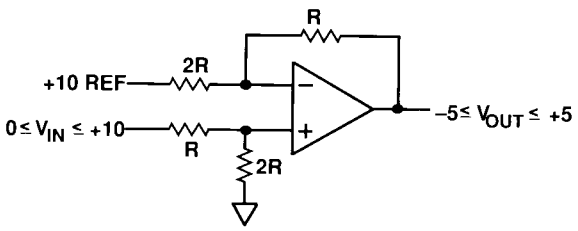

Figure 19. Unipolar-to-Bipolar Conversion (Low Input Impedance)

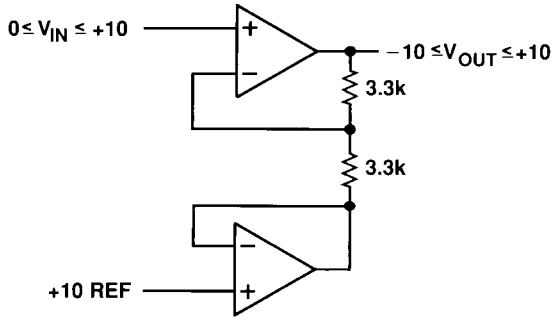

Figure 20. High Input Impedance Unipolar-to-Bipolar Conversion Circuit

Sample Board Layout

Figures 22–27 show the layout of an evaluation board for the AD1382. This layout incorporates the grounding, power distribution, and interface concepts described in previous sections. This 4-layer layout makes extensive use of ground and power planes and provides optimal AD1382 performance.

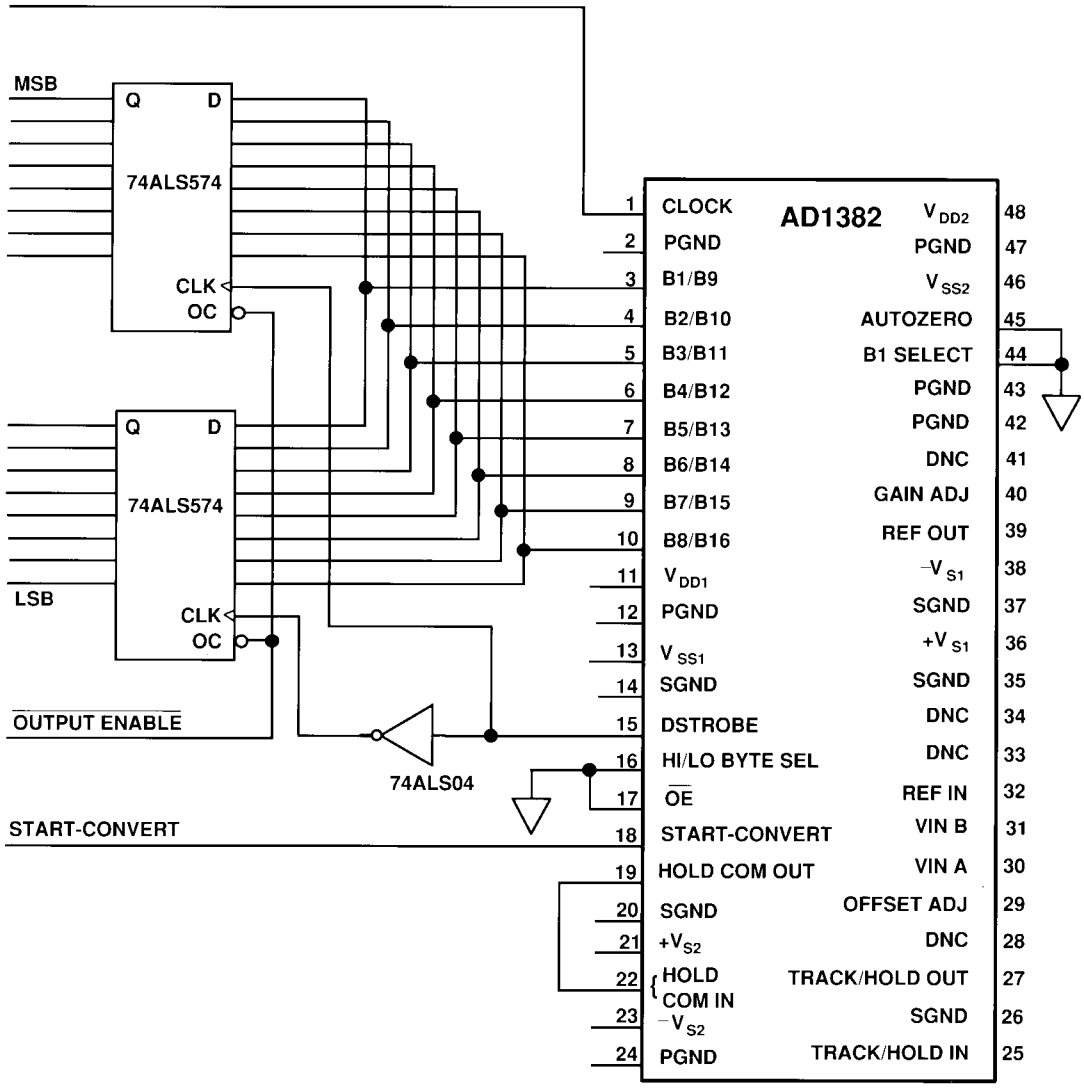

Figure 21. Basic AD1382 Digital Interface (16-Bit 2s Complement Data, Autozero Not Used)

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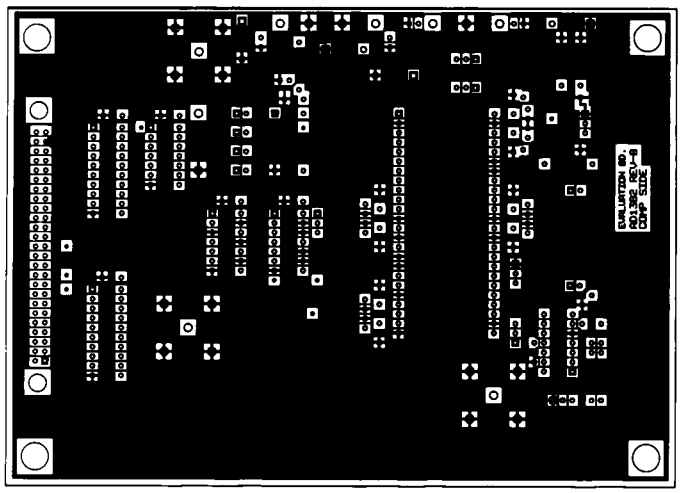

Figure 23. AD1382 Evaluation Board Layout, Layer 1 (Component Side)

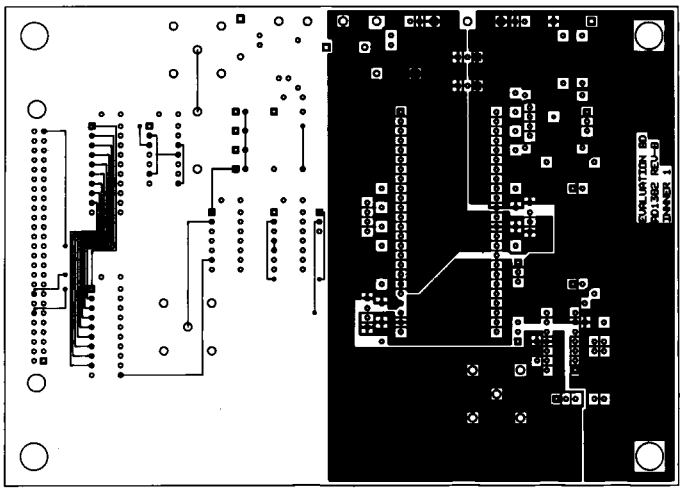

Figure 24. AD1382 Evaluation Board Layout, Layer 2

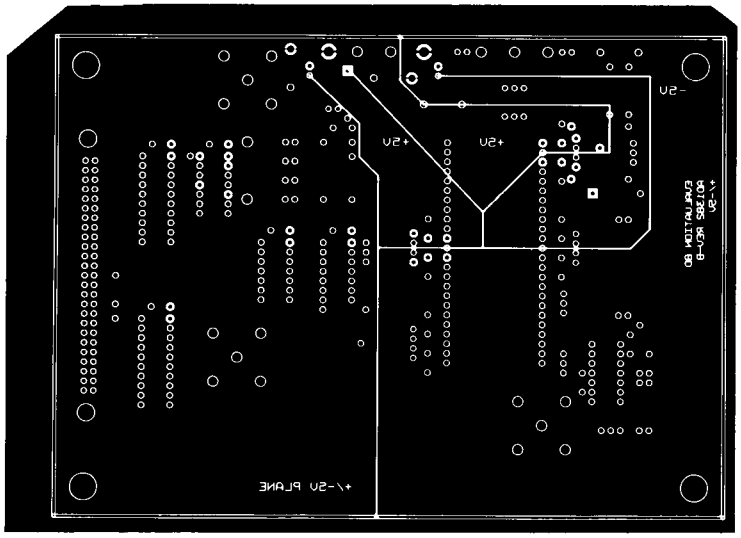

Figure 25. AD1382 Evaluation Board Layout, Layer 3

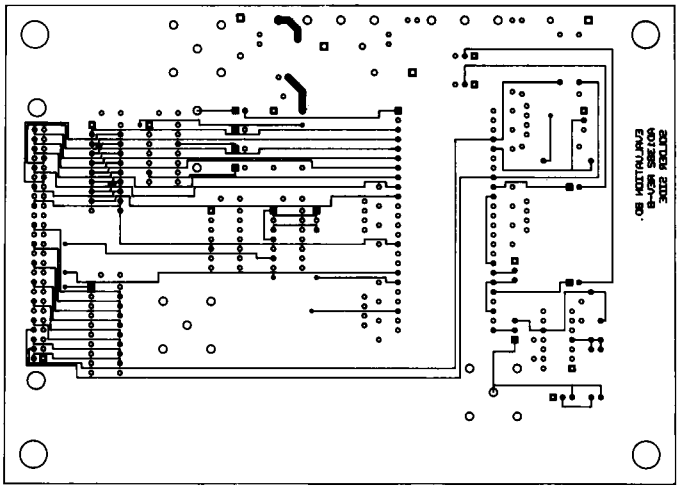

Figure 26. AD1382 Evaluation Board Layout, Layer 4 (Solder Side)

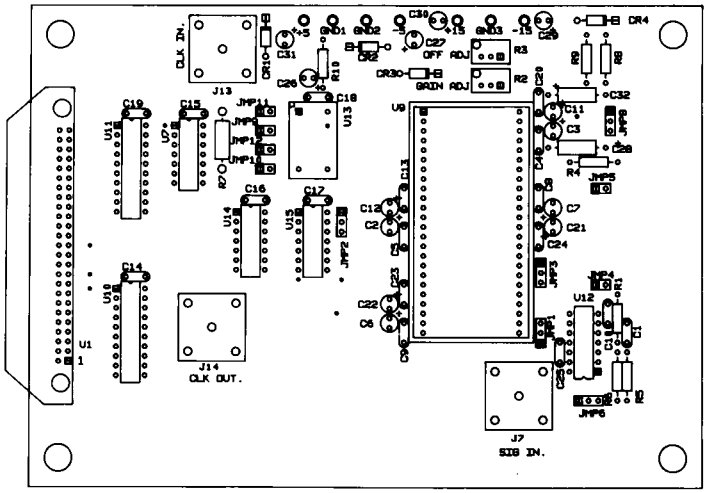

Figure 27. AD1382 Evaluation Board Silkscreen

AD1382 EVALUATION BOARD PARTS LIST

Qty.	Ref. Des.	Description (Manufacturer/PN)
1	C1	Ceramic Capacitor, 10 pF, 50 V (Mallory CEC100J)
13	C2, C3, C6, C7, C11 C12, C21, C22, C26, C27, C29–C31	Tantalum Capacitor, 10 μF, 35 V (Mallory TDL106K035S1D)
16	C4, C5, C8–C10, C13–C20, C23–C25	Ceramic Cap, 0.1 μF, 100 V (Murata Erie RPE122Z5U104M100V)
2	C28, C32	Tantalum Capacitor, 39 μF, 10 V (Kemet T110B396K010AS)
4	CR1–CR4	1N4001 Diode
3	J7, J13, J14	BNC Female, PC Mount (Pomona 4578)
8	JMP2–JMP6, JMP8, JMP9, JMP13	Jumper, 2 Position (3M 929950-00)
3	R1, R5, R6	RN55C Resistor, 2.00k
2	R2, R3	50k 20-Turn Trimpot* (Bourns 3299W-1-503)
2	R4, R9	RN55C Resistor, 10.0k
1	R7	Carbon Composition Resistor, 100 Ω, 1/2 W
1	R10	RN55C Resistor, 10 Ω
1	U7	74ALS74
1	U9	AD1382KD (Analog Devices)
2	U10, U11	74ALS574
1	U12	AD842KN (Analog Devices)
1	U13	10 MHz DIP Crystal Oscillator
1	U14	74ALS04
1	U15	74ALS32
2	—	Socket Strip (SPC MPS1P-32-GG)
1	—	Pin Strip (3M 929647-01-36)
1	—	Socket, 14-Pin Oscillator (Augat 504-AG10D)
4	—	Socket, 14-Pin (Augat 514-AG11D)
2	—	Socket, 20-Pin (Augat 520-AG11D)
2	—	Ejector Latch (3M 3505-3)
1	—	50-Pin Connector (3M 3433-5002)
2	—	Screw, 2-56 × 1/2
2	—	Hex Nut, 2-56

*Trimpot is a trademark of Bourns.