+2.5 V to +5.5 V, 500μA, 2-Wire Interface, Quad Voltage Output 8-/10-/12-Bit DACs

Preliminary Technical Data AD5306/AD5316/AD5326*

FEATURES

AD5306: Four Buffered 8-Bit DACs in 16-Lead TSSOP
AD5316: Four Buffered 10-Bit DACs in 16-Lead TSSOP
AD5326: Four Buffered 12-Bit DACs in 16-Lead TSSOP
Low Power Operation: 500 μA @ 3V, 600 μA @ 5V
2-Wire (I^2C^{TM} Compatible) Serial Interface
+2.5V to +5.5V Power Supply
Guaranteed Monotonic By Design Over All Codes
Power Down to 80nA@3V, 200nA@5V
Double-Buffered Input Logic
Buffered/Unbuffered Reference Input Options
Output Range: 0-V_{REF} or 0-2V_{REF}
Power-On-Reset to Zero Volts
Simultaneous Update of DAC Outputs ($\overline{LDAC}$ pin)
Software Clear Facility
Data Readback facility
On-Chip Rail-to-Rail Output Buffer Amplifiers
Temperature Range -40°C to 105°C

APPLICATIONS

Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Control

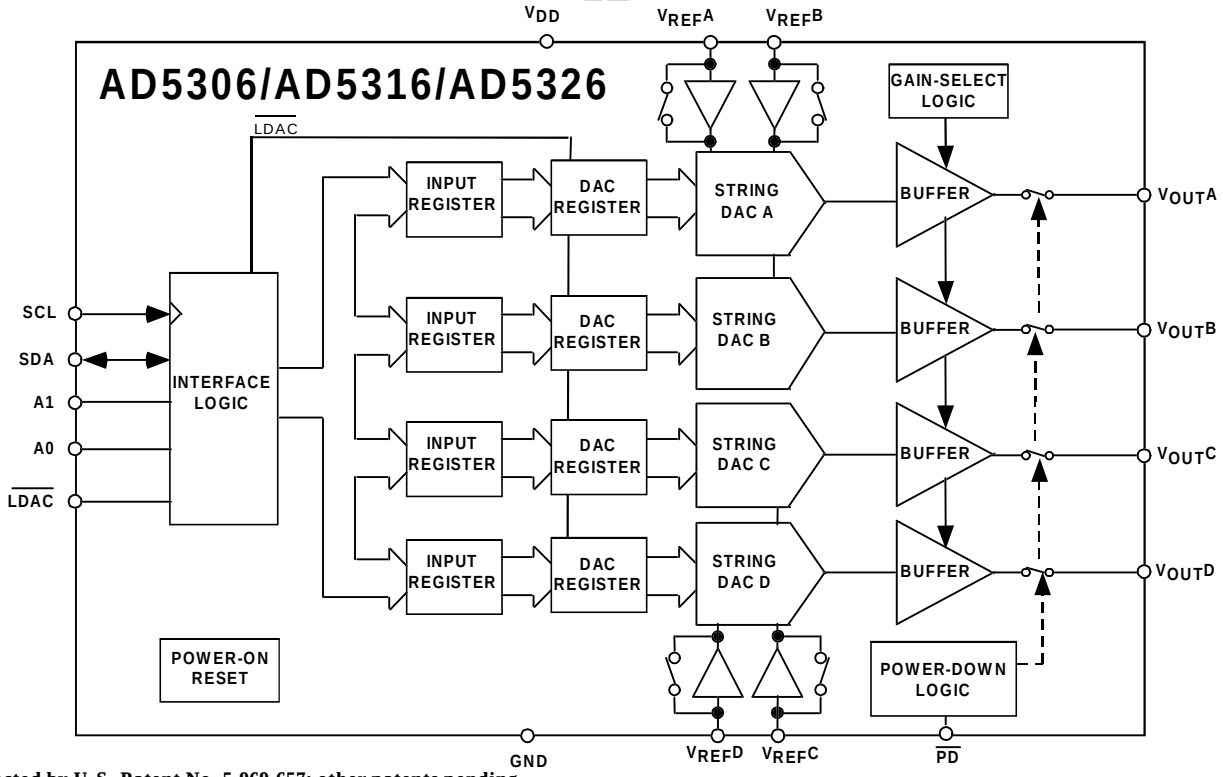
GENERAL DESCRIPTION

The AD5306/AD5316/AD5326 are quad 8-, 10- and 12-bit buffered voltage output DACs which operate from a single +2.5V to +5.5V supply consuming 500μA at 3V. Their on-chip output amplifiers allow rail-to-rail output swing with a slew rate of 0.7V/μs. A 2-wire serial interface is used which operates at clock rates up to 400kHz. This interface is SMBus-Compatible at V_{DD} < 3.6 V. Multiple devices can be placed on the same bus.

The DAC reference inputs can be configured as buffered or unbuffered inputs. The outputs of all DACs may be updated simultaneously using the asynchronous $\overline{LDAC}$ input The parts incorporate a power-on-reset circuit that ensures that the DAC outputs power up to zero volts and remain there until a valid write takes place to the device. There is also a software clear function which clears all DACs to 0V. The parts contain a power-down feature which reduces the current consumption of the device to 200nA at 5V (80nA at 3V).

All three parts are offered in the same pinout which allows users to select the amount of resolution appropriate for their application without re-designing their circuit-board.

FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,969,657; other patents pending
I^2C^{TM} is a registered trademark of Philips Corporation

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AD5306/AD5316/AD5326–SPECIFICATIONS

(V_{DD} = +2.5V to +5.5 V; V_{REF}=+2V; R_L=2kΩ to GND; C_L=200pFto GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Units	Conditions/Comments
DC PERFORMANCE[3,4]					
AD5306					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic by design over all codes
AD5316					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic by design over all codes
AD5326					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	See Figures 2 and 3
Gain Error		±0.15	±1	% of FSR	See Figures 2 and 3
Lower Deadband[5]		20	60	mV	Lower Deadband exists only if offset error is negative
Upper Deadband		TBD	TBD	mV	Upper Deadband exists if $V_{REF} = V_{DD}$
Offset Error Drift[6]		-12		ppm of FSR/°C	
Gain Error Drift[6]		-5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		-60		dB	ΔV_{DD} = ±10%
DC Crosstalk[6]		200		µV	R_L = 2kΩ to GND and V_{DD}
DAC REFERENCE INPUTS[6]					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference Mode.
	0.25		V_{DD}	V	Unbuffered Reference Mode
V_{REF} Input Impedance		>10		MΩ	Buffered reference mode and Power-Down mode.
	TBD	180		kΩ	Unbuffered reference mode. 0-V_{REF} output range.
	TBD	90		kΩ	Unbuffered reference mode. 0-2V_{REF} output range.
Reference Feedthrough		-90		dB	Frequency=10kHz
Channel-to-Channel Isolation		-80		dB	Frequency=10kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[7]		0.001		V min	This is a measure of the minimum and maximum drive
Maximum Output Voltage[7]		V_{DD}-0.001		V max	capability of the output amplifier
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = +5V
		16		mA	V_{DD} = +3V
Power Up Time		2.5		µs	Coming out of Power Down Mode. V_{DD} = +5 V
		5		µs	Coming out of Power Down Mode. V_{DD} = +3 V
LOGIC INPUTS (excl.SCL, SDA)[6]					
Input Current			±1	µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = +5V±10%
			0.6	V	V_{DD} = +3V±10%
			0.5	V	V_{DD} = +2.5V
V_{IH}, Input High Voltage	1.7			V	V_{DD} = +2.5V to 5.5V; TTL & 1.8V-CMOS compatible
Pin Capacitance		3		pF	
LOGIC I/O'S (SCL, SDA)[6]					
V_{IH}, Input High Voltage	0.7 V_{DD}		V_{DD}+0.3	V	
V_{IL}, Input Low Voltage	-0.3		0.3 V_{DD}	V	
I_{IN}, Input Leakage Current		TBD	±1	µA	V_{IN} = 0V to V_{DD}.
V_{HYST}, Input Hysteresis	0.05 V_{DD}			V	
C_{IN}, Input Capacitance		3		pF	
Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50ns
LOGIC OUTPUT (SDA)[6]					
V_{OL}, Output Low Voltage			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1	µA	
Three-State Output Capacitance			10	pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					$V_{IH} = V_{DD}$, V_{IL} = GND.
V_{DD}= +4.5V to +5.5V		0.6	0.9	mA	I_{DD} spec. is valid for all DAC codes. All DACs active.
V_{DD}= +2.5V to +3.6V		0.5	0.7	mA	Interface inactive. DAC Outputs unloaded.
I_{DD} (Full Power-Down)					$V_{IH} = V_{DD}$, V_{IL} = GND.
V_{DD} = +4.5V to +5.5V		0.2	1	µA	Idd = 5 µA (max) during "0" readback on SDA
V_{DD} = +2.5V to +3.6V		0.08	1	µA	Idd = 1.5 µA (max) during "0" readback on SDA

NOTES

[1]See Terminology

[2]Temperature range: B Version: -40°C to +105°C; typical at +25°C

[3]DC specifications tested with the outputs unloaded unless stated otherwise.

[4]Linearity is tested using a reduced code range:AD5306(code 8 to 255); AD5316 (code 28 to 1023); AD5326 (code 115 to 4095)

[5]This corresponds to x codes. x= Deadband Voltage/LSB size

[6]Guaranteed by Design and Characterization, not production tested

[7]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, V_{REF}=V_{DD} and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

AC CHARACTERISTICS[1]

(V_{DD} = +2.5V to +5.5 V; R_L=2kΩ to GND and V_{DD}; C_L=200pF to GND; All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Units	Conditions/Comments
Output Voltage Settling Time					V_{REF}=V_{DD}=+5V
AD5306		6	8	µs	1/4 Scale to 3/4 Scale change (40 Hex to C0 Hex)
AD5316		7	9	µs	1/4 Scale to 3/4 Scale change (100 Hex to 300 Hex)
AD5326		8	10	µs	1/4 Scale to 3/4 Scale change (400 Hex to C00 Hex)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Impulse		12		nV-s	1 LSB change around major carry.
Digital Feedthrough		0.10		nV-s	
Digital Crosstalk		0.01		nV-s	
Analog Crosstalk		0.01		nV-s	
DAC-to-DAC Crosstalk		0.01		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF}=2V±0.1Vpp
Total Harmonic Distortion		-70		dB	V_{REF}=2.5V±Vpp. Frequency=10kHz.

NOTES
[1]See Terminology
[2]Guaranteed by Design and Characterization, not production tested.
[3]Temperature range: B Version: -40°C to +105°C; typical at +25°C
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +2.5 V to +5.5 V . All specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter[2]	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
F_{SCL}	400	kHz max	SCL Clock Frequency
t_1	2.5	µs min	SCL Cycle Time
t_2	0.6	µs min	t_{HIGH}, SCL High Time
t_3	1.3	µs min	t_{LOW}, SCL Low Time
t_4	0.6	µs min	$t_{HD,STA}$, Start/Repeated Start Condition Hold Time
t_5	100	ns min	$t_{SU,DAT}$, Data Setup Time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, Data Hold Time
	0	µs min	
t_7	0.6	µs min	$t_{SU,STA}$, Setup Time for Repeated Start
t_8	0.6	µs min	$t_{SU,STO}$, Stop Condition Setup Time
t_9	1.3	µs min	t_{BUF}, Bus Free Time Between a STOP and a START Condition.
t_{10}	300	ns max	t_R, Rise Time of SCL and SDA when receiving
	0	ns min	t_R, Rise Time of SCL and SDA when receiving (CMOS compatible)
t_{11}	250	ns max	t_F, Fall Time of SDA when transmitting.
	0	ns min	t_F, Fall Time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, Fall Time of SCL and SDA when receiving
	$20+0.1C_b$[4]	ns min	t_F, Fall Time of SCL and SDA when transmitting
t_{12}	TBD	ns min	$\overline{LDAC}$ PulseWidth
t_{13}	TBD	ns min	SCLK falling edge to $\overline{LDAC}$ Rising Edge
C_b	400	pF max	Capacitive Load for Each Bus Line.

NOTES
[1]See Figure 1.
[2]Guaranteed by Design and Characterization, not production tested.
[3]A master device must provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH\ min}$ of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[4]C_b is the total capacitance of one bus line in pF. t_R and t_F measured between $0.3V_{DD}$ and $0.7V_{DD}$.
Specifications subject to change without notice.

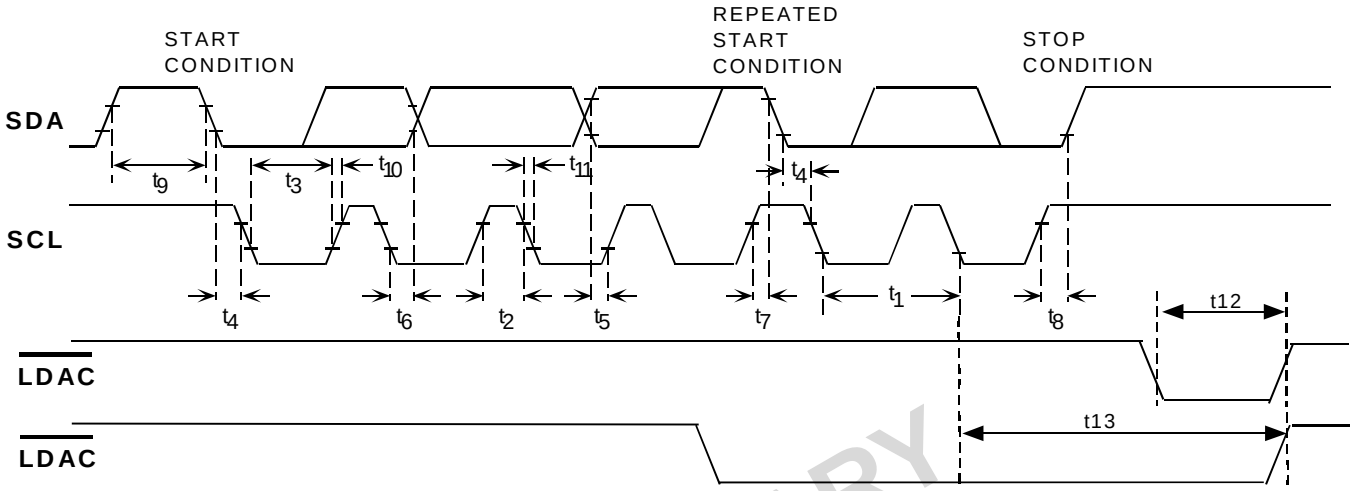


Figure 1. 2-Wire Serial Interface Timing Diagram

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD5306BRU	-40°C to +105°C	RU-16
AD5316BRU	-40°C to +105°C	RU-16
AD5326BRU	-40°C to +105°C	RU-16

*RU = TSSOP (Thin Shrink Small Outline Package)

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... -0.3 V to +7 V
SCL, SDA to GND ..... -0.3 V to V_{DD} + 0.3 V
A0, A1, $\overline{LDAC}$, $\overline{PD}$ to GND ..... -0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND .. -0.3 V to V_{DD} + 0.3 V
V_{OUT}A-D to GND ..... -0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature (T_J max) ..... +150°C

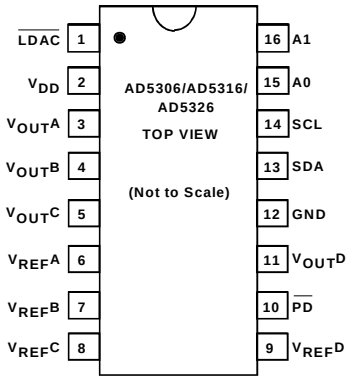
16-Lead TSSOP Package
Power Dissipation.....(T_J max - T_A) / θ_{JA}
θ_{JA} Thermal Impedance ..... 150.4 °C /W
Reflow Soldering
Peak Temperature ..... 220 +5/-0 °C
Time at Peak Temperature ..... 10 sec to 40 sec

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5306/AD5316/AD5326 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges.Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTION

PIN NUMBERS

Pin No.	Mnemonic	Function
1	$\overline{LDAC}$	Active low control input which transfers the contents of the input registers to their respective DAC registers. Pulsing this pin low allows the simultaneous update of all DAC outputs
2	V_{DD}	Power Supply Input. These parts can be operated from +2.5V to +5.5V and the supply should be decoupled to GND.
3	$V_{OUT}A$	Buffered analog output voltage from DAC A. The output amplifier has rail-to-rail operation.
4	$V_{OUT}B$	Buffered analog output voltage from DAC B. The output amplifier has rail-to-rail operation.
5	$V_{OUT}C$	Buffered analog output voltage from DAC C. The output amplifier has rail-to-rail operation.
6	$V_{REF}A$	Reference Input pin for DAC A. It may be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC A. It has an input range from 0.25V to V_{DD} in unbuffered mode and from 1V to V_{DD} in buffered mode.
7	$V_{REF}B$	Reference Input pin for DAC B. It may be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC B. It has an input range from 0.25V to V_{DD} in unbuffered mode and from 1V to V_{DD} in buffered mode.
8	$V_{REF}C$	Reference Input pin for DAC C. It may be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC C. It has an input range from 0.25V to V_{DD} in unbuffered mode and from 1V to V_{DD} in buffered mode.
9	$V_{REF}D$	Reference Input pin for DAC D. It may be configured as a buffered or an unbuffered input depending on the state of the BUF bit in the input word to DAC D. It has an input range from 0.25V to V_{DD} in unbuffered mode and from 1V to V_{DD} in buffered mode.
10	$\overline{PD}$	Active low control input which acts as a hardware Power-Down option. All DACs go into power-down mode when this pin is tied low. The DAC outputs go into a high-impedance state. The current consumption of the part drops to 200nA @ 5V (80nA @ 3V).
11	$V_{OUT}D$	Buffered analog output voltage from DAC D. The output amplifier has rail-to-rail operation.
12	GND	Ground reference point for all circuitry on the part.
13	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into the 16-bit input shift register. It is a bi-directional open-drain data line which should be pulled to the supply with an external pull-up resistor.
14	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 16-bit input shift register. Clock rates of up to 400kbit/s can be accommodated in the I^2C compatible interface.
15	A0	Address Input. Sets the least significant bit of the 7-bit slave address.
16	A1	Address Input. Sets the 2nd least significant bit of the 7-bit slave address.

TERMINOLOGY

RELATIVE ACCURACY
For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. Typical INL vs. Code plots can be seen in Figures 4, 5 and 6.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. Code plots can be seen in Figures 7, 8 and 9.

OFFSET ERROR
This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

GAIN ERROR
This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

OFFSET ERROR DRIFT
This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of Full-Scale Range)/°C.

GAIN ERROR DRIFT
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of Full-Scale Range)/°C.

DC POWER-SUPPLY REJECTION RATIO (PSRR)
This indicates how the output of a DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at +2V and V_{DD} is varied ± 10%.

DC CROSSTALK
This is the DC change in the output level of one DAC at mid-scale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in µV.

REFERENCE FEEDTHROUGH
This is the ratio of the amplitude of the signal at the DAC output to it's reference input when the DAC output is not being updated (i.e. $\overline{\text{LDAC}}$ is high). It is expressed in dBs.

CHANNEL-TO-CHANNEL ISOLATION
This is the ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference input of another DAC. It is measured in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY
Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-secs and is measured when the digital code is changed by 1LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

DIGITAL FEEDTHROUGH
Digital Feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, when the DAC output is not being updated. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g. from all 0s to all 1s or vice versa.

DIGITAL CROSSTALK
This is the glitch impulse transferred to the output of one DAC at mid-scale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV-secs.

ANALOG CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The energy of the glitch is expressed in nV-secs.

DAC-TO-DAC CROSSTALK
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-secs.

MULTIPLYING BANDWIDTH
The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3dB below the input.

TOTAL HARMONIC DISTORTION
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

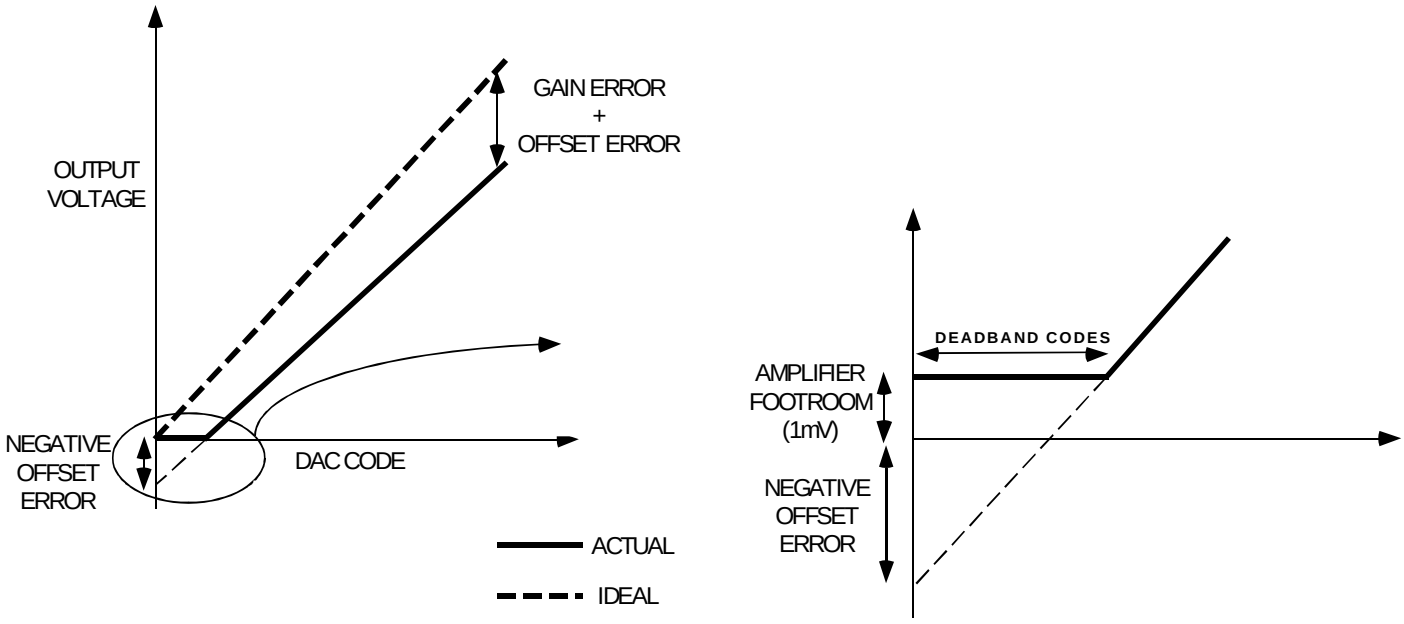


Figure 2. Transfer Function with Negative Offset

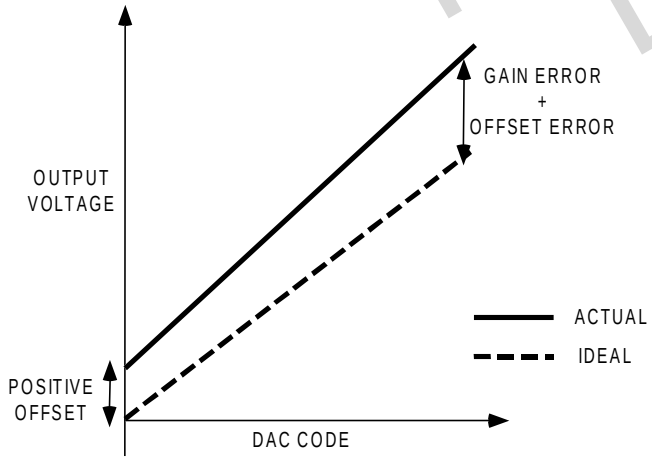


Figure 3. Transfer Function with Positive Offset

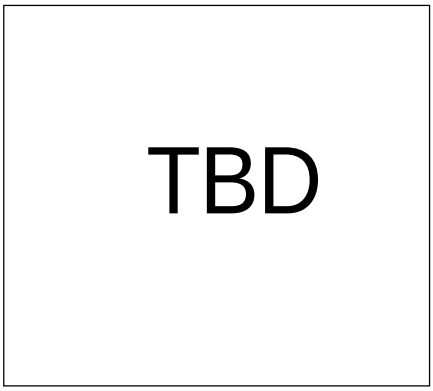


Figure 4. AD5306 Typical INL Plot

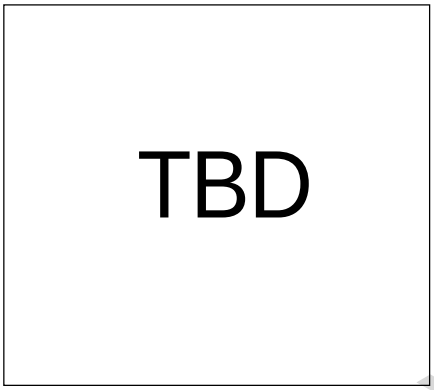


Figure 5. AD5316 Typical INL Plot

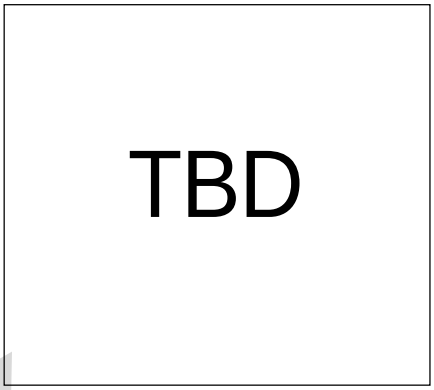


Figure 6. AD5326 Typical INL Plot

Figure 7. AD5306 Typical DNL Plot

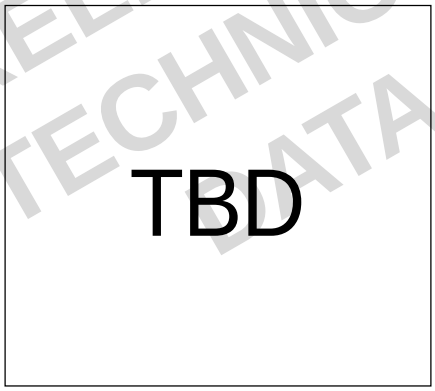


Figure 8. AD5316 Typical DNL Plot

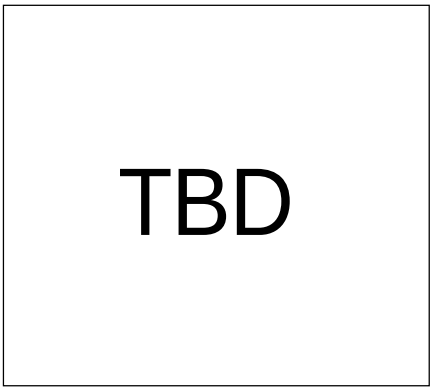


Figure 9. AD5326 Typical DNL Plot

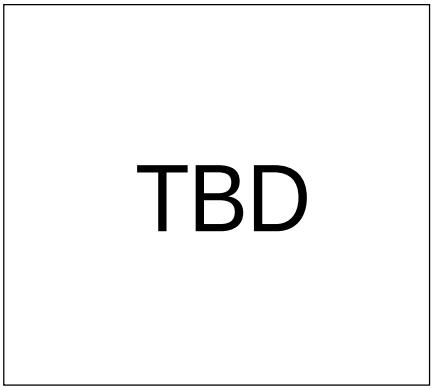


Figure 10. AD5306 INL and DNL Error vs. V_{REF}

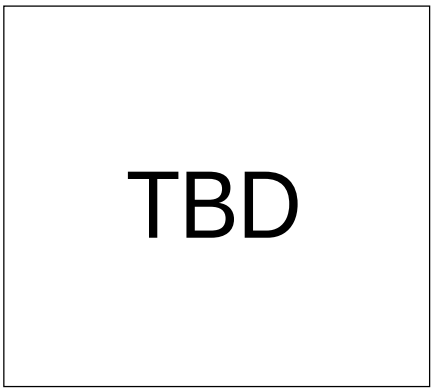


Figure 11. AD5306 INL Error and DNL Error vs. Temperature

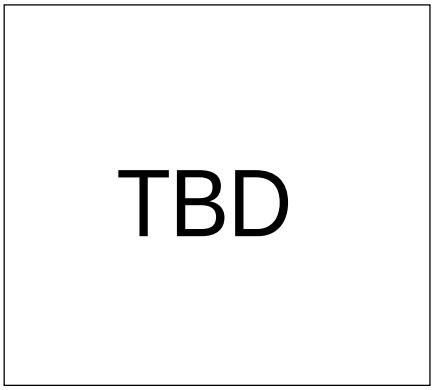


Figure 12. AD5306 Offset Error and Gain Error vs. Temperature

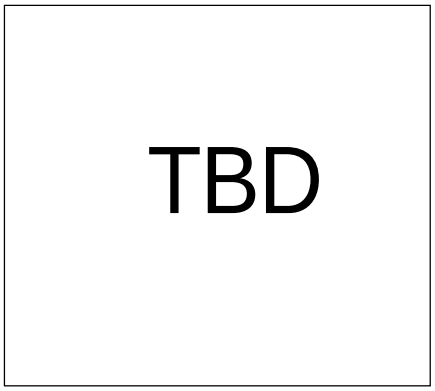


Figure 13. Offset Error and Gain Error vs. V_{DD}

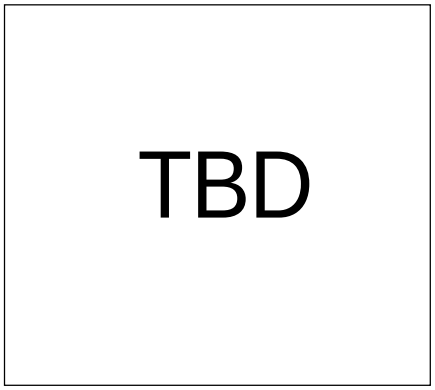


Figure 14. V_{OUT} Source and Sink Current Capability

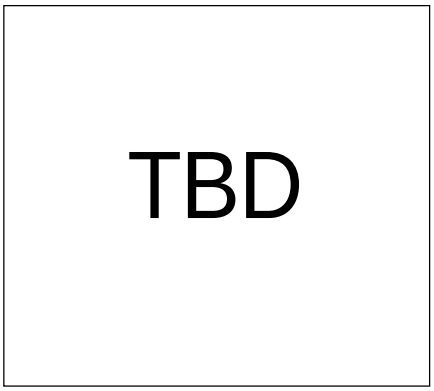


Figure 15. Supply Current vs. DAC Code

Figure 16. Supply Current vs. Supply Voltage

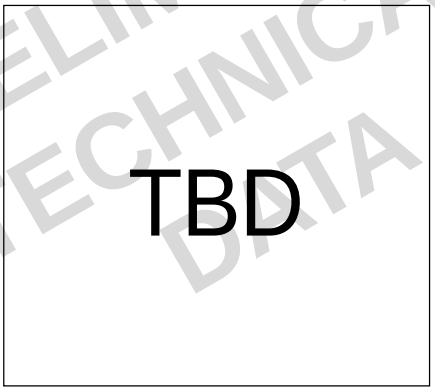


Figure 17. Power-Down Current vs. Supply Voltage

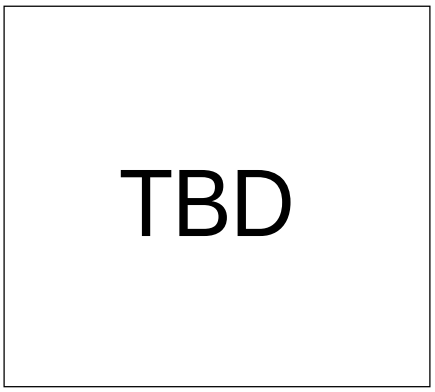


Figure 18. Supply Current vs. Logic Input Voltage

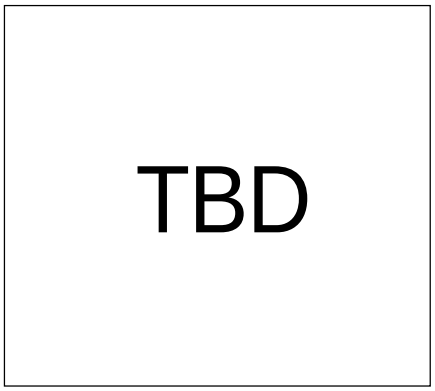


Figure 18. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

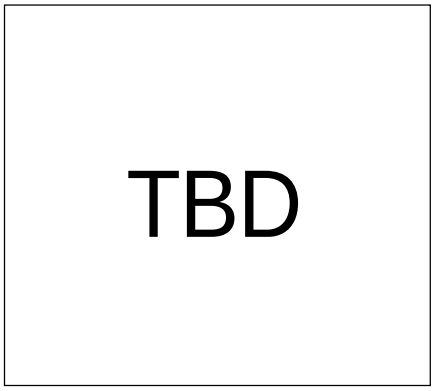


Figure 20. Power-On Reset to 0V

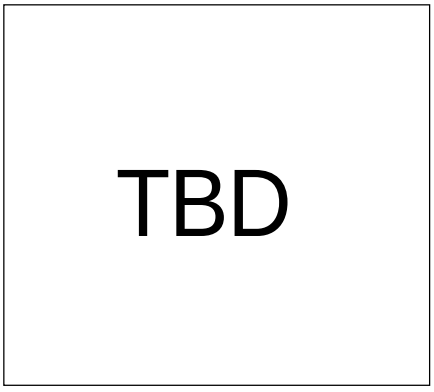


Figure 21. Exiting Power-Down to Mid-Scale

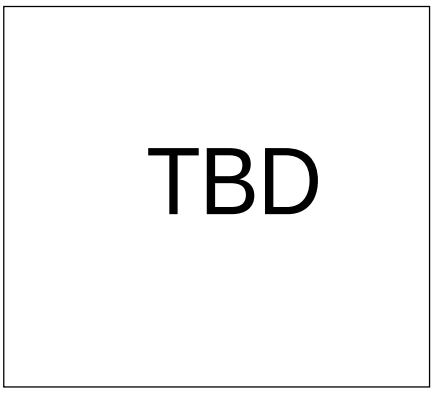


Figure 22. I_{DD} Histogram with V_{DD} = +3 V and V_{DD} = +5 V

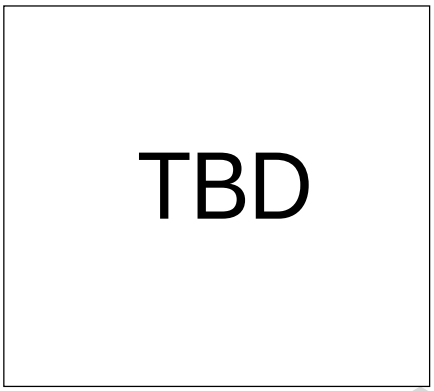


Figure 23. AD5326 Major-Code Transition Glitch Energy

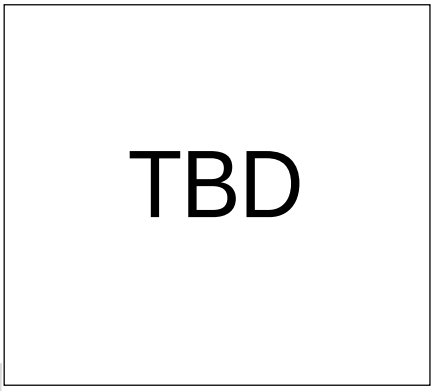


Figure 24. Multiplying Bandwidth (Small-Signal Frequency Response)

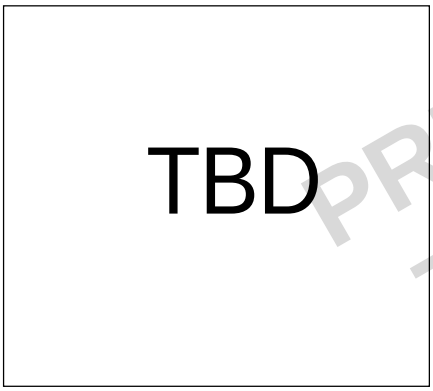


Figure 25. Full-Scale Error vs. V_{REF}

Figure 26. DAC-DAC Crosstalk

FUNCTIONAL DESCRIPTION

The AD5306/AD5316/AD5326 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10 and 12 bits respectively. Each contains four output buffer amplifiers and is written to via a 2-wire serial interface. They operate from single supplies of +2.5V to +5.5V and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7V/µs. Each DAC is provided with a separate reference input, which may be buffered to draw virtually no current from the reference source, or unbuffered to give a reference input range from 0.25 V to V_{DD}. The devices have a power-down mode, in which all DACs may be turned off completely with a high-impedance output.

Digital-to-Analog Section

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the corresponding DAC. Figure 27 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = \frac{V_{REF} * D}{2^N}$$

where D=decimal equivalent of the binary code which is loaded to the DAC register;

0-255 for AD5306 (8-bits)
0-1023 for AD5316 (10-bits)
0-4095 for AD5326 (12-bits)

N = DAC resolution

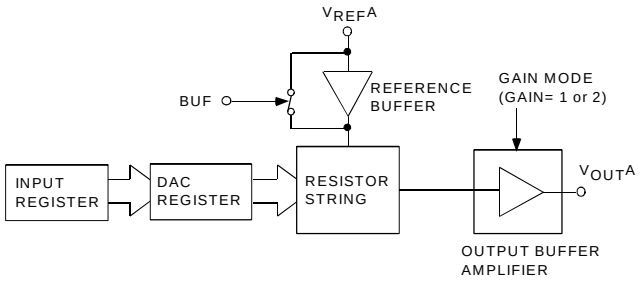


Figure 27. Single DAC channel architecture

Resistor String

The resistor string section is shown in Figure 28. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

DAC Reference Inputs

There is a reference pin for each of the four DACs. The reference inputs are buffered but can also be individually configured as unbuffered. The advantage with the buffered input is the high impedance it presents to the voltage source driving it. However if the unbuffered mode is used, the user can have a reference voltage as low as 0.25 V and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier.

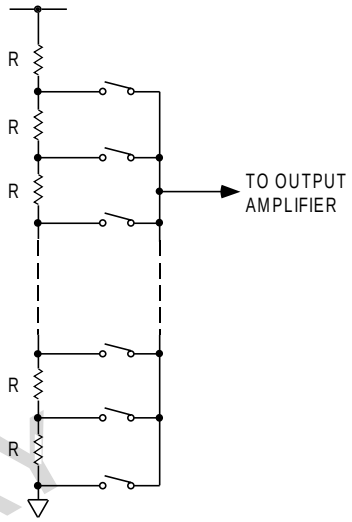


Figure 28. Resistor String

If there is a buffered reference in the circuit (e.g., REF192), there is no need to use the on-chip buffers of the AD5306/AD5316/AD5326. In unbuffered mode the input impedance is still large at typically 180 kΩ per reference input for 0-V_{REF} mode and 90 kΩ for 0-2V_{REF} mode.

The buffered/unbuffered option is controlled by the BUF bit in the Control Byte. The BUF bit setting applies to whichever DAC is selected in the Pointer Byte.

Output Amplifier

The output buffer amplifier is capable of generating output voltages to within 1mV of either rail. Its actual range depends on the value of the V_{REF}, GAIN and offset error. If a gain of 1 is selected (GAIN=0) the output range is 0.001 V to V_{REF}.
If a gain of 2 is selected (GAIN=1) the output range is 0.001 V to 2V_{REF}. However because of clamping the maximum output is limited to V_{DD} - 0.001V.

The output amplifier is capable of driving a load of 2kΩ to GND or $V_{DD,}$ in parallel with 500pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in the plot in Figure 14.

The slew rate is 0.7V/µs with a half-scale settling time to +/-0.5 LSB (at 8 bits) of 6ms.

POWER-ON RESET

The AD5306/AD5316/AD5326 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal operation
- Reference inputs unbuffered.
- 0-V_{REF} output range.
- Output voltage set to 0V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering-up.

SERIAL INTERFACE

The AD5306/AD5316/AD5326 are controlled via an I^2C-compatible serial bus. These devices are connected to this bus as slave devices (i.e. no clock is generated by the AD5306/AD5316/AD5326 DACs). This interface is SMBus-Compatible at V_{DD} < 3.6 V

The AD5306/AD5316/AD5326 has a 7-bit slave address. The 5 MSBs are 00011 and the two LSB's are determined by the state of the A0 and A1 pins. The facility to make hardwired changes to A0 and A1 allows the user to have up to four of these devices on one bus.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition which is when a high to low transition on the SDA line occurs while SCL is high. The following byte is the address byte which consists of the 7-bit slave address followed by a R/$\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

The slave whose address corresponds to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written or read from it's shift register.

2. Data is transmitted over the serial bus in sequences of 9 clock pulses (8 data bits followed by an Acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a STOP condition is established. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the 9th clock pulse (i.e. the SDA line remains high). The master will then bring the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a STOP condition.

Read/Write Sequence

In the case of the AD5306/AD5316/AD5326, all write access sequences and most read sequences begin with the device address (with R/$\overline{W}$ = 0) followed by the pointer byte. This pointer byte specifies the data format and determines which DAC is being accessed in the subsequent read/write operation. See Figure 29. In a write operation the data follows immediately. In a read operation the address is resent with R/$\overline{W}$ = 1 and then the data is read back. However it is also possible to perform a read operation by sending only the address with R/$\overline{W}$ = 1. The previously loaded pointer settings are then used for the readback operation.

MSB LSB

X	X	RIGHT/$\overline{\text{LEFT}}$	SINGLE/$\overline{\text{DOUBLE}}$	DACD	DACC	DACB	DACA

Figure 29. Pointer Byte

Pointer Byte Bits

The following is an explanation of the individual bits which make up the Pointer Byte.

X: Don't Care Bits

RIGHT/$\overline{\text{LEFT}}$:
0: Data written to the device and read from the device is Left-Justified (in Double Byte mode)
1: Data written to the device and read from the device is Right-Justified (in Double Byte mode)

SINGLE/$\overline{\text{DOUBLE}}$:
0: Data Write and Readback are done as 2-byte write/read sequences
1: Data Write and Readback are done as 1-byte (most significant 8 bits only) write/read sequences

DACD: 1: The following data bytes are for DAC D

DACC: 1: The following data bytes are for DAC C

DACB: 1: The following data bytes are for DAC B

DACA: 1: The following data bytes are for DAC A

Input Shift Register

The input shift register is 16-bits wide. Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1 on page 4. The 16-bit word consists of four control bits followed by 8, 10 or 12 bits of DAC data, depending on the device type. The first bits loaded are the control bits - GAIN, BUF, $\overline{\text{CLR}}$ and $\overline{\text{PD}}$. The remaining bits are left- or right-justified DAC data bits, starting with the MSB. See Figure 30.

GAIN: 0: Output range for that DAC set at 0-V_{REF}
1: Output range for that DAC set at 0-2V_{REF}

BUF: 0: Reference Input for that DAC is unbuffered
1: Reference Input for that DAC is buffered

$\overline{\text{CLR}}$: 0: All DAC registers and input registers are filled with zeros on completion of the write sequence.
1:Normal operation.

$\overline{\text{PD}}$: 0: On completion of the write sequence all four DACs go into Power-Down mode. The DAC outputs enter a high-impedance state.
1:Normal operation.

Default Readback Conditions

All Pointer Byte bits power-up to 0. Therefore, if user initiates a readback without writing to the pointer byte first, no single DAC channel has been specified. In this case, the default readback bits are all 0 except for the $\overline{\text{CLR}}$ bit which is a 1.

Multiple-DAC write sequence

Because there are individual bits in the Pointer Byte for each DAC, it is possible to write the same data and control bits to 2, 3 or 4 DACs simultaneously by setting the relevant bits to 1.

Multiple-DAC readback sequence

If the user attempts to readback data from more than 1 DAC at a time, the part will readback the default, power-on-reset conditions for a double-byte readback i.e. all 0s except for $\overline{\text{CLR}}$ which is 1. For a single-byte readback, the part will readback all 0s.

LEFT-JUSTIFIED DATA BYTES (WRITE AND READBACK)

MOST SIGNIFICANT DATA BYTE

MSB — *8-bit AD5306* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	D7	D6	D5	D4

MSB — *10-bit AD5316* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	D9	D8	D7	D6

MSB — *12-bit AD5326* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	D11	D10	D9	D8

LEAST SIGNIFICANT DATA BYTE

MSB — *8-bit AD5306* — LSB

D3	D2	D1	D0	X	X	X	X

MSB — *10-bit AD5316* — LSB

D5	D4	D3	D2	D1	D0	X	X

MSB — *12-bit AD5326* — LSB

D7	D6	D5	D4	D3	D2	D1	D0

RIGHT-JUSTIFIED DATA BYTES (WRITE AND READBACK)

MOST SIGNIFICANT DATA BYTE

MSB — *8-bit AD5306* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	X	X	X	X

MSB — *10-bit AD5316* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	X	X	D9	D8

MSB — *12-bit AD5326* — LSB

GAIN	BUF	$\overline{CLR}$	$\overline{PD}$	D11	D10	D9	D8

LEAST SIGNIFICANT DATA BYTE

MSB — *8-bit AD5306* — LSB

D7	D6	D5	D4	D3	D2	D1	D0

MSB — *10-bit AD5316* — LSB

D7	D6	D5	D4	D3	D2	D1	D0

MSB — *12-bit AD5326* — LSB

D7	D6	D5	D4	D3	D2	D1	D0

SINGLE BYTE ONLY (WRITE AND READBACK)

MSB — *8-bit AD5306* — LSB

D7	D6	D5	D4	D3	D2	D1	D0

MSB — *10-bit AD5316* — LSB

D9	D8	D7	D6	D5	D4	D3	D2

MSB — *12-bit AD5326* — LSB

D11	D10	D9	D8	D7	D6	D5	D4

Figure 30. Double- and Single-Byte Data formats

WRITE OPERATION

When writing to the AD5306/AD5316/AD5326 DACs, the user must begin with an address byte (R/$\overline{W}$ = 0) after which the DAC will Acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the pointer byte which is also acknowledged by the DAC. Depending on the value of SINGLE/$\overline{DOUBLE}$ one or two bytes of data are then written to the DAC as shown in Figure 31 below. A STOP condition follows.

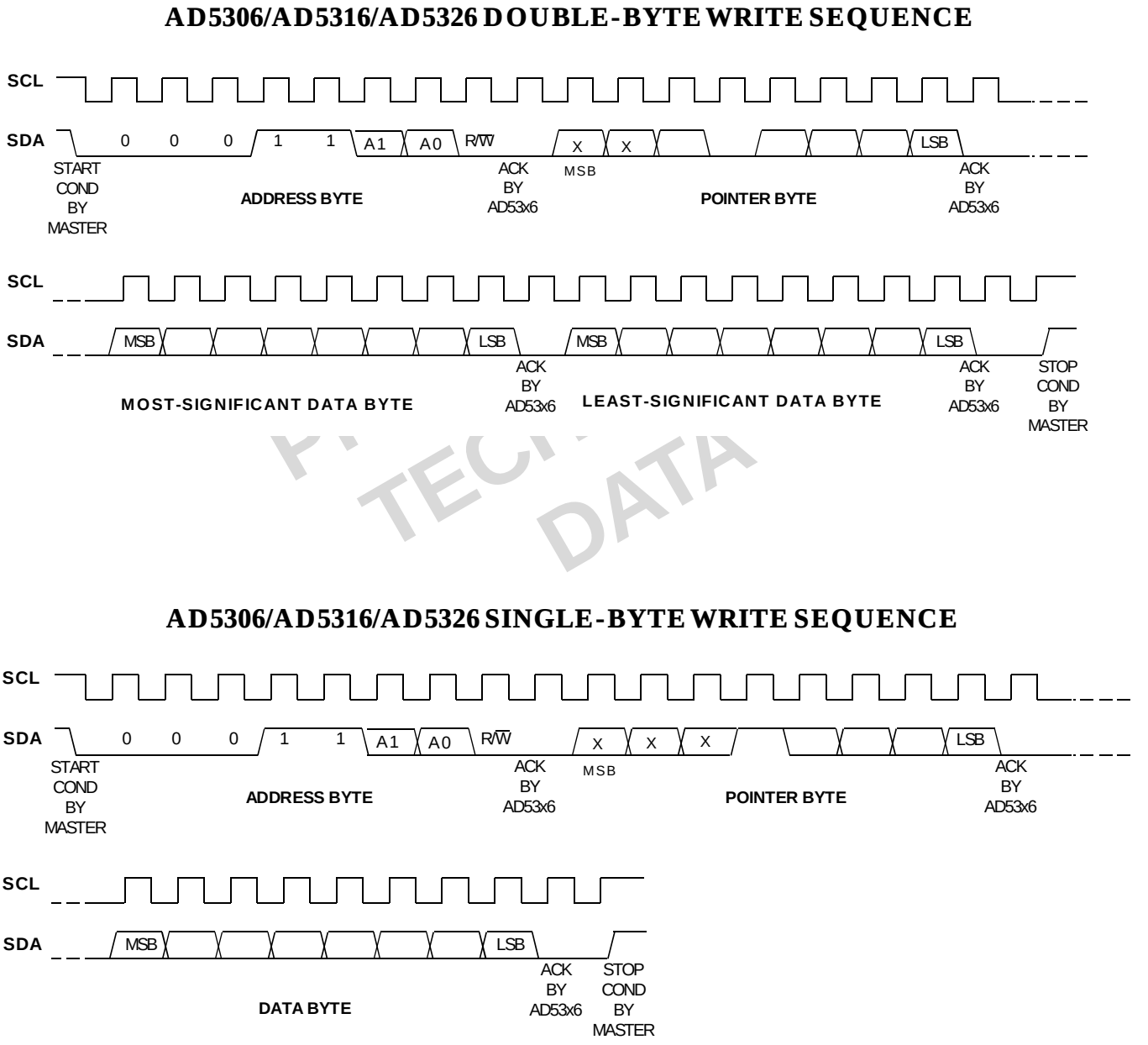


Figure 31. Double- and Single-Byte Write Sequences

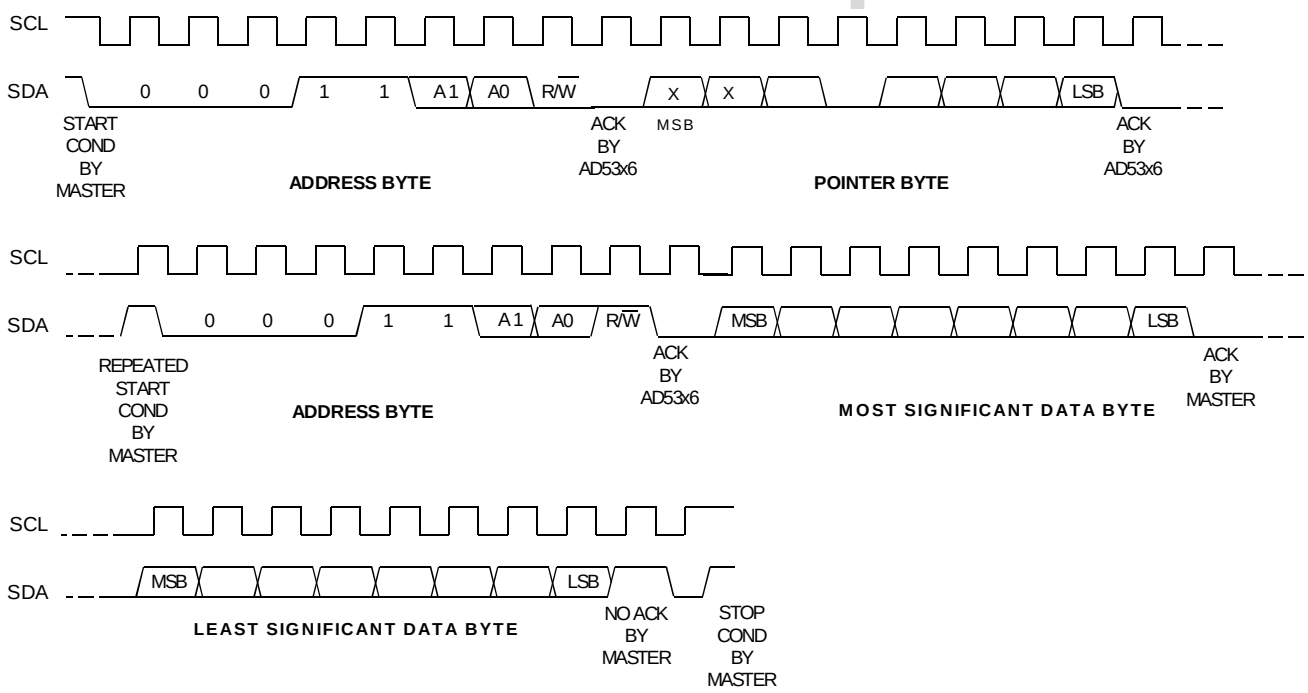
READ OPERATION

When reading data back from the AD5306/AD5316/ AD5326 DACs, the user begins with an address byte (R/$\overline{W}$ = 0) after which the DAC will Acknowledge that it is prepared to receive data by pulling SDA low. This address byte is usually followed by the pointer byte which is also acknowledged by the DAC. Following this there is a repeated start condition by the master and the address is resent with R/$\overline{W}$ = 1. This is acknowledged by the DAC indicating that it is prepared to transmit data. Depending on the value of SINGLE/$\overline{DOUBLE}$, one or two bytes of data are then read from the DAC as shown in Figure 32 below. A STOP condition follows.

However, if the master sends an ACK and continues clocking SCL (no STOP is sent), the DAC will re-transmit the same one or two bytes of data on SDA. This allows continuous readback of data from the selected DAC register.

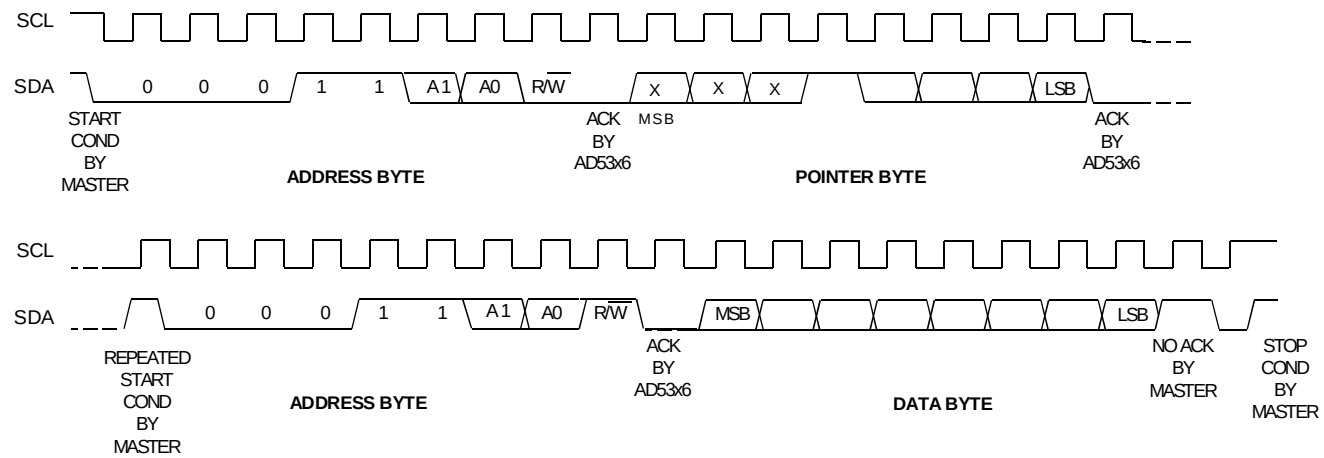
Alternatively the user may send a START followed by the address with R/$\overline{W}$ = 1. In this case the previously loaded pointer settings are used and readback of data can commence immediately.

AD5306/AD5316/AD5326 DOUBLE-BYTE READBACK SEQUENCE*



*Data Bytes same as those on page 13 (double-byte write sequence) except Don't Cares are read back as 0s

AD5306/AD5316/AD5326 SINGLE-BYTE READBACK SEQUENCE*



*Data Bytes same as those on page 13 (single-byte write sequence)

Figure 32. Double- and Single-Byte Read Sequences

DOUBLE-BUFFERED INTERFACE

The AD5306/AD5316/AD5326 DACs all have double-buffered interfaces consisting of two banks of registers - input registers and DAC registers. The input register is connected directly to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code which the resistor string uses.

Access to the DAC register is controlled by the $\overline{\text{LDAC}}$ pin. When $\overline{\text{LDAC}}$ is high, the DAC register is latched and hence the input register may change state without affecting the contents of the DAC register. However, when $\overline{\text{LDAC}}$ is brought low, the DAC register become transparent and the contents of the input register are transferred to it.

This is useful if the user requires simultaneous updating of all DAC outputs. The user may write to each of the input registers individually and then, by pulsing the $\overline{\text{LDAC}}$ input low, all outputs will update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{\text{LDAC}}$ was set low. Normally, when $\overline{\text{LDAC}}$ is low, the DAC registers are filled with the contents of the input registers. In the case of the AD5306/AD5316/AD5326, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated thereby removing unnecessary digital crosstalk.

POWER-DOWN MODES

The AD5306/AD5316/AD5326 have very low power consumption, dissipating typically 1.5mW with a 3V supply and 3mW with a 5V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is selected by a zero on Bit 12 ($\overline{\text{PD}}$) of the data word.

When the $\overline{\text{PD}}$ bit is set to 1 all DACs work normally with a typical power consumption of 600µA at 5V (500µA at 3V). However, in power-down mode, the supply current falls to 200nA at 5V (80nA at 3V) when all DACs are powered-down. Not only does the supply current drop but the output stage is also internally switched from the output of the amplifier making it open-circuit. This has the advantage that the output is three-state while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure 33.

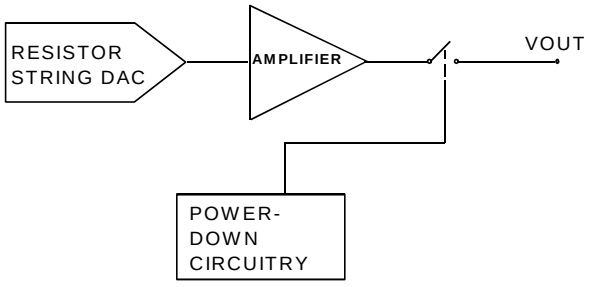


Figure 33. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5µs for V_{DD}=5V and 5µs when V_{DD}=3V. This is the time from the falling edge of the 16th SCLK pulse to when the output voltage deviates from it's power-down voltage. See Figure 21.

APPLICATIONS

Typical Application Circuit

The AD5306/AD5316/AD5326 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0V to V_{DD}. More typically, these devices are used with a fixed, precision reference voltage. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference would be the AD589, a 1.23 V bandgap reference. Figure 34 shows a typical setup for the AD5306/AD5316/AD5326 when using an external reference. Note that A0 and A1 can be high or low.

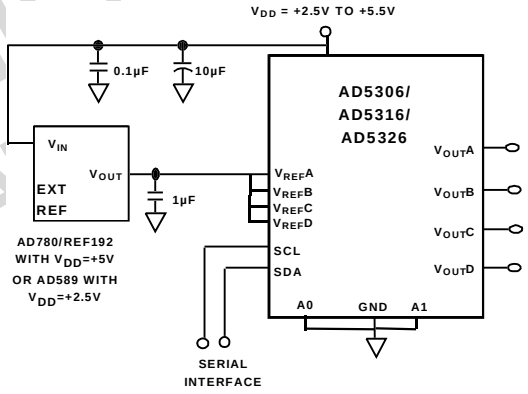


Figure 34. AD5306/AD5316/AD5326 using a 2.5V External Reference

Driving V_{DD} from the Reference Voltage

If an output range of 0V to V_{DD} is required when the reference inputs are configured as unbuffered, then the simplest solution is to connect the reference inputs to V_{DD}. As this supply may not be very accurate and may be noisy, the AD5306/AD5316/AD5326 may be powered from the reference voltage; for example using a 5V reference such as the REF195. The REF195 will output a steady supply voltage for the AD5306/AD5316/AD5326. The typical current required from the REF195 is 600µA supply current and approximately 112µA into the reference inputs (if unbuffered). This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10kW load on each output) is:

$$712\mu A + 4(5V/10k\Omega) = 2.7mA$$

The load regulation of the REF195 is typically 2ppm/mA which results in an error of 5.4ppm (27µV) for the 2.7mA current drawn from it. This corresponds to a 0.0014 LSB error at 8-bits and 0.022 LSB error at 12-bits.

Bipolar Operation Using the AD5306/AD5316/AD5326

The AD5306/AD5316/AD5326 have been designed for single-supply operation but a bipolar output range is also possible using the circuit in Figure 35. The circuit below will give an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

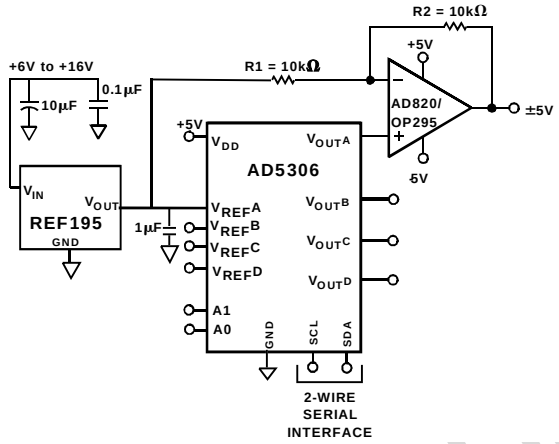


Figure 35. Bipolar Operation with the AD5306

The output voltage for any input code can be calculated as follows:

$V_{OUT} = [(REFIN \times (D/2^N) \times (R1+R2)/R1) - REFIN \times (R2/R1)]$

where D is the decimal equivalent of the code loaded to the DAC.

N is the DAC resolution.

REFIN is the reference voltage input

With REFIN = 5V, R1 = R2 = 10 kΩ :

$V_{OUT} = (10 \times D/2^N) - 5\ V$

Multiple devices on one bus

Figure 36 below shows four AD5306 devices on the same serial bus. Each has a different slave address since the states of the A0 and A1 pins are different. This allows each of sixteen DACs to be written to or read from independently.

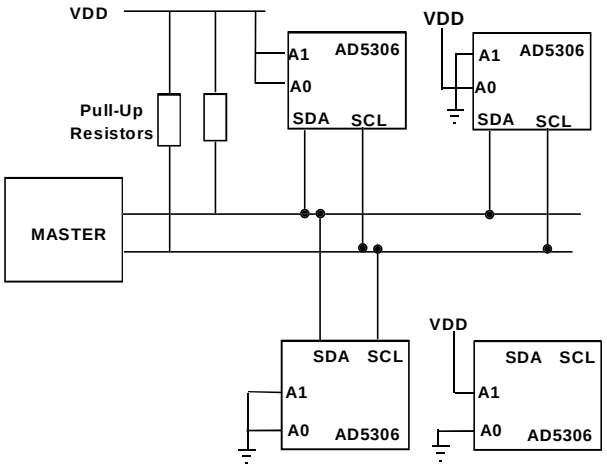


Figure 36. Multiple AD5306 devices on one bus.

AD5306/AD5316/AD5326 as a Digitally Programmable Window Detector

A digitally programmable upper/lower limit detector using two of the DACs in the AD5306/AD5316/AD5326 is shown in Figure 37. The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, a LED will indicate the fail condition. Similarly DACs C and D can be used for window detection on a second V_{IN} signal.

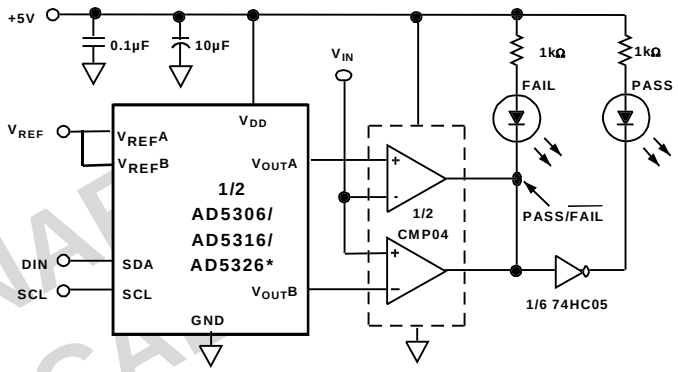


Figure 37. Window detection

Coarse and Fine Adjustment Using the AD5306/AD5316/AD5326

Two of the DACs in the AD5306/AD5316/AD5326 can be paired together to form a coarse and fine adjustment function, as shown in Figure 38. DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 will change the relative effect of the coarse and fine adjustments. With the resistor values and external reference shown the output amplifier has unity gain for the DAC A output, so the output range is 0V to 2.5V - 1 LSB. For DAC B the amplifier has a gain of 7.6 x 10^{-3}, giving DAC B a range equal to 19mV. Similarly DACs C and D can be paired together for coarse and fine adjustment.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} may be used. The op-amps indicated will allow a rail-to-rail output swing.

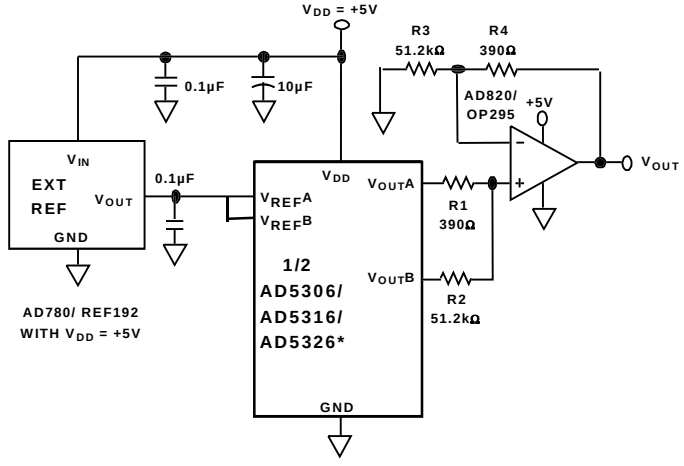


Figure 38. Coarse/Fine Adjustment.

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5306/AD5316/AD5326 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the AD5306/AD5316/AD5326 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. The AD5306/AD5316/AD5326 should have ample supply bypassing of 10µF in parallel with 0.1µF on the supply located as close to the package as possible, ideally right up against the device. The 10µF capacitors are the tantalum bead type. The 0.1µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5306/AD5316/AD5326 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the SDA and SCL lines will help reduce crosstalk between them (not required on a multilayer board as there will be a separate ground plane, but separating the lines will help).

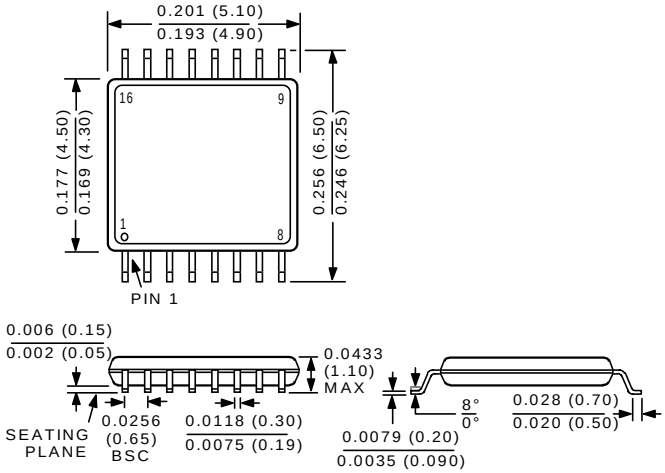
Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Thin Shrink Small Outline Package (TSSOP)

(RU-16)



OVERVIEW OF AD53xx SERIAL DEVICES

Part no.	Resolution	No. of DACS	DNL	Interface	Settling Time	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI	4 µs	SOT-23, MicroSOIC	6,8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23, MicroSOIC	6,8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23, MicroSOIC	6,8
AD5301	8	1	±0.25	2-wire	6 µs	SOT-23, MicroSOIC	6,8
AD5311	10	1	±0.5	2-wire	7 µs	SOT-23, MicroSOIC	6,8
AD5321	12	1	±1.0	2-wire	8 µs	SOT-23, MicroSOIC	6,8
DUALS							
AD5302	8	2	±0.25	SPI	6 µs	MicroSOIC	8
AD5312	10	2	±0.5	SPI	7 µs	MicroSOIC	8
AD5322	12	2	±1.0	SPI	8 µs	MicroSOIC	8
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
QUADS							
AD5304	8	4	±0.25	SPI	6 µs	MicroSOIC	10
AD5314	10	4	±0.5	SPI	7 µs	MicroSOIC	10
AD5324	12	4	±1.0	SPI	8 µs	MicroSOIC	10
AD5305	8	4	±0.25	2-wire	6 µs	MicroSOIC	10
AD5315	10	4	±0.5	2-wire	7 µs	MicroSOIC	10
AD5325	12	4	±1.0	2-wire	8 µs	MicroSOIC	10
AD5306	8	4	±0.25	2-wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16

Visit our web-page at http://www.analog.com/support/standard_linear/selection_guides/AD53xx.html