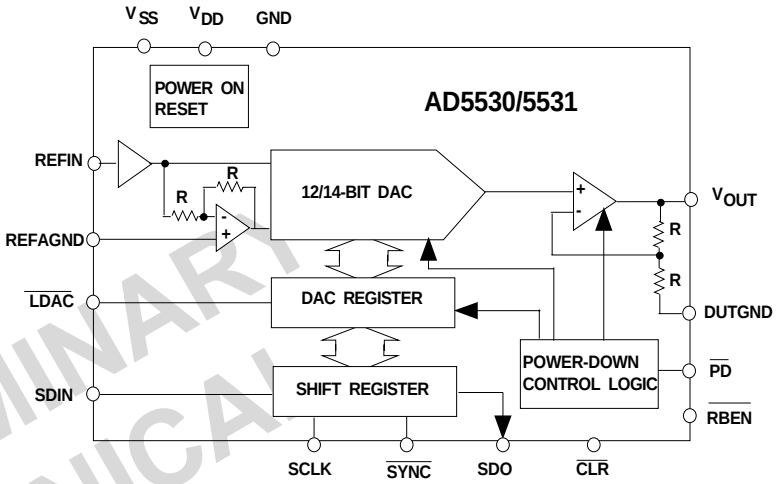
Serial Input Voltage Output, 12/14 Bit DACs

Preliminary Technical Data — AD5530/AD5531

FEATURES
Pin Compatible 12 and 14 Bit DACs
Serial Input, Voltage Output
Maximum Output Voltage Range of ±10V
Data Readback
Clear Function to a User Defined Voltage
Power Down Function
Power On Reset
Serial Data Output for Daisy Chaining

APPLICATIONS
Industrial Automation
Automatic Test Equipment
Process Control
General Purpose Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5530 and AD5531 are single 12/14 bit serial input, voltage output DAC's respectively.

They utilize a versatile three-wire interface that is compatible with SPI™, QSPI™, MICROWIRE™ and DSP interface standards. Data is presented to the part in the format of a sixteen bit serial word. Serial data is available on the SDO pin for daisy chaing purposes. Data Readback allows the user to read the contents of the DAC register via the SDO pin.

Upon power up, the DAC register is loaded with midscale, (800H for the AD5530, and 2000H for the AD5531).

The DAC output is buffered by a gain of two amplifier and referenced to the potential at DUTGND. $\overline{\text{LDAC}}$ may be used to update the output of the DAC. A Power Down ($\overline{\text{PD}}$) pin allows the DAC to be put into a low power state, and a $\overline{\text{CLR}}$ pin allows the output to be cleared to a user defined voltage, the potential at DUTGND.

The AD5530 and AD5531 are available in a 16 lead TSSOP package.

PRODUCT HIGHLIGHTS

1. 12/14 Bit Pin Compatible DAC's.
2. Bipolar Voltage Output up to ±10V.
3. Data Readback Capability.
4. Three Wire Serial Interface.
5. Power On Reset Circuitry, midscale is loaded to the DAC.
6. Daisy Chaining mode.
7. Small 16 lead TSSOP package.

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MICROWIRE is a trademark of National Semiconductor Corporation.

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AD5530/AD5531–SPECIFICATIONS[1] (V_{DD} = +12 V ±5% or +15 V ±10%; V_{SS} = -12 V ±5% or -15 V ±10%; GND = 0 V; R_L = 5 kΩ and C_L = 220 pF to GND, All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD5530	AD5531	Units	Test Conditions/Comments
ACCURACY				
Resolution	12	14	Bits	
Relative Accuracy	±1	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic Over Temperature
Zero-Scale Error	±2	±8	LSB max	Typically within ±1 LSB
Full-Scale Error	±2	±8	LSB max	Typically within ±1 LSB
Gain Error	±1	±8	LSB typ	
Gain Temperature Coefficient[2]	20	20	ppm FSR/°C typ	
	40	40	ppm FSR/°C max	
REFERENCE INPUTS[2]				
Reference Input Range	0/5	0/5	V min/V max	Max output range ±10V
DC Input Resistance	100	100	MΩ typ	
Input Current	±1	±1	µA max	Per Input. Typically ±20 nA
DUTGND INPUT[2]				
DC Input Impedance	60	60	kΩ typ	
Max Input Current	±0.3	±0.3	mA typ	
Input Range	-5/+5	-5/+5	V min/V max	Max output range ±10V
O/P CHARACTERISTICS				
Output Voltage Swing	±10	±10	V max	
Short Circuit Current[2]	15	15	mA max	
Resistive Load	5	5	kΩ min	To 0 V
Capacitive Load	220	220	pF max	To 0 V
DC Output Impedance[2]	0.5	0.5	Ω max	
DIGITAL INPUTS				
V_{INH}, Input High Voltage	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	µA max	Total for All Pins
C_{IN}, Input Capacitance[2]	10	10	pF max	
POWER REQUIREMENTS				
V_{DD}/V_{SS}	+12/-12	+12/-12	V nom	±5% For Specified Performance
V_{DD}/V_{SS}	+15/-15	+15/-15	V nom	±10% For Specified Performance
Power Supply Sensitivity				
ΔFull Scale/ΔV_{DD}	110	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	100	dB typ	
I_{DD}	2	2	mA max	Outputs Unloaded. I_{DD} in power down < 50µA
I_{SS}	2	2	mA max	Outputs Unloaded.

NOTES
[1]Temperature range for B Version: –40°C to +85°C.
[2]Guaranteed by design.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS[1]

(V_{DD} = +12 V ±5% or +15 V ±10%; V_{SS} = -12 V ±5% or -15 V ±10%; GND = 0 V; R_L = 5 kΩ and C_L = 220 pF to GND, All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time	20	µs typ	Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	1.5	V/µs typ	
Digital-to-Analog Glitch Impulse	120	nV-s typ	DAC Latch Alternately Loaded with 0FFF Hex and 1000 Hex. Not Dependent on Load Conditions
Digital Feedthrough	0.5	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density			
@ 1 kHz	130	nV/(Hz)$^{1/2}$typ	All 1s Loaded to DAC.

NOTES
[1]Specifications subject to change without notice. Guaranteed by design, not subject to production test.

TIMING CHARACTERISTICS[1,2]

(V_{DD} = +12 V ±5% or +15 V ±10%; V_{SS} = -12 V ±5% or -15 V ±10%; GND = 0 V; R_L = 5 kΩ and C_L = 220 pF to GND, All specifications T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
t_1	100	ns min	SCLK cycle time
t_2	40	ns min	SCLK low time
t_3	60	ns min	SCLK high time
t_4	40	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	40	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	30	ns min	Data setup time
t_7	10	ns min	Data hold time
t_8	0	ns min	$\overline{SYNC}$ high to $\overline{LDAC}$ low
t_9	40	ns min	$\overline{LDAC}$ pulse width
t_{10}	0	ns min	$\overline{LDAC}$ high to $\overline{SYNC}$ low
t_{11}	40	ns min	$\overline{CLR}$ pulse width
t_{12}	30	ns min	SDO data setup time for next device
t_{13}	10	ns min	SDO data hold time for next device
t_{14}	40	ns min	$\overline{RBEN}$ to SCLK falling edge setup time
t_{15}	20	ns min	$\overline{RBEN}$ hold time
t_{16}	40	ns min	$\overline{RBEN}$ falling edge to SDO valid

[1]Guaranteed by design. Not production tested.

[2]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.

Specifications subject to change without notice.

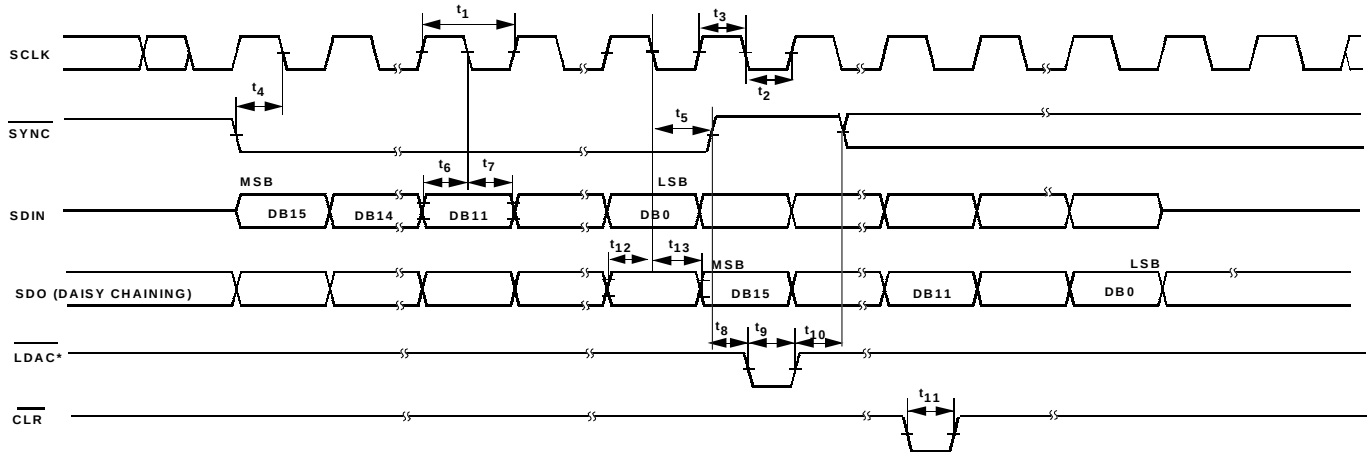


Figure 1. Timing Diagram for Stand Alone Mode and Daisy Chain Mode

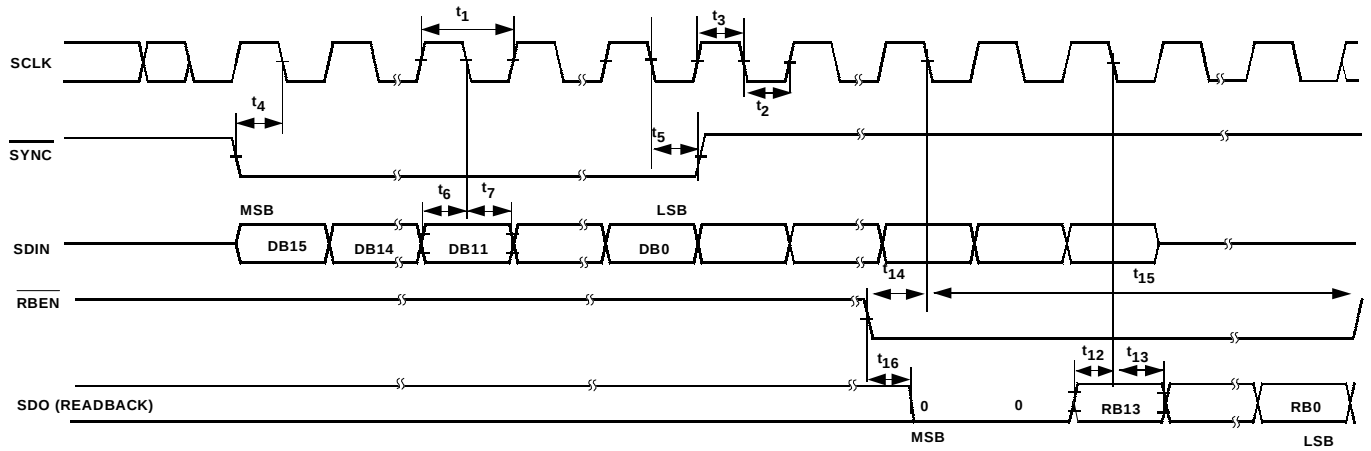


Figure 2. Timing Diagram for Readback

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	–0.3 V, +17 V
V_{SS} to GND	+0.3 V, -17 V
Digital Inputs to GND	-0.3V to +17 V +0.3 V
REFIN to REFAGND	-0.3V, +17 V
REFIN to GND	V_{SS} - 0.3V, V_{DD} + 0.3V
REFAGND to GND	V_{SS} - 0.3V, V_{DD} + 0.3V
DUTGND to GND	V_{SS} - 0.3V, V_{DD} + 0.3V
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature, (T_J max)	+150°C
Package Power Dissipation	(T_J max – T_A)/θ_{JA}
Thermal Impedance θ_{JA}	
TSSOP(RU-16)	150.4°C/W
Lead Temperature (Soldering 10s)	300°C
IR Reflow, Peak Temperature	220°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

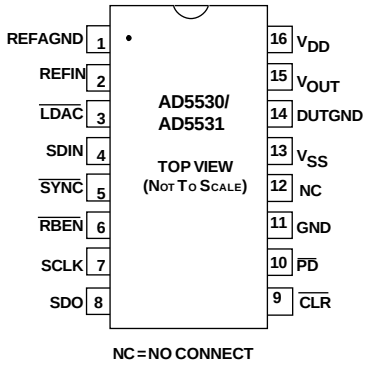
Model	Temperature Range	INL (LSBs)	DNL(LSBs)	Package Option*
AD5530BRU	-40 °C to +85 °C	±1	±1	RU-16
AD5531BRU	-40 °C to +85 °C	±2	±1	RU-16

*RU = Thin Shrink Small Outline Package.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5530/5531 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESDprecautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION
16 Lead TSSOP



NC = NO CONNECT

AD5530/AD5531 PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	REFAGND	For bipolar ±10 V output range, this pin should be tied to 0V.
2	REFIN	This is the voltage reference input for the DAC. Connect to external +5V reference for specified bipolar ±10 V output.
3	$\overline{LDAC}$	Load DAC logic input (acitve low). When taken low, the contents of the shift register is transferred to the DAC register. $\overline{LDAC}$ may be tied permanently low enabling the outputs to be updated on the rising edge of $\overline{SYNC}$.
4	SDIN	Serial data input. This device accepts 16-bit words. Data is clocked into the input register on the falling edge of SCLK.
5	$\overline{SYNC}$	Logic Input signal used to frame the serial data input.
6	$\overline{RBEN}$	Readback enable function. This function allows the contents of the DAC register to be read. Data from the DAC register will be shifted out on SDO pin on each rising edge of SCLK.
7	SCLK	Clock input. Data is clocked into the input register on the falling edge of SCLK.
8	SDO	Serial Data out. This pin is used to clock out the serial data previously written to the input shift register or may be used in conjunction with $\overline{RBEN}$ to read back the data from the DAC register. This is an open drain output, it should be pulled high with an external pull up resistor. In stand alone mode, SDO should be tied to GND or left high impedance.
9	$\overline{CLR}$	Level sensitive, active low input. A falling edge of $\overline{CLR}$ resets V_{OUT} to DUTGND. The contents of the registers are untouched. When $\overline{CLR}$ is brought high again, the DAC output reverts to the original output as determined by the data in the DAC register.
10	$\overline{PD}$	This allows the DAC to be put into a power down state.
11	GND	Ground reference.
12	NC	Do not connect anything to this pin.
13	V_{SS}	Negative analog supply voltage, -12 V ±5% or -15 V ±10% for specified performance.
14	DUTGND	V_{OUT} is referenced to the voltage applied to this pin.
15	V_{OUT}	DAC output.
16	V_{DD}	Positive analog supply voltage, +12 V ±5% or +15 V ±10% for specified performance.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Zero Scale Error
Zero code error is a measure of the output error when all 0s are loaded to the DAC latch.

Full Scale Error
This is the error in DAC output voltage when all 1s are loaded into the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be 2 V_{REF} - 1 LSB.

Output Voltage Settling time
This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse
Digital-to-Analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

TYPICAL PERFORMANCE CHARACTERISTICS

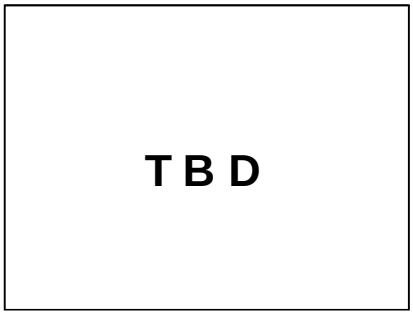


Figure 3 . Typical INL Plot

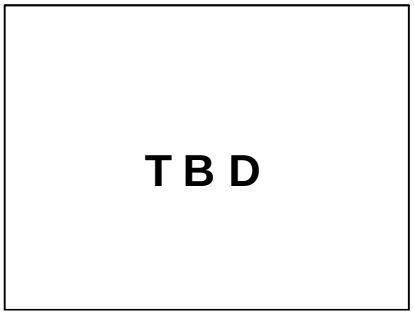


Figure 4. Typical DNL Plot

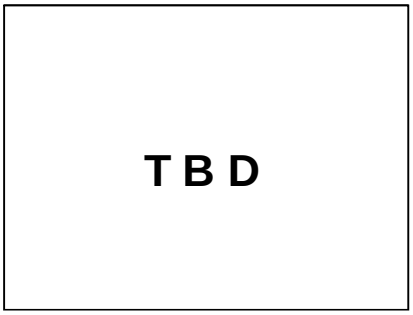


Figure 5. Typical INL Error vs. Temperature

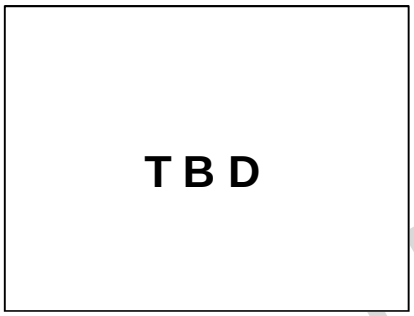


Figure 6. Typical DNL error vs. Temperature

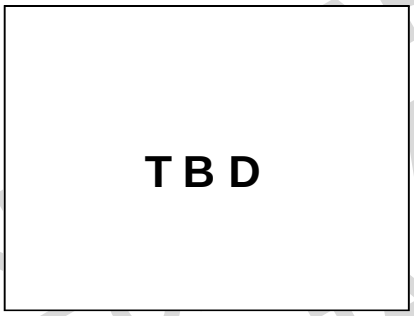


Figure 7. Zero Scale and Full Scale Error vs. Temperature

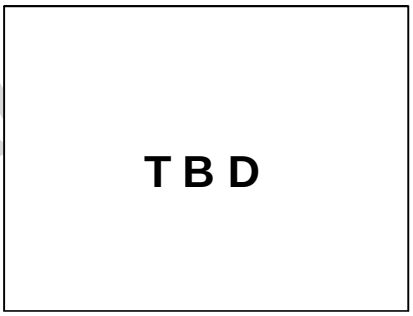


Figure 8. Typical Digital to Analog Glitch Impulse

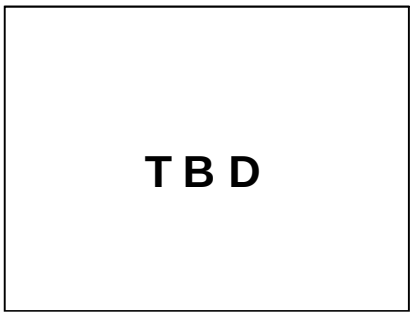


Figure 9. Settling Time

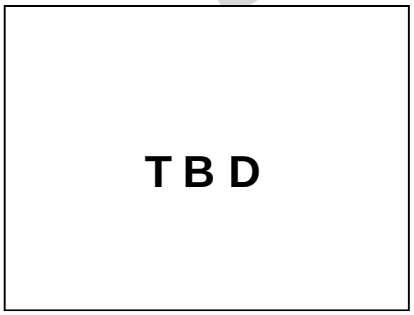


Figure 10. I_{DD}, I_{SS} vs. Temperature

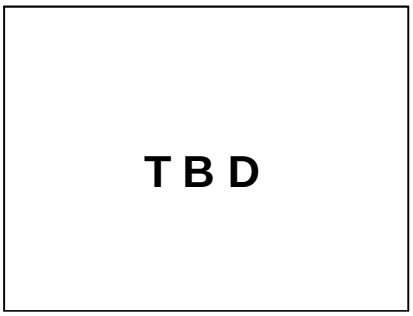


Figure 11. Power On Reset

GENERAL DESCRIPTION

DAC Architecture

The AD5530/AD5531 are pin compatible 12/14 bit DACs. The AD5530 consists of a straight 12 bit R-2R voltage mode DAC, while the AD5531 consists of a 14 bit R-2R section. Using a +5 V reference connected to the REFIN pin and REFAGND tied to 0V, a bipolar ±10V voltage output results. The DAC coding is straight binary.

Serial Interface

Serial data on the SDIN input is loaded to the input register under the control of SCLK, $\overline{SYNC}$ and $\overline{LDAC}$. A write operation transfers a 16 bit word to the AD5530/ AD5531. Figure 1 and 2 show the timing diagrams. Figure 12 shows the contents of the input shift register. 12 or 14 bits of the serial word are data bits, the rest are don't cares. Upon power up, the input register and DAC register are loaded with midscale, (800H for the AD5530, and 2000H for the AD5531).

The serial word is framed by the signal, $\overline{SYNC}$. After a high to low transition on $\overline{SYNC}$, data is latched into the input shift register on the falling edges of SCLK. There are two ways in which the DAC register and output may be updated. The $\overline{LDAC}$ signal is examined on the falling edge of $\overline{SYNC}$, depending on its status, either a synchronous or asynchronous update is selected. If $\overline{LDAC}$ is low, then the DAC register and output are updated on the low to high transition of $\overline{SYNC}$. Alternatively, if $\overline{LDAC}$ is high upon sampling, the DAC register is not loaded with the new data on a rising edge of $\overline{SYNC}$. The contents of the DAC register and the output voltage will be updated by bringing $\overline{LDAC}$ low any time after the 16 bit data transfer is complete. $\overline{LDAC}$ may be tied permanently low if required. A simplified diagram of the input loading circuitry is illustrated in Figure 13.

Data written to the part via SDIN is available on the SDO pin 16 clocks later if the readback function is not used. SDO data is clocked out on the falling edge of the serial clock.

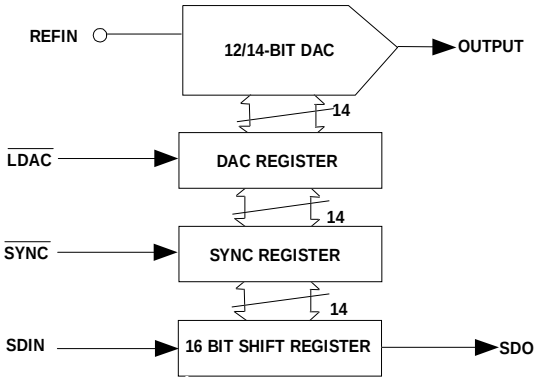


Figure 13. Simplified Serial Interface

READBACK Function

The AD5530/AD5531 allows the data contained in the DAC register to be read back if required. The pins involved are the $\overline{RBEN}$ and SDO (serial data out). $\overline{RBEN}$ is first asserted low, on the next falling edge of SCLK, while $\overline{RBEN}$ is still low, the contents of the DAC register are transferred to the shift register. $\overline{RBEN}$ may be used to frame the readback data by leaving it low for 16 clock cycles, or it may be asserted high after the required hold time. The shift register contains the DAC register data and this is shifted out on the SDO line on each falling edge of SCLK with some delay. This ensures the data on the serial data output pin is valid for the falling edge of the receiving part. The two MSBs of the 16-bit word will be '0's.

$\overline{CLR}$ function

The falling edge of $\overline{CLR}$ causes V_{OUT} to be reset to the same potential as DUTGND. The contents of the registers remain unchanged, so the user can reload the previous data with $\overline{LDAC}$ after $\overline{CLR}$ is asserted high. Alternatively, if $\overline{LDAC}$ is tied low, the output will be loaded with the contents of the DAC register automatically after $\overline{CLR}$ is brought high.

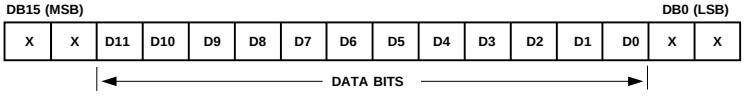


Figure 12a. AD5530 Input Shift register contents

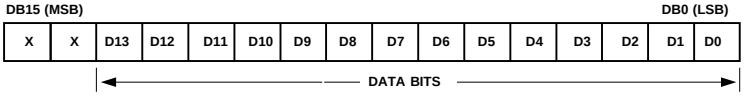


Figure 12b. AD5531 Input Shift register contents

Output Voltage
The DAC transfer function is as follows

$$V_{OUT} = 2[2*(REFIN - REFAGND)*D/2^N + 2*RefAGND - REFIN] - DUTGND$$

where :

D is the decimal data word loaded to the DAC register,
N is the resolution of the DAC.

Bipolar Configuration
Figure 14 shows the AD5530/AD5531 in a bipolar circuit configuration. REFIN is driven by the AD586, +5V reference, while the REFAGND and DUTGND pins are tied to GND. This results in a bipolar output voltage ranging from -10 V to +10 V. Resistor R1 is provided (if required) for gain adjust. Figure 15 shows the transfer function of the DAC when REFAGND is tied to 0V.

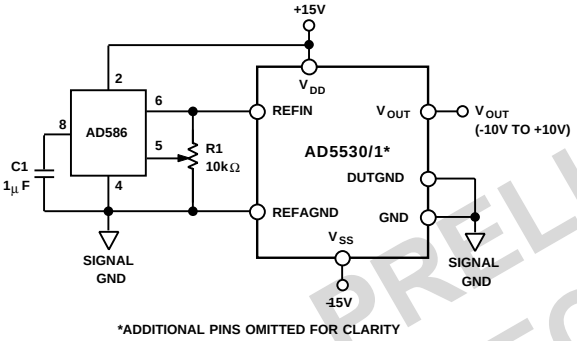


Figure 14. Bipolar +/-10 V operation.

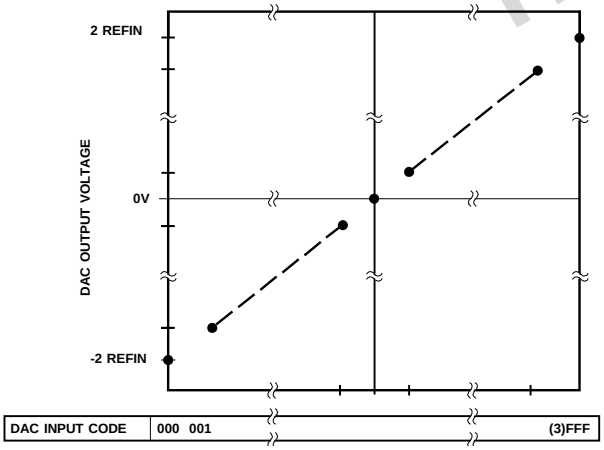


Figure 15. Output Voltage vs. DAC input codes (Hex).

CONTROLLED POWER-ON OF THE OUTPUT STAGE
A block diagram of the output stage of the AD5530/ AD5531 is shown in Figure 16. It is capable of driving a load of 5 kΩ in parallel with 220 pF. G_1 to G_6 are transmission gates that are used to control the power-on voltage present at V_{OUT}. On power up G_1 and G_2 are also used in conjunction with the $\overline{CLR}$ input to set V_{OUT} to the user defined voltage present at the DUTGND pin. When $\overline{CLR}$ is taken back high the DAC outputs reflect the data in the DAC registers (assumes that $\overline{LDAC}$ is tied low).

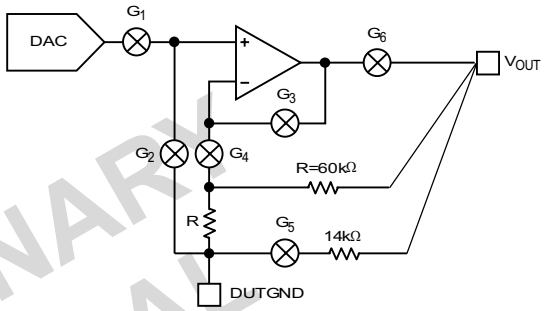


Figure 16. Block Diagram of AD5530/AD5531 Output Stage

Power-On with $\overline{CLR}$ Low
The output stage of the AD5530/AD5531 has been designed to allow output stability during power-on. If $\overline{CLR}$ is kept low during power-on, then just after power is applied to the AD5530/AD5531, the situation is as depicted in Figure 17. G_1, G_4 and G_6 are open while G_2, G_3 and G_5 are closed.

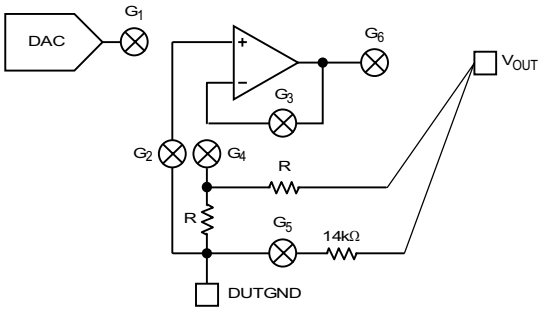


Figure 17. Output Stage with V_{DD} < 7 V or V_{SS} > -3 V; $\overline{CLR}$ Low

V_{OUT} is kept within a few hundred millivolts of DUTGND via G_5 and a 14kΩ resistor. This thin-film resistor is connected in parallel with the gain resistors of the output amplifier. The output amplifier is connected as a unity gain buffer via G_3, and the DUTGND voltage is applied to the buffer input via G_2. The amplifier's output is thus at the same voltage as the DUTGND pin. The output stage remains configured as in Figure 17 until the voltage at $|V_{DD} - V_{SS}|$ reaches approximately +10 V. By now the output amplifier has enough headroom to handle signals at its input and has also had time to settle. The internal power-on circuitry opens G_3 and G_5 and closes

G_4 and G_6. This situation is shown in Figure 18. Now the output amplifier is configured in its noise gain configuration via G_4 and G_6. The DUTGND voltage is still connected to the noninverting input via G2 and this voltage appears at V_{OUT}.

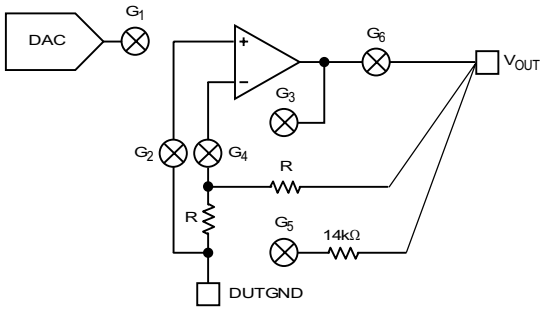


Figure 18. Output Stage with V_{DD} > 7 V or V_{SS} < -3 V; $\overline{CLR}$ Low

V_{OUT} has been disconnected from the DUTGND pin by the opening of G_5 but will track the voltage present at DUTGND via the configuration shown in Figure 18.

When $\overline{CLR}$ is taken back high, the output stage is configured as shown in Figure 9. The internal control logic closes G_1 and opens G_2. The output amplifier is connected in a noninverting gain of two configuration. The voltage that appears on the V_{OUT} pins is determined by the data present in the DAC registers,(assumes that $\overline{LDAC}$ is tied low).

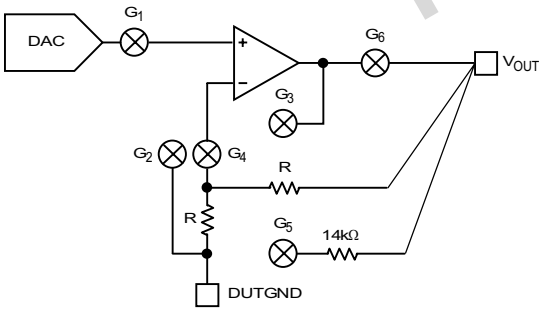


Figure 19. Output Stage After $\overline{CLR}$ Is Taken High

Power-On with $\overline{CLR}$ High

If $\overline{CLR}$ is high on the application of power to the device, the output stages of the AD5530/AD5531 are configured as in Figure 20 while V_{DD} is less than 7 V and V_{SS} is more positive than -3 V. G_1 is closed and G_2 is open thereby connecting the output of the DAC to the input of its output amplifier. G_3 and G_5 are closed while G_4 and G_6 are open thus connecting the output amplifier as a unity gain buffer. V_{OUT} is connected to DUTGND via G_5 through a 14 kΩ resistor until V_{DD} exceeds 7 V and V_{SS} is more negative than -3 V.

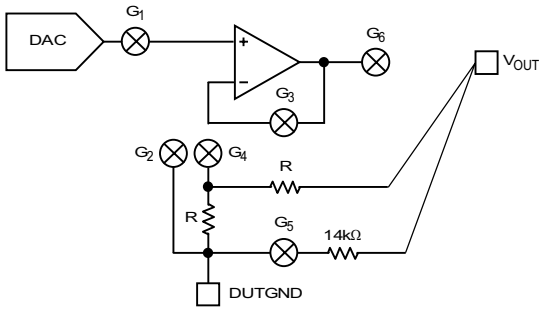


Figure 20. Output Stage Powering Up with $\overline{CLR}$ High While V_{DD} < 7 V or V_{SS} > -3 V

When the difference between the supply voltages reaches +10 V, the internal power-on circuitry opens G_3 and G_5 and closes G_4 and G_6 configuring the output stage as shown in Figure 21.

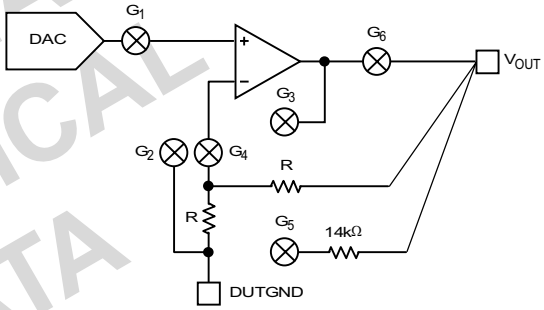


Figure 21. Output Stage Powering Up with $\overline{CLR}$ High; When V_{DD} > 7 V and V_{SS} < -3 V

DUTGND Voltage Range

During power-on, the V_{OUT} pin of the AD5530/AD5531 are connected to the DUTGND pin via G_5 and the 14 kΩ thin-film resistor. The DUTGND potential must obey the max ratings at all times. Thus, the voltage at DUTGND must always be within the range V_{SS} – 0.3 V, V_{DD} + 0.3 V. However, in order that the voltages at the V_{OUT} pin of the AD5530/AD5531 stay within ±2 V of DUTGND potential during power-on, the voltage applied to DUTGND should also be kept within the range GND – 2 V, GND + 2 V.

Once the AD5530/AD5531 has powered-on and the on-chip amplifier has settled, any voltage that is now applied to the DUTGND pin is subtracted from the DAC output which has been gained up by a factor of two. Thus, for specified operation, the maximum voltage that can be applied to the DUTGND pin increases to the maximum allowable $2V_{REF}(+)$ voltage, and the minimum voltage that can be applied to DUTGND is the minimum $2V_{REF}(–)$ voltage. After the AD5530/AD5531 has fully powered on, the outputs can track any DUTGND voltage within this minimum/maximum range.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5530/AD5531 is via a serial bus that uses standard protocol compatible with microcontrollors and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal and a synchronization signal. The AD5530/AD5531 requires a 16-bit data word with data valid on the falling edge of SCLK.

For all the interfaces, the DAC output update may be done automatically when all the data is clocked in or it may be done under the control of $\overline{\text{LDAC}}$.

The contents of the DAC register may be read using the Readback function. $\overline{\text{RBEN}}$ is used to frame the readback data which is clocked out on SDO. The following figures illustrate these DACs interfacing with a simple 4 wire interface. The serial interface of the AD5530/AD5531 may be operated from a minimum of three wires.

AD5530/AD5531 to ADSP-21xx

An interface between the AD5530/AD5531 and the ADSP-21xx is shown in Figure 22. In the interface example shown, SPORT0 is used to transfer data to the DAC. The SPORT control register should be configured as follows : internal Clock operation, alternate framing mode; active low framing signal.

Transmission is initiated by writing a word to the Tx register after the SPORT has been enabled. As the data is clocked out of the DSP on the rising edge of SCLK, no glue logic is required to interface the DSP to the DAC. In the interface shown, the DAC output is updated using the $\overline{\text{LDAC}}$ pin via the DSP. Alternatively, the $\overline{\text{LDAC}}$ input could be tied permanently low and then the update takes place automatically when $\overline{\text{TFS}}$ is taken high.

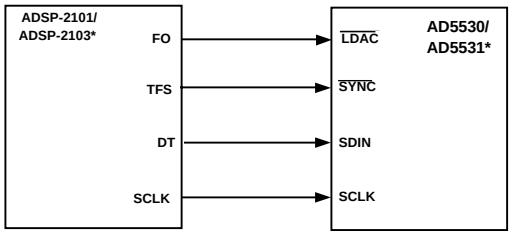


Figure 22. AD5530/AD5531 to ADSP-21xx interface.

AD5530/AD5531 to 8051 Interface

A serial interface between the AD5530/AD5531 and the 8051 is shown in Figure 23. TXD of the 8051 drives SCLK of the AD5530/AD5531, while RXD drives the serial data line, SDIN. P3.3 and P3.4 are bit programmable pins on the serial port and are used to drive $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$ respectively.

The 8051 provides the LSB of its SBUF register as the first bit in the data stream. The user will have to ensure that the data in the SBUF register is arranged correctly as the DAC expects MSB first.

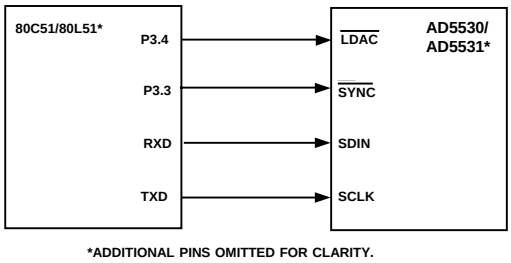


Figure 23. AD5530/AD5531 to 8051 Interface.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RXD is clocked out of the microcontroller on the rising edge of TXD and is valid on the falling edge. As a result no glue logic is required between this DAC and microcontroller interface.

The 8051 transmits data in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. As the DAC expects a 16 bit word, P3.3 must be left low after the first eight bits are transferred. After the second byte has been transferred, the P3.3 line is taken high. The DAC may be updated using $\overline{\text{LDAC}}$ via P3.4 of the 8051.

AD5530/AD5531 to MC68HC11 Interface

Figure 24 shows an example of a serial interface between the AD5530/AD5531 and the MC68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC, while the MOSI output drives the serial data lines, SDIN. $\overline{\text{SYNC}}$ is driven from one of the port lines, in this case PC7.

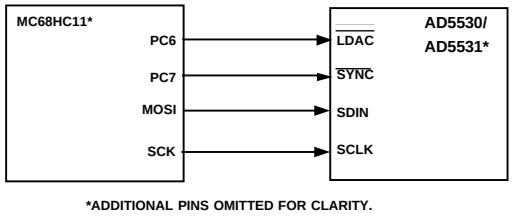


Figure 24. AD5530/AD5531 to MC68HC11 interface.

The 68HC11 is configured for master mode; MSTR=1, CPOL=0 and CPHA = 1. When data is transferred to the part, PC7 is taken low, data is transmitted MSB first. Data appearing on the MOSI output is valid on the falling edge of SCK. Eight falling clock edges occur in the transmit cycle, so in order to load the required 16 bit word, PC7 is not brought high until the second eight bit word has been transferred to the DACs input shift register.

$\overline{\text{LDAC}}$ is controlled by the PC6 port output. The DAC can be updated after each two byte transfer by bringing $\overline{\text{LDAC}}$ low. This example does not show other serial lines for the DAC. If $\overline{\text{CLR}}$ were used, it could be controlled by port output PC5. In order to read data back from the DAC register, the SDO line could be connected to MISO of the MC68HC11, with $\overline{\text{RBEN}}$ tied to another port output controlling and framing the readback data transfer.

APPLICATIONS

Serial Interface to Multiple AD5530s or AD5531s

Figure 25 shows how the $\overline{SYNC}$ pin is used to address multiple AD5530/AD5531s. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{SYNC}$ signal at any one time. The DAC addressed will be determined by the decoder. There will be some feedthrough from the digital input lines, the effects of which can be minimized by using a burst clock.

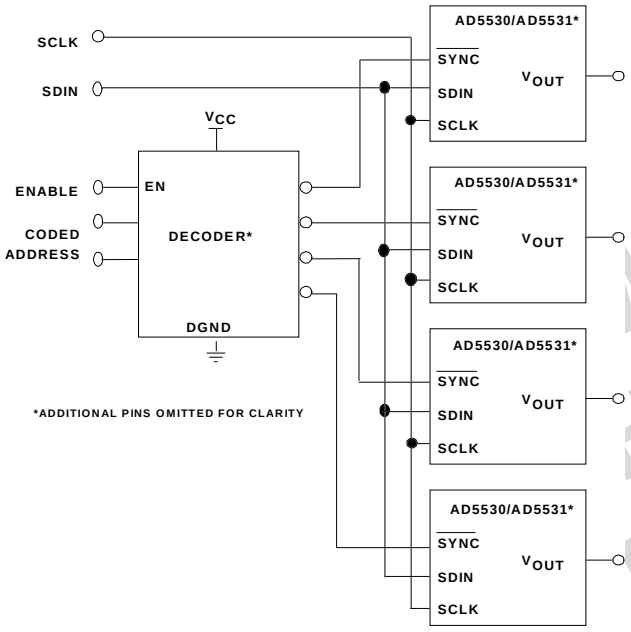


Figure 25. Addressing Multiple AD5530/AD5531s.

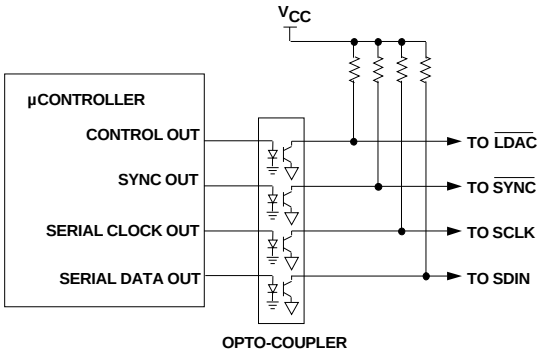


Figure 26. Opto-Isolated Interface.

Optocoupler Interface

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3kV. The serial loading structure of the AD5530/AD5531 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum. Figure 26 shows a 4 channel isolated interface to the AD5530/AD5531. To reduce the number of opto-isolators, if the simultaneous updating of the DAC is not required, then the $\overline{LDAC}$ pin may be tied permanently low.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP
(RU-16)