32-Channel 14-Bit Voltage-Output DAC

Preliminary Technical Data — AD5532*

FEATURES

High Integration: 32-channel DAC in 12x12 mm² LFBGA
Adjustable Voltage Output Range
Guaranteed Monotonic
Readback capability
DSP-/Microcontroller-Compatible Serial Interface
Output impedance: 0.5Ω (AD5532-1, AD5532-2)
500Ω (AD5532-3)
1kΩ (AD5532-5)
Output Voltage Span: 10V (AD5532-1, AD5532-3, AD5532-5)
20V (AD5532-2)
Infinite Sample & Hold Capability to ±0.012% accuracy

APPLICATIONS

Level Setting
Instrumentation
Automatic Test Equipment
Industrial Control Systems
Data Acquisition
Low Cost I/O

GENERAL DESCRIPTION

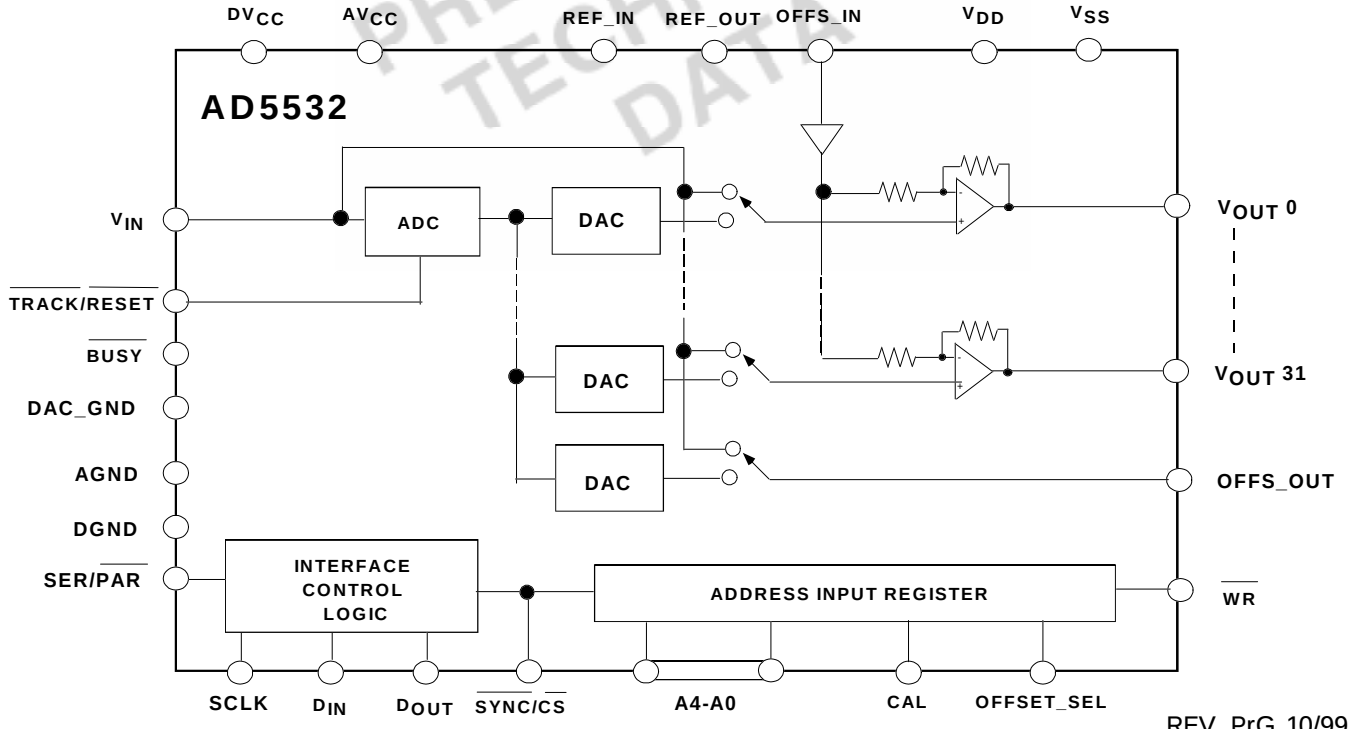
The AD5532 is a 32-channel voltage-output 14-bit DAC with an additional infinite sample-and-hold mode. The selected DAC register is written to via the 3-wire serial interface and V_{OUT} for this DAC is then updated to reflect the new contents of the DAC register. DAC selection is accomplished via address bits A0-A4. The output voltage range is determined by the offset voltage at the OFFS_IN pin and the gain of the output amplifier. It is restricted to a range from V_{SS}+2.2V to V_{DD}-2V because of the head-room of the output amplifier.

The device is operated with AVcc = +5V±5%, DVcc= 2.7V to 5.25V, V_{SS} = -4.75V to -16.5V and V_{DD}= 8V to 16.5V and requires a stable +3V reference on REF_IN as well as an offset voltage on OFFS_IN.

PRODUCT HIGHLIGHTS

1. 32 14-bit DACs in one package, guaranteed monotonic.
2. The AD5532 is available in a 74-lead LFBGA package with a body size of 12mm by 12mm.
3. Droopless/Infinite Sample & Hold Mode.

FUNCTIONAL BLOCK DIAGRAM



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*Protected by U.S. Patent No. 5684481; other patents pending

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AD5532 SPECIFICATIONS

(V_{DD} = +8V to +16.5V, V_{SS} = -4.75V to -16.5V; AV_{CC} = +4.75V to +5.25V; DV_{CC} = +2.7V to +5.25V; AGND = DGND = DAC_GND = 0V; REF_IN = 3V; Output Range from V_{SS}+2.2V to V_{DD}-2V. All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	A Version[2] AD5532-1/-3/-5	A Version[2] AD5532-2 only	Units	Conditions/ Comments
DAC DC PERFORMANCE				
Resolution	14	14	Bits	
Integral Nonlinearity (INL)	0.2	0.2	% of FSR max	
Differential Nonlinearity (DNL)	±1	±1	LSB max	Monotonic
Offset	210	400	mV typ	See Figure 6
Gain	+3.5	+6.7	typ	
Offset Error	±50	TBD	mV max	
Gain Error	±60	TBD	mV max	
Full-Scale Error	±110	TBD	mV max	
VOLTAGE REFERENCE				
REF_IN				
Nominal Input Voltage	+3.0	+3.0	V	
Input Voltage Range	+2.85/+3.15	+2.85/+3.15	V min/max	
Input Current	50	50	nA max	
REF_OUT				
Output Voltage	3	3	V typ	
Output Impedance	280	280	kΩ typ	
Reference Drift	60	60	ppm/°C typ	
ANALOG OUTPUTS (V_{OUT} 0-31)				
Output Temp Coeff[3,4]	10	10	ppm/°C typ	
DC Output Impedance				
AD5532-1	0.5	0.5	Ω typ	
AD5532-3	500		Ω typ	
AD5532-5	1		kΩ typ	
Output Range	V_{SS} +2.2 /V_{DD} - 2	V_{SS} +2.2 /V_{DD} - 2	V min/max	100µA output load
Resistive Load[5]	5	5	kΩ min	
Capacitive Load				
AD5532-1	500	500	pF max	
AD5532-3	TBD		nF max	
AD5532-5	15		nF max	
Short-Circuit Current	10	10	mA typ	
DC Power-Supply Rejection Ratio	-70	-70	dB typ	V_{DD} = 15V ±5%
	-70	-70	dB typ	V_{SS} = -15V ±5%
DC Crosstalk[3]	250	250	µV max	
ANALOG OUTPUT (OFFS_OUT)				
Output Temp Coeff[3,4]	10	10	ppm/°C typ	
DC Output Impedance	1.3	1.3	kΩ typ	
Output Range	60 /+REF_IN-30	60 /+REF_IN-30	mV typ	
Output Current	10	10	µA max	Source Current
Capacitive Load	100	100	pF max	
DIGITAL INPUTS				
Input Current	±1	±1	µA max	
Input Low Voltage	0.8	0.8	V max	DV_{CC} = 5V±5%
	0.4	0.4	V max	DV_{CC} = 3V±10%
Input High Voltage	2.0	2.0	V min	
Input Hysteresis ($\overline{SCLK}$ and $\overline{CS}$ only)	200	200	mV typ	
Input Capacitance	10	10	pF max	
DIGITAL OUTPUTS ($\overline{BUSY}$, D_{OUT})				
Output Low Voltage, DV_{CC} = 5V	0.4	0.4	V max	Sinking 200 µA
Output High Voltage, DV_{CC} = 5V	4.0	4.0	V min	Sourcing 200 µA
Output Low Voltage, DV_{CC} = 3V	0.4	0.4	V max	Sinking 200 µA
Output High Voltage, DV_{CC} = 3V	2.4	2.4	V min	Sourcing 200 µA
High Impedance Leakage Current[6]	±10	±10	µA max	
High Impedance Output Capacitance[6]	15	15	pF typ	

NOTES:
[1]See Terminology
[2]A Version: Industrial temperature range -20°C to +85°C.
[3]Guaranteed by design and characterisation, not production tested
[4]AD780 as reference for the AD5532
[5]Ensure that you do not exceed Tj(max). See max. ratings.
[6]D_{OUT} only
Specifications subject to change without notice

AD5532 SPECIFICATIONS

(V_{DD} = +8V to +16.5V, V_{SS} = -4.75V to -16.5V; AV_{CC} = +4.75V to +5.25V; DV_{CC} = +2.7V to +5.25V; AGND = DGND = DAC_GND = 0V; REF_IN = 3V; Output Range from V_{ss}+2.2V to V_{DD} -2V. All outputs unloaded. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	A Version[2] AD5532-1/-3/-5	AD5532-2 only	Units	Conditions/ Comments
POWER REQUIREMENTS				
Power-Supply Voltages				
V_{DD}	+8/+16.5	+8/+16.5	V min/max	
V_{SS}	-4.75/-16.5	-4.75/-16.5	V min/max	
AV_{CC}	+4.75/+5.25	+4.75/+5.25	V min/max	
DV_{CC}	+2.7/+5.25	+2.7/+5.25	V min/max	
Power-Supply Currents[4]				
I_{DD}	TBD		mA max	8mA typ
I_{SS}	TBD		mA max	8mA typ
AI_{CC}	TBD		mA max	27mA typ
DI_{CC}	< 1	<1	mA max	
Power Dissipation[4]	250	250	mW typ	V_{DD}=10V, V_{SS}=-5V
AC CHARACTERISTICS[3]				
Output Voltage Settling Time	16	TBD	µs max	Full Scale change
OFFS_IN Settling Time	10	TBD	µs max	
Digital-to-Analog Glitch Impulse	1	1	nV-s typ	1 LSB change around major carry
Digital Crosstalk	6	6	nV-s typ	
Analog Crosstalk	1.5	1.5	nV-s typ	
Digital Feedthrough	0.5	0.5	nV-s typ	
Output Noise Spectral Density	TBD		nV/(Hz)$^{1/2}$ typ	

NOTES:
[1]See Terminology
[2]A version: Industrial temperature range -20°C to +85°C.
[3]Guaranteed by design and characterisation, not production tested
[4]Outputs Unloaded.
Specifications subject to change without notice

SHA Mode

Parameter[1]	A Version[2] AD5532-1/-3/-5	AD5532-2 only	Units	Conditions/ Comments
ANALOG CHANNEL				
V_{IN} to V_{OUT} Nonlinearity	± 0.012	± 0.012	% max	Typically ±0.006%[3]
Offset Error	± 50	TBD	mV max	See Figure 7
Gain Error	± 60	TBD	mV max	See Figure 7
ANALOG INPUT (V_{IN})				
Input Voltage Range	0 to +3	0 to +3	V	Nominal Input Range
Input Current	100	100	nA max	V_{IN} acquired on 1 channel
Input Current (Cal Mode)	3.2	3.2	µA max	V_{IN} acquired on 32 channels
Input Capacitance	50	50	pF typ	
Input Lower Deadband	60	60	mV max	See Figure 7
Input Upper Deadband	30	30	mV max	See Figure 7
ANALOG INPUT (OFFS_IN)				
Input Current	100	100	nA max	
AC CHARACTERISTICS[4]				
AC Crosstalk	20	20	nV-s typ	
Output Settling Time	3	TBD	µs max	100pF load
Acquisition Time	16	16	µs max	To ± 0.012% accuracy

NOTES:
[1]See Terminology
[2]A version: Industrial temperature range -20°C to +85°C.
[3]With offset and gain adjustment
[4]Guaranteed by design and characterisation, not production tested
Specifications subject to change without notice

Timing Characteristics
Parallel Interface

Parameter[1,2]	Limit at T_{MIN}, T_{MAX} (A Version)	Units	Conditions/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulse Width Low
t_4	50	ns min	$\overline{WR}$ Pulse Width Low
t_5	20	ns min	A4-A0, CAL, OFFS_SEL to $\overline{WR}$ Setup Time
t_6	0	ns min	A4-A0, CAL, OFFS_SEL to $\overline{WR}$ Hold Time

NOTES:
[1]See Interface Timing Diagram below
[2]Guaranteed by design and characterization, not production tested.

Serial Interface

Parameter[1,2]	Limit at T_{MIN}, T_{MAX} (A Version)	Units	Conditions/Comments
f_{CLKIN}	15	MHz max	SCLK frequency
t_1	30	ns min	SCLK High Pulse Width
t_2	30	ns min	SCLK Low Pulse Width
t_3	5	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	TBD	ns min	$\overline{SYNC}$ Low Time
t_5	10	ns min	D_{IN} Setup Time
t_6	5	ns min	D_{IN} Hold Time
t_7	5	ns min	$\overline{SYNC}$ Falling Edge to SCLK Rising Edge Setup Time
t_8[3]	10	ns max	SCLK Rising Edge to D_{OUT} Valid
t_9[3]	20	ns max	SCLK Falling Edge to D_{OUT} High Impedance

NOTES:
[1]See Interface Timing Diagrams on following page
[2]Guaranteed by design and characterization, not production tested.
[3]These numbers are measured with the load circuit of Figure 2

Parallel Interface Timing Diagram

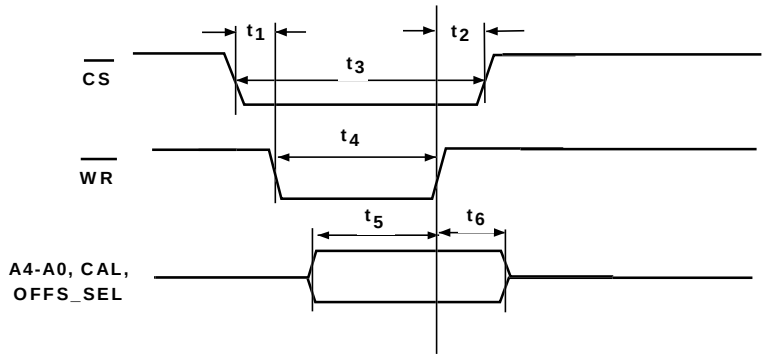


Figure 1. Parallel Write (SHA Mode only)

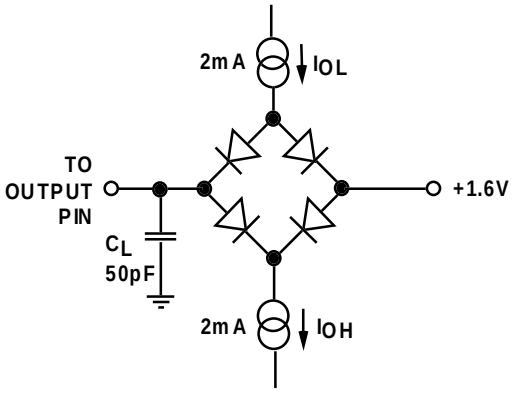


Figure 2. Load Circuit for D_{OUT} Timing Specifications

Serial Interface Timing Diagrams

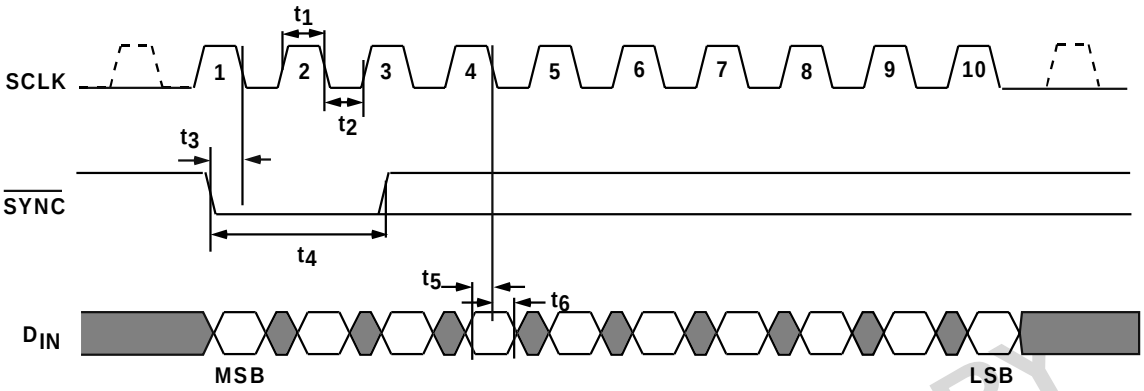


Figure 3. 10-Bit Write (SHA Mode and Both Readback Modes)

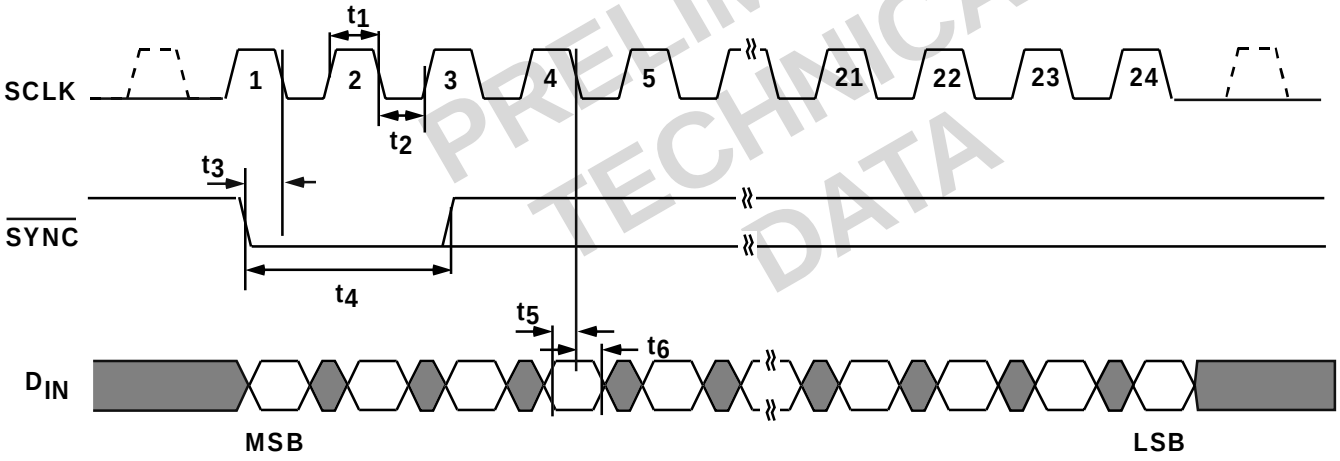


Figure 4. 24-Bit Write (DAC Mode)

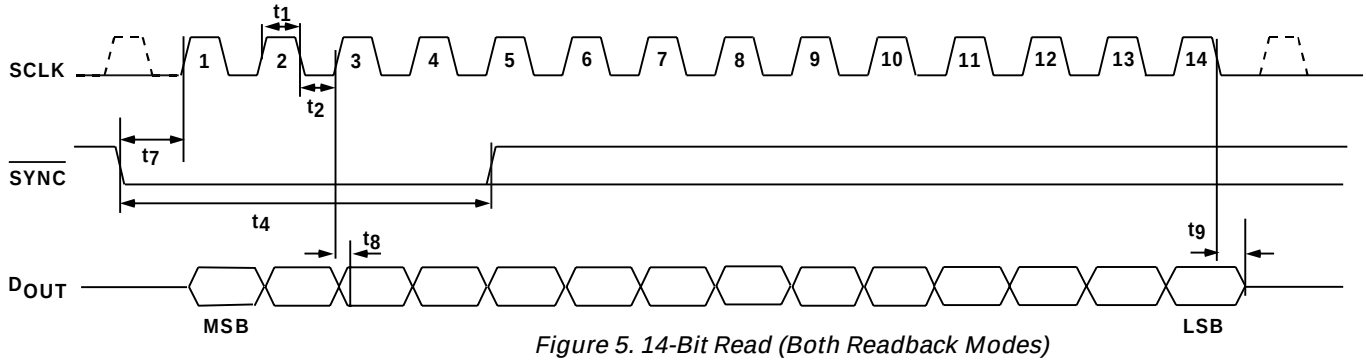


Figure 5. 14-Bit Read (Both Readback Modes)

ORDERING GUIDE

Model	Function	Output Impedance	Output Voltage Span	Package Option
AD5532ABC-1	32 DACs, 32-channel SHA	0.5Ω typ	10V	74-lead LFBGA
AD5532ABC-2	32 DACs, 32-channel SHA	0.5Ω typ	20V	74-lead LFBGA
AD5532ABC-3	32 DACs, 32-channel SHA	500Ω typ	10V	74-lead LFBGA
AD5532ABC-5	32 DACs, 32-channel SHA	1kΩ typ	10V	74-lead LFBGA
AD5533ABC-1*	32-channel SHA only	0.5Ω typ	10V	74-lead LFBGA

* Separate datasheet

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND.....-0.3V to +17V
V_{SS} to AGND.....+0.3V to -17V
AV_{CC} to AGND, DAC_GND.....-0.3V to +7V
DV_{CC} to DGND.....-0.3V to +7V
Digital Inputs to DGND.....-0.3V to DV_{CC}+0.3V
Digital Outputs to DGND.....-0.3V to DV_{CC}+0.3V
REF_IN to AGND, DAC_GND.....-0.3V to +7V
V_{IN} to AGND, DAC_GND.....-0.3V to +7V
V_{OUT}0-31 to AGND.....V_{SS}-0.3V to V_{DD}+0.3V
OFFS_IN to AGND.....V_{SS}-0.3V to V_{DD}+0.3V
OFFS_OUT to AGND.....AGND-0.3V to AV_{CC}+0.3V
AGND to DGND.....TBD

Operating Temperature Range
Industrial .....-20°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max).....+150°C
74-lead LFBGA Package,
Power Dissipation.....(T_J max - T_A)/θ_{JA} mW
θ_{JA} Thermal Impedance.....75°C/W
Solder Ball Temperature, Soldering.....TBD °C.

NOTES:
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100mA will not cause SCR latch-up

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5532 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

AD5532	Function
AGND(1-2)	Analog GND pins.
AV_{CC} (1-2)	Analog supply pins. Voltage range from +4.75V to +5.25V.
V_{DD} (1-4)	V_{DD} supply pins. Voltage range from +8V to +16.5V.
V_{SS} (1-4)	V_{SS} supply pins. Voltage range from -4.75V to -16.5V.
DGND	Digital GND pins
DV_{CC}	Digital supply pins. Voltage range from +2.7V to +5.25V.
DAC_GND(1-2)	Reference GND supply for all the DACs.
REF_IN	Reference voltage for channels 0-31
REF_OUT	Reference output voltage
V_{OUT} (0-31)	Analog output voltages from the 32 channels.
V_{IN}	Analog input voltage. Connect this to AGND if operating in DAC mode only.
A4-A1[1], A0[2]	Parallel Interface: 5 address pins for 32 channels. A4=MSB of channel address. A0=LSB
CAL[1]	Parallel Interface: Control input which allows all 32 channels to acquire V_{IN} simulta neously
$\overline{CS}$ / $\overline{SYNC}$	This pin is both the active low Chip Select pin for the parallel interface and the Frame Synchronisation pin for the serial interface.
$\overline{WR}$[1]	Parallel Interface. Write pin. Active low. This is used in conjunction with the $\overline{CS}$ pin to address the device using the parallel interface.
OFFSET_SEL[1]	Offset Select pin. This is activated when writing to the DAC which provides its output at the OFFS_OUT pin.
SCLK[2]	Serial Clock input for serial interface. This operates at clock speeds up to 20MHz
D_{IN}[2]	Data input for serial interface. Data must be valid on the falling edge of SCLK
D_{OUT}	Output from the DAC registers for readback. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
SER/$\overline{PAR}$[1]	This pin allows the user to select whether the serial or parallel interface will be used. If the pin is tied low, the parallel interface will be used. If it is tied high, the serial interface will be used.
OFFS_IN	Offset input. The user can supply a voltage here to offset the output span. OFFS_OUT can also be tied to this pin if the user wants to drive this pin with the Offset Channel.
OFFS_OUT	Offset output. This is the acquired offset voltage which can be tied to OFFS_IN to offset the span.
$\overline{BUSY}$	This output tells the user when the input voltage is being acquired. It goes low during acquisition and returns high when the acquisition operation is complete.
$\overline{TRACK}$/$\overline{RESET}$[2]	If this input is held high, V_{IN} is acquired once the channel is addressed. While it is held low, the input to the gain/offset stage is switched directly to V_{IN}. The addressed channel begins to acquire V_{IN} on the rising edge of $\overline{TRACK}$. See $\overline{TRACK}$ Input section for further information. This input can also be used as a means of resetting the complete device to its power-on-reset conditions. This is achieved by applying a low going pulse of between 50ns and 150ns to this pin. See section on $\overline{RESET}$ Function for further details.

NOTES:
[1]Internal Pull-down devices on these logic inputs. Therfore, they can be left floating and will default to a logic low condition.
[2]Internal Pull-up devices on these logic inputs. Therfore, they can be left floating and will default to a logic high condition.

TERMINOLOGY

DAC MODE

Integral Nonlinearity (INL)
This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of Full-Scale span.

Differential Nonlinearity (DNL)
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Offset
Offset is a measure of the output with all zeros loaded to the DAC and OFFS_IN = 0. Since the DAC is lifted off the ground by 60mV this output should be:

V_{OUT} = Gain * 60mV

Offset Error
This is a measure of the output error with all zeros loaded to the DAC. Ideally the output should be:

V_{OUT} = (Gain * 60) - ((Gain - 1) * V_{OFFS_IN}) mV

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Full-Scale Error
This is a measure of the output error with all ones loaded to the DAC. Ideally, the output should be:

V_{OUT} = (Gain * V_{REF}) - ((Gain - 1)*V_{OFFS_IN})

Full-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the transfer function expressed in mV. It is calculated as:

Gain Error = Full-Scale error - Offset Error

Output Settling Time
This is the time taken from when the last data bit is clocked into the DAC until the output has settled to within ± 0.2% (± 0.5 LSB at 9 bits).

OFFS_IN Settling Time
This is the time taken from a step change in input voltage on OFFS_IN until the output has settled to within ± 0.2% (± 0.5 LSB at 9 bits).

Digital-to-Analog Glitch Impulse
This is the area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-secs when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00 or 100...00 to 011...11).

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at mid-scale while a full-scale code change (all 1s to all 0s and vice versa) is being written to another DAC. It is expressed in nV-secs.

Analog Crosstalk
This the area of the glitch transferred to the output (V_{OUT}) of one DAC due to a full-scale change in the output (V_{OUT}) of another DAC. The area of the glitch is expressed in nV-secs.

Digital Feeedthrough
This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e. $\overline{CS}/\overline{SYNC}$ is high. It is specified in nV-secs and is measured with a worst-case change on the digital input pins, e.g. from all 0s to all 1s and vice versa.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per root Hertz). It is measured in $nV/(Hz)^{1/2}$.

Output Temp Coefficient
This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

DC Power-Supply Rejection Ratio
DC Power-Supply Rejection Ratio (PSRR) is a measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dBs. V_{DD} and V_{SS} are varied ± 5%.

DC Crosstalk
This the DC change in the output level of one DAC at mid-scale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in µV.

SHA MODE

V_{IN} to V_{OUT} Nonlinearity
This is a measure of the maximum deviation from a straight line passing through the endpoints of the V_{IN} vs. V_{OUT} transfer function. It is expressed as a percentage of the full-scale span.

Offset Error
This is a measure of the output error when V_{IN} = 60mV. Ideally, with V_{IN}=60mV:

V_{OUT} = (Gain * 60) - ((Gain - 1) * V_{OFFS_IN}) mV

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Gain Error
This is a measure of the span error of the analog channel. It is the deviation in slope of the transfer function expressed in mV. It is calculated as:

Gain Error = Ideal Fullscale Output - Actual Fullscale Output - Offset Error

where

Ideal Fullscale Output = Gain*2.97 - ((Gain-1)*V_{OFFS_IN})

AC Crosstalk
This is the area of the glitch that occurs on the output of one channel while another channel is acquiring. It is expressed in nV-secs.

Output Settling Time
This is the time taken from when $\overline{BUSY}$ goes high to when the output has settled to ± 0.012% (± 0.5 LSB at 12 bits).

Acquisition Time
This is the time taken for the V_{IN} input to be acquired. It is the length of time that $\overline{BUSY}$ stays low.

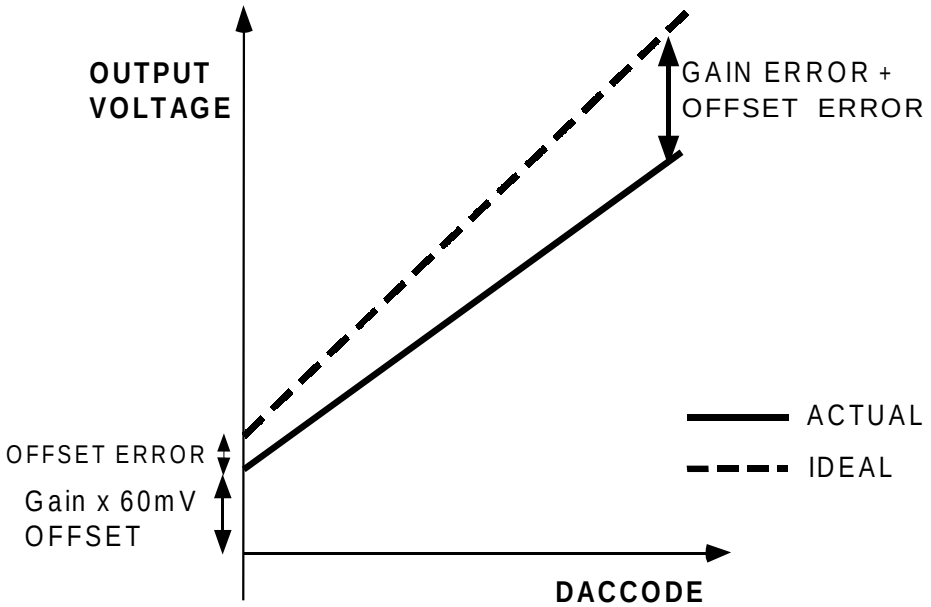


Figure 6. DAC Transfer Function (OFFS_IN = 0)

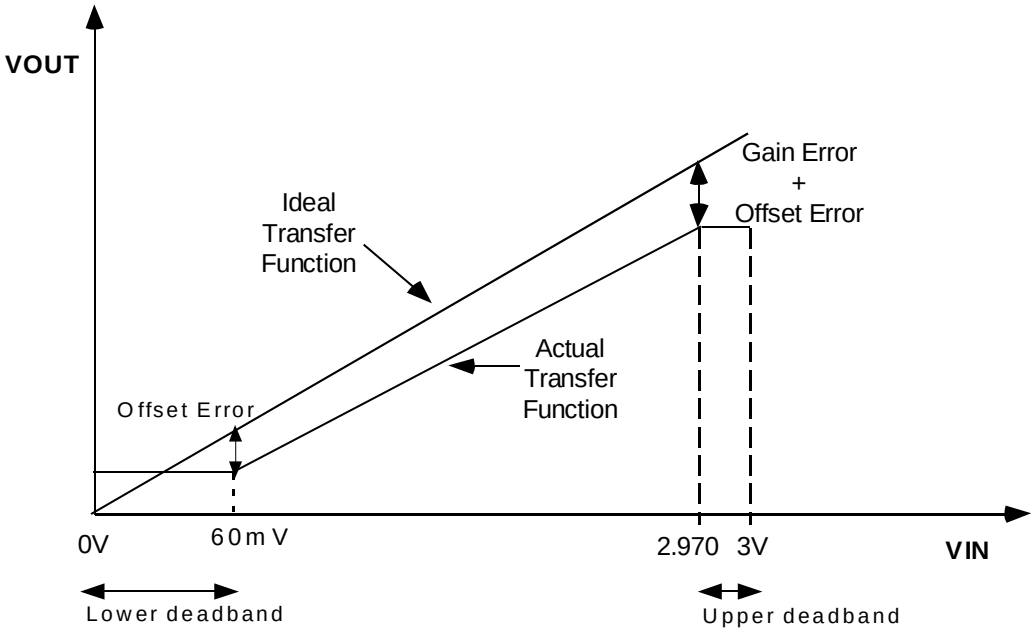


Figure 7. SHA Transfer Function

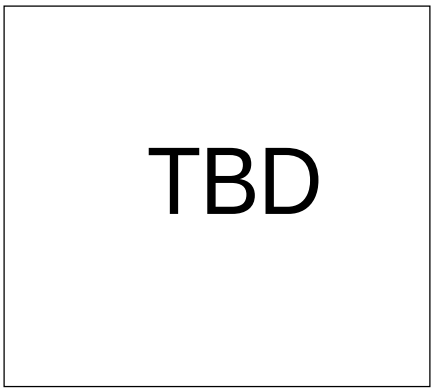


Figure 8. AD5532 Typical DNL Plot

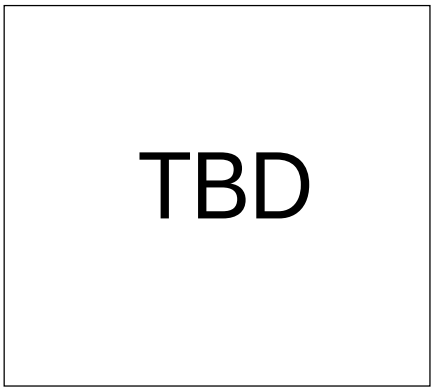


Figure 9. AD5532 Typical INL Plot

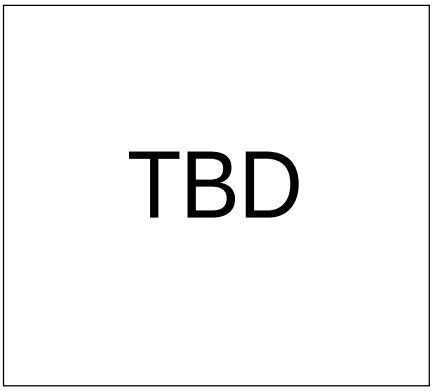


Figure 10. AD5532 INL Error and DNL Error vs. Temperature

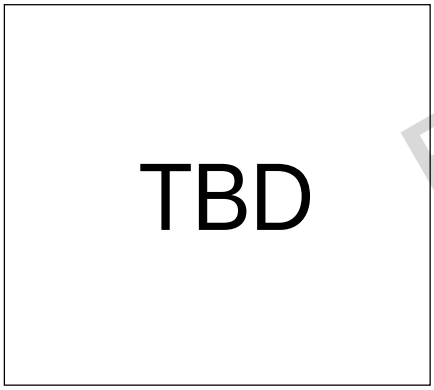


Figure 11. AD5532 Offset Error and Gain Error vs. Temperature

Figure 12. AD5532 Offset Error and Gain Error vs. V_{DD}

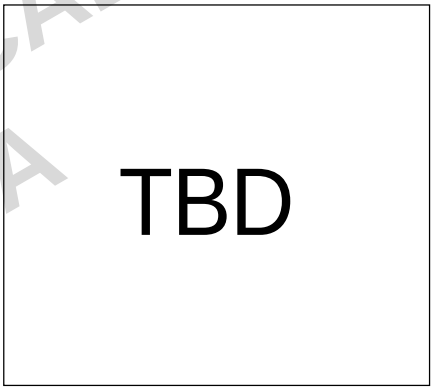


Figure 13. AD5532 V_{OUT} Source and Sink Capability

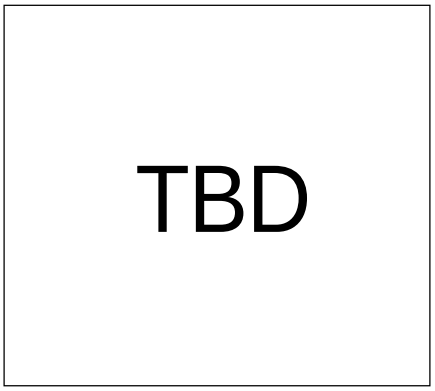


Figure 14 Full-Scale Settling Time

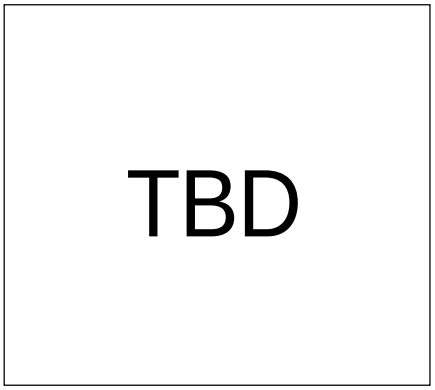


Figure 15. AD5532 Major Code Transition Glitch Impulse

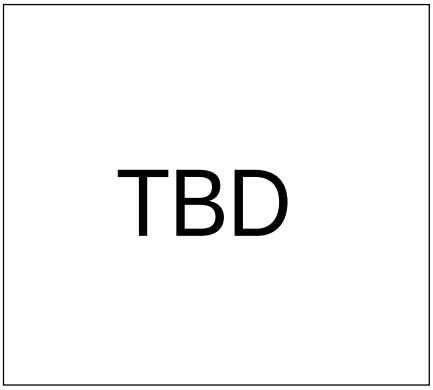


Figure 16. V_{IN} to V_{OUT} accuracy (SHA mode)

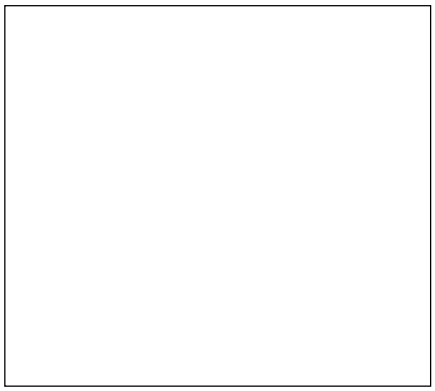


Figure 17. Acquisition Time and Output Settling Time (SHA mode)

Figure 18. Noise distribution (SHA mode)

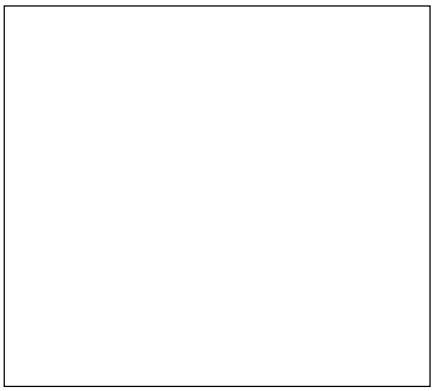
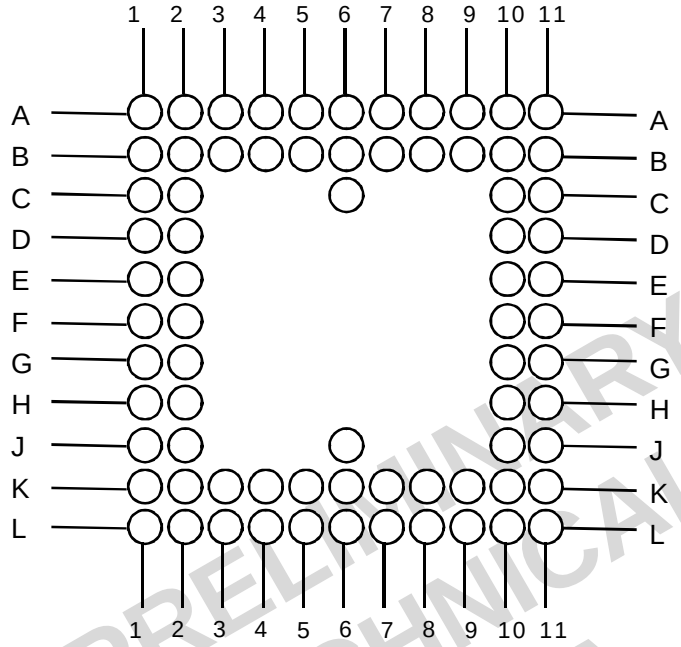


Figure 19. Output Noise Spectral Density



AD5532 74-LEAD LFBGA BALL CONFIGURATION

LFBGA Number	Ball Name	LFBGA Number	Ball Name	LFBGA Number	Ball Name
A1	N/C	C10	AVCC1	J10	VO9
A2	A4	C11	REF_OUT	J11	VO11
A3	A2	D1	VO20	K1	VO17
A4	A0	D2	DAC_GND2	K2	VO15
A5	$\overline{CS}$/$\overline{SYNC}$	D10	AVCC2	K3	VO27
A6	DVCC	D11	OFFS_OUT	K4	VSS3
A7	SCLK	E1	VO26	K5	VSS1
A8	OFFSET_SEL	E2	VO14	K6	VSS4
A9	$\overline{BUSY}$	E10	AGND1	K7	VDD2
A10	$\overline{TRACK}$/$\overline{RESET}$	E11	OFFS_IN	K8	VO2
A11	N/C	F1	VO25	K9	VO10
B1	VO16	F2	VO21	K10	VO13
B2	N/C	F10	AGND2	K11	VO12
B3	A3	F11	VO6	L1	N/C
B4	A1	G1	VO24	L2	VO28
B5	$\overline{WR}$	G2	VO8	L3	VO29
B6	DGND	G10	VO5	L4	VO30
B7	DIN	G11	VO3	L5	VDD3
B8	CAL	H1	VO23	L6	VDD1
B9	SER/$\overline{PAR}$	H2	VIN	L7	VDD4
B10	DOUT	H10	VO4	L8	VO31
B11	REF_IN	H11	VO7	L9	VO0
C1	VO18	J1	VO22	L10	VO1
C2	DAC_GND1	J2	VO19	L11	N/C
C6	N/C	J6	VSS2		

FUNCTIONAL DESCRIPTION

The AD5532 can be thought of as consisting of 32 DACs and an ADC (for SHA mode) in a single package. In DAC mode a 14-bit digital word is loaded into one of the 32 DAC registers via the serial interface. This is then converted (with gain and offset) into an analog output voltage ($V_{OUT}0$ - V_{OUT} 31).

To update a DAC's output voltage the required DAC is addressed via the serial port. When the DAC address and code have been loaded the selected DAC converts the code.

On power-on, all the DACs, including the offset channel, are loaded with zeros. The internal DAC outputs are at 60mV (negative full-scale). If the OFFS_IN pin is driven by the on-board offset channel, the outputs $V_{OUT}0$ to $V_{OUT}31$ are also at 60mV on power-on since OFFS_IN = 60mV, V_{OUT}= (Gain*V_{DAC}) - (Gain-1)*V_{OFFS_IN} = 60mV.

Output Buffer Stage - Gain and Offset

The function of the output buffer stage is to translate the 0-3V output of the DAC to a wider range. This is done by gaining up the DAC output by 3.5/6.7 and offsetting the voltage by the voltage on OFFS_IN pin.

AD5532-1/AD5532-3/AD5532-5:

$V_{OUT} = 3.5*V_{DAC} - 2.5*V_{OFFS\_IN}$

AD5532-2:

$V_{OUT} = 6.7*V_{DAC} - 5.7*V_{OFFS\_IN}$

V_{DAC} is the output of the DAC
V_{OFFS_IN} is the voltage at the OFFS_IN pin

The following table shows how the output range on V_{OUT} relates to the Offset voltage supplied by the user:

SAMPLE OUTPUT VOLTAGE RANGES

V_{OFFS_IN}(V)	V_{DAC}(V)	V_{OUT}(AD5532-1/-3/-5)	V_{OUT}(AD5532-2)
0.5	0 to 3	-1.25 to 9.25	Not allowed
1	0 to 3	-2.5 to 8	-5.7 to 14.4

V_{OUT} is limited only by the headroom of the output amplifiers. V_{OUT} must be within maximum ratings.

Offset Voltage Channel

The offset voltage can be supplied externally by the user at OFFS_IN or it can be supplied by an additional offset voltage channel on the device itself. The offset can be set up in two ways. In SHA mode the required offset voltage is set up on V_{IN} and acquired by the offset DAC. In DAC mode the code corresponding to the offset value is loaded directly into the offset DAC. This offset channel's DAC output is connected directly to OFFS_OUT. By connecting OFFS_OUT to OFFS_IN this offset voltage can be used as the offset voltage for the 32 output amplifiers. It is important to choose the offset so that V_{OUT} is within max. ratings.

Reset Function

The reset function on the AD5532 can be used to reset all nodes on this device to their power-on-reset condition. This is implemented by applying a low going pulse of between 50ns and 150ns to the $\overline{\text{TRACK}}$/$\overline{\text{RESET}}$ pin on the device. If the applied pulse is less than 50ns it is taken as being a glitch and no operation takes place. If the applied pulse is wider than 150ns this pin adopts its track function on the selected channel, V_{IN} is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{\text{TRACK}}$.

SHA mode

In SHA mode the input voltage V_{IN} is sampled and converted into a digital word. The non-inverting input to the output buffer (gain and offset stage) is tied to V_{IN} during the acquisition period to avoid spurious outputs while the DAC acquires the correct code. This is completed in 16 µs max. At this time the updated DAC output assumes control of the output voltage. The output voltage of the DAC is connected to the non-inverting input of the output buffer. Since the channel output voltage is effectively the output of a DAC there is no droop associated with it. As long as power is maintained to the device the output voltage will remain constant until this channel is addressed again.

$\overline{\text{TRACK}}$ Function (SHA mode)

Normally in SHA mode of operation, $\overline{\text{TRACK}}$ is held high and the channel begins to acquire when it is addressed. However, if $\overline{\text{TRACK}}$ is low when the channel is addressed then V_{IN} is switched to the output buffer and an

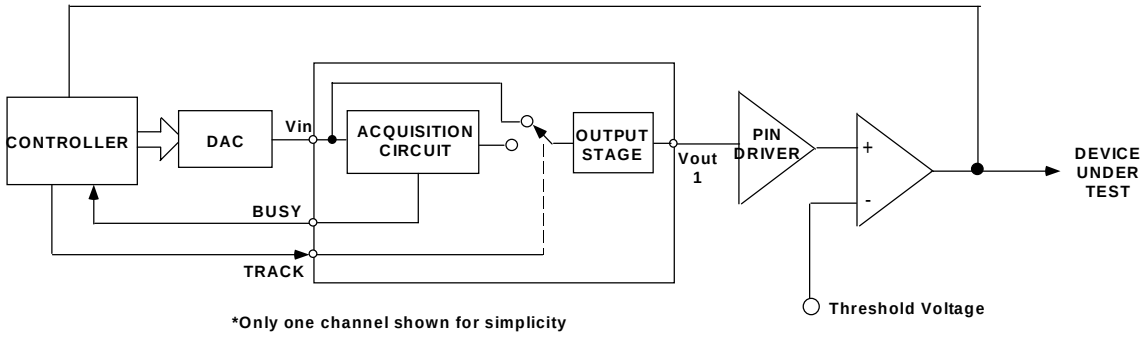


Figure 20. Typical ATE circuit using TRACK Input

acquisition on the channel will not occur until a rising edge of $\overline{TRACK}$. At this stage the $\overline{BUSY}$ pin will go low until the acquisition is complete at which point the DAC assumes control of the voltage to the output buffer and V_{IN} is free to change again without affecting this output value.

This is useful in an application where the user wants to ramp up V_{IN} until V_{OUT} reaches a particular level (Figure 20). V_{IN} doesn't need to be acquired continuously while it is ramping up. $\overline{TRACK}$ can be kept low and only when V_{OUT} has reached its desired voltage is $\overline{TRACK}$ brought high. At this stage, the acquisition of V_{IN} begins.

In the example shown, a desired voltage is required on the output of the pin driver. This voltage is represented by one input to a comparator. The microcontroller/ microprocessor ramps up the input voltage on V_{IN} through a DAC. $\overline{TRACK}$ is kept low while the voltage on V_{IN} ramps up so that V_{IN} is not continually acquired. When the desired voltage is reached on the output of the pin driver, the comparator output switches. The µC/µP then knows what code is required to be input in order to get the desired voltage at the DUT. The $\overline{TRACK}$ input is now brought high and the part begins to acquire V_{IN}. At this stage $\overline{BUSY}$ goes low until V_{IN} has been acquired. Then the output buffer is switched from V_{IN} to the output of the DAC.

MODES OF OPERATION

The AD5532 can be used in 4 different modes of operation. These modes are set by two Mode bits, the first 2 bits in the serial word.

MODES OF OPERATION

Mode Bit 1	Mode Bit 2	Operating Mode
0	0	SHA Mode
0	1	DAC Mode
1	0	Acquire and Readback
1	1	Readback

1) DAC Mode:
In this standard mode a selected DAC register is loaded serially. This requires a 24-bit write (10 bits to address the relevant DAC plus an extra 14 bits of DAC data). Any one of the 32 DAC registers may be written to individually or they can all be loaded simultaneously.

2) SHA Mode:
In this mode a channel is addressed and that channel acquires the voltage on V_{IN}. This mode requires a 10-bit write (see figure below) to address the relevant channel ($V_{OUT}0$-$V_{OUT}31$, Offset Channel or all channels).

3) Acquire and Readback Mode:
This mode allows the user to acquire V_{IN} and read back the data in a particular DAC register. The relevant DAC is addressed (10-bit write) and V_{IN} is acquired in 16µs (max). Following the acquisition the next falling edge of $\overline{SYNC}$ clocks the data in the relevant DAC register out onto the D_{OUT} line in a 14-bit serial format. The full acquisition time must elapse before the DAC register data can be clocked out.

4) Readback Mode
Again, this is a readback mode but no acquisition is performed. The relevant DAC is addressed (10-bit write) and on the next falling edge of $\overline{SYNC}$, the data in the relevant DAC register is clocked out onto the D_{OUT} line in a 14-bit serial format. The serial write and read words can be seen in Figure 21.

This feature allows the user to readback the DAC register code of any of the DACs. In DAC mode this is useful in verification of write cycles. In SHA mode readback is useful if the system has been calibrated and the user wants to know what code in the DAC corresponds to a desired voltage on V_{OUT}. If the user requires this voltage again, all he needs to do is to input the code directly to the DAC register without going through the acquisition sequence.

INTERFACES

Serial Interface

The SER/$\overline{PAR}$ pin is tied high to enable the serial interface and to disable the parallel interface. The serial interface is controlled by 4 pins as follows:

$\overline{SYNC}$, D_{IN}, SCLK: Standard 3-wire interface pins. The $\overline{SYNC}$ pin is shared with the $\overline{CS}$ function of the parallel interface.

D_{OUT}: Data Out pin for reading back the contents of the DAC registers. The data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.

Mode bits: There are 4 different modes of operation as described above.

Cal bit: This is used as a calibration instruction. When this is high in DAC mode all 32 DACs are loaded simultaneously. In SHA mode all 32 channels acquire V_{IN} simultaneously.

Offset_Sel bit: Used to address the offset voltage control channel. Normally low.

A4-A0: Used to address any one of the 32 channels (A4 = MSB of address, A0=LSB).

DB13-DB0: These are used to write a 14-bit word into the addressed DAC register. Clearly, this is only valid when in DAC mode.

The serial interface is designed to allow easy interfacing to most microcontrollers and DSPs, e.g., PIC16C, PIC17C, QSPI, SPI, DSP56000, TMS320 and ADSP21xx, without the need for any glue logic. When interfacing to the 8051, the SCLK must be inverted. The Microprocessor/Microcontroller Interface section explains how to interface to some popular DSPs and microcontrollers.

Figures 3, 4 and 5 show the timing diagram for a serial read and write to the AD5532. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{SYNC}$ resets a counter that counts the number of serial clocks to ensure the correct number of bits are shifted in and out of the serial shift registers. Any further edges on $\overline{SYNC}$ are ignored until the correct number of bits are shifted in or out. Once the correct number of bits for the selected mode have been shifted in or out, the SCLK is ignored. In order for another serial transfer to take place the counter must be reset by the falling edge of $\overline{SYNC}$.

In readback the first rising SCLK edge after the falling edge of $\overline{SYNC}$ causes D_{OUT} to leave its high impedance state and data is clocked out onto the D_{OUT} line and also on subsequent SCLK rising edges. The D_{OUT} pin goes back into a high impedance state on the falling edge of the 14th SCLK. Data on the D_{IN} line is latched in on the first SCLK falling edge after the falling edge of the $\overline{SYNC}$ signal and on subsequent SCLK falling edges. During readback D_{IN} is ignored. The serial interface will not shift data in or out until it receives the falling edge of the $\overline{SYNC}$ signal.

Parallel Interface (SHA mode only)

The SER/$\overline{PAR}$ bit must be tied low to enable the parallel interface and disable the serial interface. The parallel interface is controlled by 10 pins.

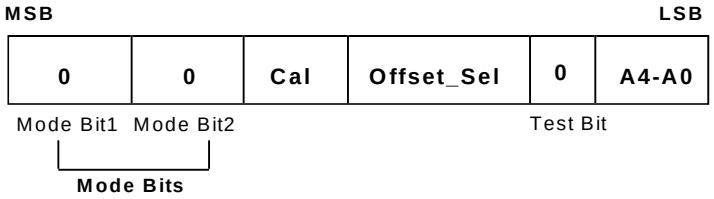
$\overline{CS}$: Active low package select pin. This pin is shared with the $\overline{SYNC}$ function for the serial interface.

$\overline{WR}$: Active low Write pin. The values on the address pins are latched on a rising edge of $\overline{WR}$.

A4-A0: 5 Address pins (A4=MSB of address, A0=LSB). These are used to address the relevant channel (out of a possible 32).

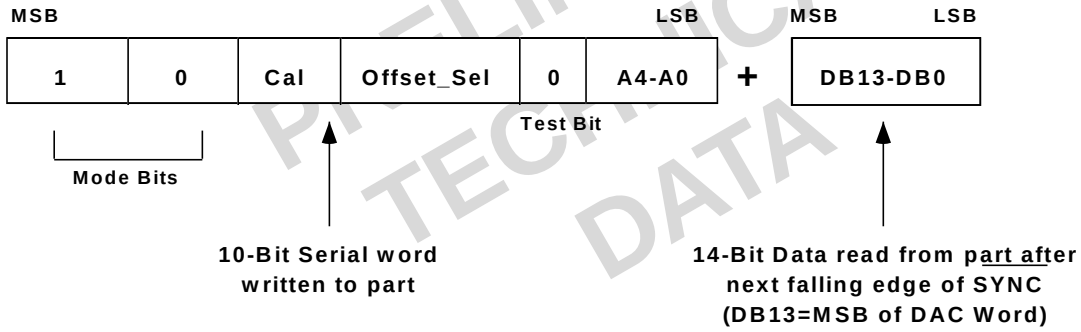
Offset_Sel: Offset select pin. This has the same function as the Offset_Sel bit in the serial interface. When it is activated, the offset voltage control channel is addressed. The address on A4-A0 is ignored in this case.

Cal: Same functionality as the Cal bit in the serial interface (calibration instruction). When this pin is active, all 32 channels acquire V_{IN} simultaneously.

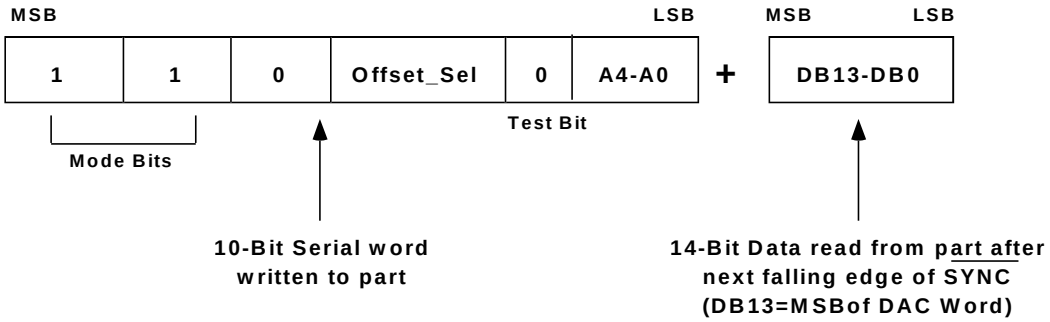


10-Bit Input Serial Write Word (SHA Mode)

24-Bit Input Serial Write Word (DAC Mode)



Input Serial Interface (Acquire and Readback Mode)



Input Serial Interface (Readback Mode)

Figure 21. Serial Interface Formats

MICROPROCESSOR INTERFACING

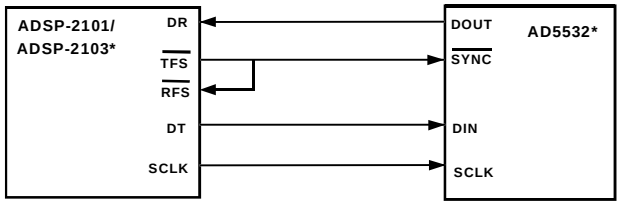
AD5532 to ADSP-21xx Interface

The ADSP21xx family of DSPs are easily interfaced to the AD5532 without the need for extra logic.

A data transfer is initiated by writing a word to the TX register after the SPORT has been enabled. In a write sequence data is clocked out on each rising edge of the DSP's serial clock and clocked into the AD5532 on the falling edge of it's SCLK. In readback 16 bits of data are clocked out of the AD5532 on each rising edge of SCLK and clocked into the DSP on the rising edge of SCLK. DIN is ignored. The valid 14 bits of data will be centred in the 16-bit RX register when using this configuration. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0, External Framing Signal
ITFS = 1, Internal Framing Signal
SLEN = 1001, 10-Bit Data Words (SHA mode write)
SLEN = 0111, 3x 8-Bit Data Words (DAC mode write)
SLEN = 1111, 16-Bit Data Words (Readback mode)

Figure 22 shows the connection diagram.

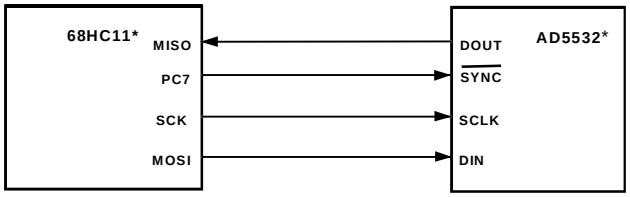


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 22. AD5532 to ADSP-2101/03 Interface

AD5532 to MC68HC11

The Serial Peripheral Interface (SPI) on the MC68HC11 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 0 and the Clock Phase Bit (CPHA) = 1. The SPI is configured by writing to the SPI Control Register (SPCR)—see 68HC11 user manual. SCK of the 68HC11 drives the SCLK of the AD5532, the MOSI output drives the serial data line (DIN) of the AD5532 and the MISO input is driven from DOUT. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). When data is being transmitted to the AD5532, the $\overline{\text{SYNC}}$ line is taken low (PC7). Data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. In order to transmit 10 data bits in SHA mode it is important to left-justify the data in the SPDR register. PC7 must be pulled low to start a transfer. It is taken high and pulled low again before any further read/write cycles can take place. A connection diagram is shown in Figure 23.

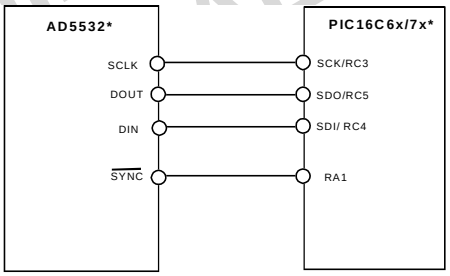


*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 23. AD5532 to 68HC11 Interface

AD5532 to PIC16C6x/7x

The PIC16C6x Synchronous Serial Port (SSP) is configured as an SPI Master with the Clock Polarity bit = 0. This is done by writing to the Synchronous Serial Port Control Register (SSPCON). See user PIC16/17 Microcontroller User Manual. In this example I/O port RA1 is being used to pulse $\overline{\text{SYNC}}$ and enable the serial port of the AD5532. This microcontroller transfers only eight bits of data during each serial transfer operation; therefore, two or three consecutive read/write operations are needed depending on the mode. Figure 24 shows the connection diagram.

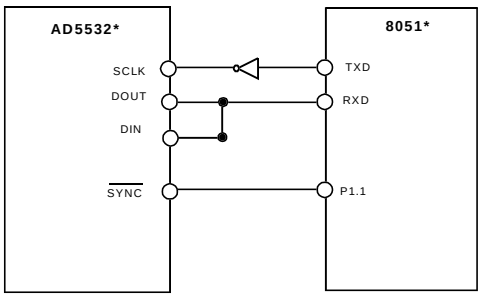


*Additional Pins omitted for clarity

Figure 24. AD5532 to PIC16C6x Interface

AD5532 TO 8051

The AD5532 requires a clock synchronized to the serial data. The 8051 serial interface must therefore be operated in Mode 0. In this mode serial data enters and exits through RXD and a shift clock is output on TXD. Figure x shows how the 8051 is connected to the AD5532. Because the AD5532 shifts data out on the rising edge of the shift clock and latches data in on the falling edge, the shift clock must be inverted. The AD5532 requires it's data with the MSB first. Since the 8051 outputs the LSB first, the transmit routine must take this into account.



*Additional Pins omitted for clarity

Figure 25. AD5532 to 8052 Interface

APPLICATION CIRCUITS

AD5532 in a typical ATE system

The AD5532 is ideally suited for use in Automatic Test Equipment. Several DACs are required to control pin drivers, comparators, active loads and signal timing. Traditionally Sample-and-Hold devices were used in this application.

The AD5532 has several advantages: no refreshing is required, there is no droop, pedestal error is eliminated and there in no need for extra filtering to remove glitches. Overall a higher level of integration is achieved in a smaller area. See below.

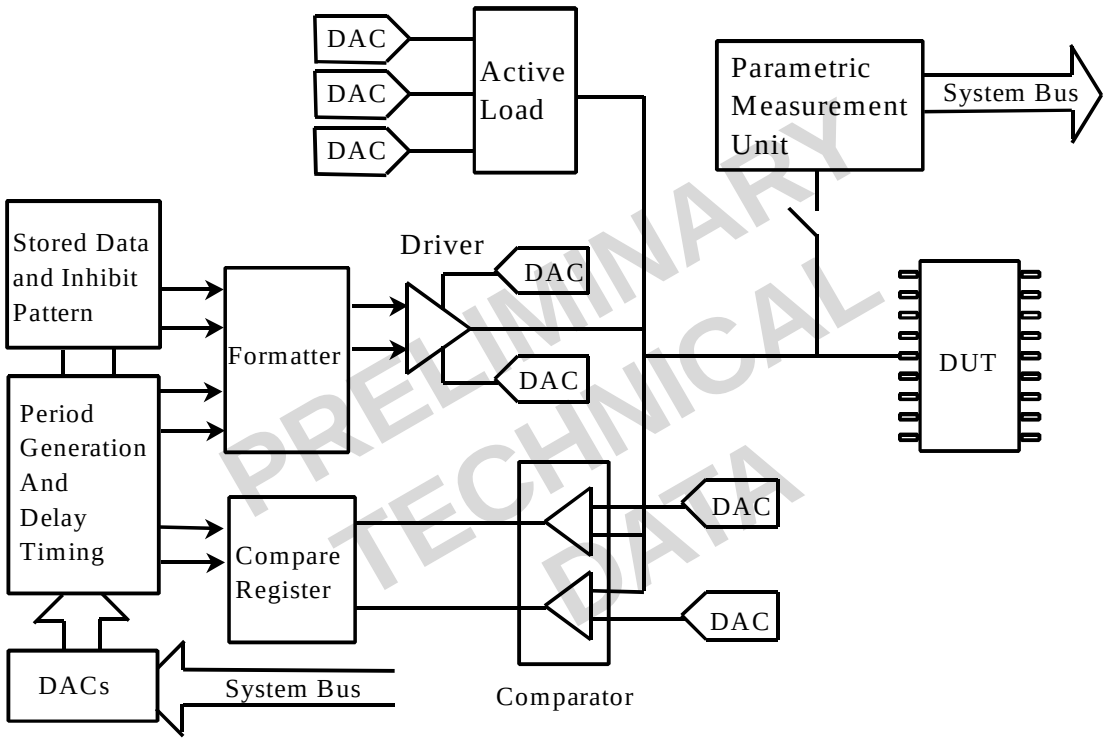


Figure 26. AD5532 in an ATE system

OUTLINE DIMENSIONS

Dimensions shown in mm.

74-lead LFBGA