a

Dual Channel, Gain-Ranging ADC with RSSI

PRELIMINARY TECHNICAL DATA AD6600

FEATURES
Dual "IF" Inputs, 70-250 MHz
Diversity or two independent IF signals
Separate Attenuation Paths
Oversample RF Channels
20 MSPS on a Single Carrier
10 MSPS/channel in Diversity Mode
Total Signal Range 90+ dB
30 dB from Automatic Gain-Ranging (AGC)
60 dB from A/D Converter
Range >100 dB after Processing Gain
Digital Outputs
11-Bit ADC Word
3-Bit RSSI Word
2X Clock, A/B Indicator
Single +5V Power Supply
Output DVCC +3.3V or +5V
775mW Power Dissipation

APPLICATIONS
Communications Receivers
PCS/Cellular Base Stations
GSM, CDMA, TDMA
Wireless Local Loop, Fixed Access

PRODUCT DESCRIPTION

The AD6600 mixed-signal receiver chip directly samples signals at analog input frequencies up to 250 MHz. The device includes two input channels, each with 1GHz input amplifiers and 30dB of automatic gain-ranging circuitry. Both channels are sampled with a 450MHz track-and-hold followed by an 11-bit, 20MSPS analog-to-digital converter. Digital RSSI outputs, an A/B channel indicator, a 2X Clock output, references, and control circuitry are all on-chip. Digital output signals are twos complement, CMOS-compatible and interface directly to +3.3V or +5V digital processing chips.

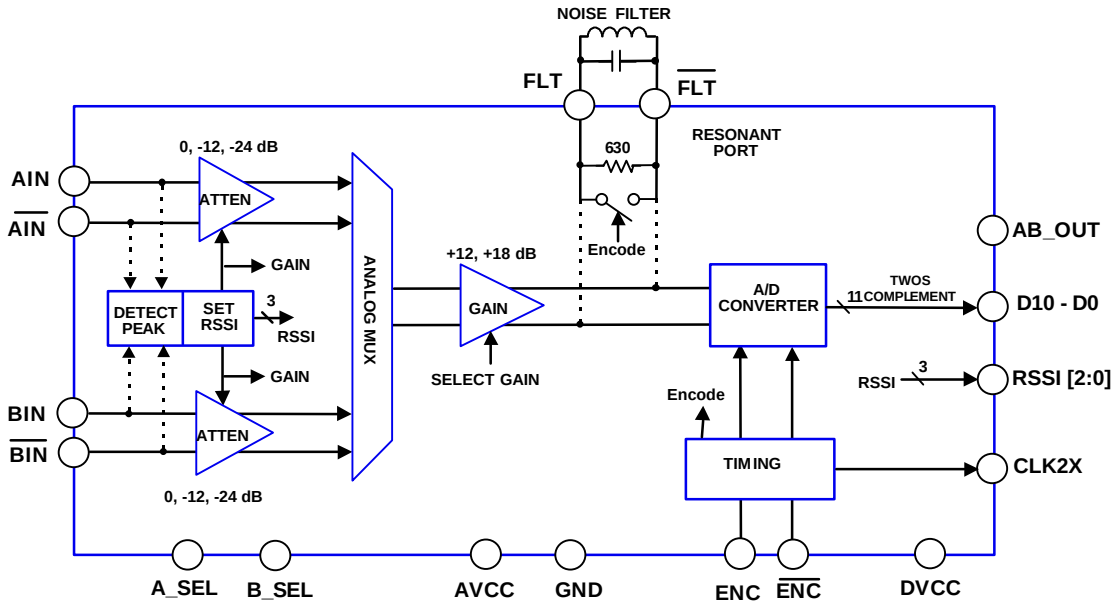
The primary use for the dual analog input structure is sampling both antennas in a two-antenna diversity receiver. However channels A and B may also be used to sample two, independent IF signals. Diversity, or dual-channel mode, is limited to 10 MSPS per channel. In single channel mode, the full clock rate of 20 MSPS may be applied to a single carrier.

The AD6600 may be used as a stand-alone sampling chip, or it may be combined with the AD6620 Digital Receive Signal Processor. The AD6620 provides 10-25dB of additional processing gain before passing data to a fixed or floating point DSP.

Driving the AD6600 is simplified by using the AD6630, differential IF amplifier. The AD6630 is easily matched to inexpensive SAW filters from 70 to 250 MHz.

Designed specifically for cellular/PCS receivers, the AD6600 supports GSM, IS-136, CDMA, Wireless LANs, as well as proprietary air interfaces used in WLL/fixed access systems.

Units are available in plastic, surface-mount packages (44-pin TQFP) and specified over the industrial temperature range (-40°C to +85°C).



FUNCTIONAL BLOCK DIAGRAM

AD6600 – SPECIFICATIONS

DC SPECIFICATIONS (AVCC = +5V, DVCC = +3.3V; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Temp	Test Level	AD6600AST Min	Typ	Max	Units
ANALOG INPUTS (AIN, $\overline{AIN}$ / BIN, $\overline{BIN}$)						
Differential Analog Input Voltage Range[1]	Full	V		2.0		V_{PP}
Differential Analog Input Resistance[2]	Full	IV	160	200	240	Ω
Differential Analog Input Capacitance	+25°C	V		1.5		pF
PEAK DETECTOR (internal), RSSI						
Resolution				3		Bits
RSSI Gain Step	Full	V		6		dB
RSSI Hysterisis[3]	Full	V		6		dB
RESONANT PORT (FLT, $\overline{FLT}$)						
Differential Port Resistance	Full	V		630		Ω
Differential Port Capacitance	Full	V		1.75		pF
A/D CONVERTER						
Resolution	Full	IV		11		Bits
ENCODE INPUTS (ENC, $\overline{ENC}$)						
Differential Input Voltage (ac-coupled)[4]	Full	IV	0.4			V_{PP}
Differential Input Resistance	+25°C	V		11		kΩ
Differential Input Capacitance	+25°C	V		2.5		pF
A/B MODE INPUTS (A_SEL, B_SEL)[5]						
Input High Voltage Range	Full	IV	4.75		5.25	V
Input Low Voltage Range	Full	IV	0.0		0.5	V
POWER SUPPLY						
Supply Voltages						
AVCC	Full	II	4.75	5.0	5.25	V
DVCC	Full	IV	3.0	3.3	5.25	V
Supply Current						
I_{AVCC} (AVCC = 5.0V)	Full	II		145	182	mA
I_{DVCC} (DVCC = 3.3V)	Full	II		15	20	mA
POWER CONSUMPTION[6]	Full	II		775	976	mW

NOTES
[1] Analog Input Range is a function of input frequency. See AC specifications for 70-250 MHz inputs.
[2] Analog Input Impedance is a function of input frequency. See AC specifications for 70-450 MHz inputs.
[3] Six dB of digital hysterisis is used to eliminate level uncertainty at the RSSI threshold points due to noise and amplitude variations.
[4] Encode inputs should be ac-coupled and driven differentially. See "Encoding the AD6600" for details.
[5] A_SEL and B_SEL should be tied directly to ground or AVCC.
[6] Maximum power consumption is computed as maximum current at nominal supplies.

DIGITAL SPECIFICATIONS (AVCC = +5V, DVCC = +3.3V; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter (Conditions)	Temp	Test Level	AD6600AST Min	Typ	Max	Units
LOGIC OUTPUTS (D10 - D0, AB_OUT, RSSI2-0)[1]						
Logic Compatibility				CMOS		
Logic "1" Voltage (DVCC = +3.3V)	Full	II	2.8	DVCC-0.2		V
Logic "0" Voltage (DVCC = +3.3V)	Full	II		0.2	0.5	V
Logic "1" Voltage (DVCC = +5.0V)	Full	IV	4.0	DVCC-0.35		V
Logic "0" Voltage (DVCC = +5.0V)	Full	IV		0.35	0.5	V
Output Coding (D10 - D0)				Twos Complement		
CLK2X OUTPUT[1,2]						
Logic "1" Voltage (DVCC = +3.3V)	Full	II	2.8	DVCC-0.2		V
Logic "0" Voltage (DVCC = +3.3V)	Full	II		0.2	0.5	V
Logic "1" Voltage (DVCC = +5.0V)	Full	IV	4.0	DVCC-0.3		V
Logic "0" Voltage (DVCC = +5.0V)	Full	IV		0.35	0.5	V

NOTES
[1] Digital output load is one LCX gate.
[2] CLK2X output voltage levels, high and low, tested at switching rate of 10MHz.

TIMING REQUIREMENTS & SWITCHING SPECIFICATIONS[1]

(AVCC = +5V, DVCC = +3.3V; ENC & $\overline{\text{ENC}}$ = 20 MSPS; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Name	Temp	Test Level	AD6600AST Min	Typ	Max	Units
A/D CONVERTER							
Conversion Rate	f_{ENC}				$1/(t_{ENC})$		MSPS
Maximum Conversion Rate		Full	II	20			MSPS
Minimum Conversion Rate		Full	IV			6	MSPS
Aperture Uncertainty	tj	+25°C	V		0.3		ps_{RMS}
ENCODE INPUTS (ENC, $\overline{\text{ENC}}$)[2]							
Period	t_{ENC}	Full	II	50			ns
Pulsewidth High[3]	t_{ENCH}	Full	IV	20			ns
Pulsewidth Low[4]	t_{ENCL}	Full	IV	20			ns
2X CLOCK OUTPUT (CLK2X)[5]							
Output Frequency		Full	V		$2*f_{ENC}$		MSPS
Output Period[6]	t_{CLK2X_1}	Full	V		t_{ENCL}		ns
	t_{CLK2X_2}	Full	V		t_{ENCH}		ns
CLK2X Pulsewidth Low[6]	t_{CLK2XL}	Full	V		$t_{ENCH}/2$		ns
Output Risetime[8]		Full	V		3		ns
Output Falltime[8]		Full	V		2.6		ns
OUTPUT RISE/FALL TIMES[9]							
Output Risetime (D10:D0, RSSI2:0)		Full	V		8		ns
Output Falltime (D10:D0, RSSI2:0)		Full	V		8.4		ns
Output Risetime (AB_OUT)		Full	V		6		ns
Output Falltime (AB_OUT)		Full	V		6.2		ns

NOTES

[1] See AD6600 Timing Diagrams.

[2] All switching specifications tested by driving ENC and $\overline{\text{ENC}}$ differentially.

[3] Several timing specifications are a function of Encode high time, t_{ENCH}; these specifications are shown in the data tables and timing diagrams. Encode duty cycle should kept as close to 50% as possible.

[4] Encode pulse low directly affects the amount of settling time available at FLT resonant port. See "External Analog (Resonant) Filter" section for details.

[5] The 2X Clock is generated internally, therefore some specifications are functions of encode period and duty cycle. All timing measurements to or from CLK2X are referenced to 2.0Vcrossing.

[6] This specification IS a function of Encode period and duty cycle; reference timing diagrams Figure 8.

[7] This specification IS NOT a function of Encode period and duty cycle.

[8] Output rise time is measured from 20% point to 80% point of total CLK2X voltage swing; output fall time is measured from 80% point to 20% point of total CLK2X voltage swing.

[9] Output rise time is measured from 20% point to 80% point of total data voltage swing; output fall time is measured from 80% point to 20% point of total data voltage swing. All outputs specified with 10pF load.

TIMING REQUIREMENTS & SWITCHING SPECIFICATIONS cont.[1]

(AVCC = +5V, DVCC = +3.3V; ENC & $\overline{\text{ENC}}$ = 20 MSPS, Duty Cycle = 50%; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Name	Temp	Test Level	AD6600AST Min	Typ	Max	Units
ENCODE/CLK2X							
Encode Rising to CLK2X Falling[6]	t_{CF}	Full	IV	6.5	8.0	9.5	ns
Encode Rising to CLK2X Rising[5]	t_{CR}	Full	IV		$t_{CF} + (t_{ENCH})/2$		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	25.7	27.2	28.7	ns
@ Encode = 20MSPS, 50% Duty Cycle		Full	IV	19.0	20.5	22.0	ns
CLK2X/DATA (D10:0, RSSI2:0)							
CLK2X to DATA Rising Low Delay[6]	t_{2X_DRL}	Full	IV	3.0	6.5		ns
CLK2X to DATA Hold Time[6]	t_{H_D2X}	Full	IV	3.0	6.5		ns
CLK2X to DATA Falling Low[6,8]	t_{2X_DFL}	25°C	IV	10.0	15.0	20.0	ns
		Full	IV	11.0	15.5	22.0	ns
CLK2X to DATA Setup Time[5]	t_{S_D2X}	Full	IV		$t_{ENCH} - t_{2X\_DFL}$		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	16.5	23.0		ns
@ Encode = 20MSPS, 50% Duty Cycle[8]		25°C	IV	5.0	10.0		ns
		Full	IV	3.0	9.5		ns
CLK2X/AB_OUT							
CLK2X to AB_OUT Rising Low Delay[6]	t_{2X_ARL}	Full	IV	7.0	11.0		ns
CLK2X to AB_OUT Hold Time[6]	t_{H_A2X}	Full	IV	7.0	11.0		ns
CLK2X to AB_OUT Falling Low Delay[6,8]	t_{2X_AFL}	25°C	IV	12.0	18.0	23.0	ns
		Full	IV	10.7	19.0	26.0	ns
CLK2X to AB_OUT Setup Time[5]	t_{S_A2X}	Full	IV		$t_{ENCH} - t_{2X\_AFL}$		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	12.5	19.5		ns
@ Encode = 20MSPS, 50% Duty Cycle[8]		25°C	IV	2.0	7.0		ns
		Full	IV	-1.0	6.0		ns
ENCODE/DATA (D10:0, RSSI2:0)							
ENCODE to DATA Rising Low Delay[5]	t_{EN_DRL}	Full	IV		$t_{CR} + t_{2X\_DRL}$		ns
ENCODE to DATA Hold Time[5]	t_{H_DEN}	Full	IV		t_{EN_DRL}		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	28.7	33.7		ns
@ Encode = 20MSPS, 50% Duty Cycle		Full	IV	22.0	27.0		ns
ENCODE to DATA Falling Low Delay[5]	t_{EN_DFL}	Full	IV		$t_{CR} + t_{2X\_DFL}$		ns
ENCODE to DATA Delay (Setup)[5]	t_{S_DEN}	Full	IV		$t_{ENC} - t_{EN\_DFL}$		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	26.2	34.2		ns
@ Encode = 20MSPS, 50% Duty Cycle[8]		25°C	IV	8.0	14.5		ns
		Full	IV	6.0	14.0		ns
ENCODE/AB_OUT							
ENCODE to AB_OUT Rising Low Delay[5]	t_{EN_ARL}	Full	IV		$t_{CR} + t_{2X\_ARL}$		ns
ENCODE to AB_OUT Delay (Hold)[5]	t_{H_AEN}	Full	IV		t_{EN_ARL}		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	32.7	38.2		ns
@ Encode = 20MSPS, 50% Duty Cycle		Full	IV	26.0	31.5		ns
ENCODE to AB_OUT Falling Low Delay[5]	t_{EN_AFL}	Full	IV		$t_{CR} + t_{2X\_AFL}$		ns
ENCODE to AB_OUT Delay (Setup)[5]	t_{S_AEN}	Full	IV		$t_{ENC} - t_{EN\_AFL}$		ns
@ Encode = 13MSPS, 50% Duty Cycle		Full	IV	22.2	30.7		ns
@ Encode = 20MSPS, 50% Duty Cycle[8]		25°C	IV	5.0	11.5		ns
		Full	IV	2	10.5		ns

NOTES

[1] See AD6600 Timing Diagrams.

[2] All switching specifications tested by driving ENC and $\overline{\text{ENC}}$ differentially.

[3] Several timing specifications are a function of Encode high time, t_{ENCH}; these specifications are shown in the data tables and timing diagrams. Encode duty cycle should kept as close to 50% as possible. Reference AD6600 Timing Diagrams

[4] The 2X Clock is generated internally, therefore some specifications are functions of encode period and duty cycle.

[5] This specification IS a function of Encode period and duty cycle.

[6] This specification IS NOT a function of Encode period and duty cycle.

[7] CLK2X referenced to 2.0Vcrossing; digital output levels referenced to 0.8 and 2.0V crossings; all outputs with 10pF load.

[8] For these particular specifications, the "+25°C" specification is valid from +25°C to +85°C. The "Full" temperature specification includes cold temperature extreme and covers the entire range, -40°C to +85°C.

AC SPECIFICATIONS

(AVCC = +5V, DVCC = +3.3V; ENC & $\overline{\text{ENC}}$ = 20 MSPS, Duty Cycle = 50%; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Temp	Test Level	AD6600AST Min	Typ	Max	Units
ANALOG INPUTS[1]						
Analog Input 3dB Bandwidth[2]	Full	V		450		MHz
Differential Analog Input Voltage Range						
70 MHz	Full	V		2.45		V_{PP}
150 MHz	Full	V		2.57		V_{PP}
200 MHz	Full	V		2.62		V_{PP}
250 MHz	Full	V		2.86		V_{PP}
Differential Analog Input Impedance[3]						
70 MHz	+25°C	V		197 - j24		Ω
150 MHz	+25°C	V		188 - j48		Ω
200 MHz	+25°C	V		175 - j57		Ω
250 MHz	+25°C	V		161 - j67		Ω
300 MHz	+25°C	V		151 - j73		Ω
350 MHz	+25°C	V		140 - j80		Ω
400 MHz	+25°C	V		141 - j75		Ω
450 MHz	+25°C	V		173 - j107		Ω
Full-scale Input Power						
70 MHz	Full	V		5.8		dBm
150 MHz	Full	V		6.3		dBm
200 MHz	Full	V		6.7		dBm
250 MHz	Full	V		7.7		dBm
Full-scale Gain Tolerance[4]						
70-250 MHz	Full	V		±0.5		dB
200 MHz[5]	+25°C	I	-1.0	±0.1	+1.0	dB
Gain Matching (Input A:B)						
70-250 MHz	Full	V		±0.1		dB
200 MHz	Full	II	-0.5	±0.05	+0.5	dB
Range-to-Range Gain Tolerance						
70-250 MHz	Full	V		±0.1		dB
Range-to-Range Phase Tolerance						
70 MHz	Full	V		0.2		degree
250 MHz	Full	V		0.5		degree
Channel Isolation[6]						
70– 250 MHz	Full	IV	45	50		dB
Noise[7]						
Minimum Attenuation Level	Full	V		34		µVrms
Maximum Attenuation Level	Full	V		869		µVrms
Attenuator 3OIP[8]	Full	V		+33		dBm

NOTES

[1] AIN, $\overline{\text{AIN}}$ / BIN, $\overline{\text{BIN}}$: The AD6600 analog inputs are unconditionally stable and guarantee proper operation over the 70-250MHz specified operating range. Circuit board layout is critical on this device, and proper PCB layout must be employed to achieve specified results.

[2] Analog Input 3dB Bandwidth is determined by internal track-and-hold. The front-end attenuators have a bandwidth of 1GHz

[3] Measured real and imaginary values using Network Analyzer.

[4] Full-scale gain tolerance is the typical variation in gain at a given IF input frequency. The nominal value for fullscale input power is a function of frequency as shown in previous specification.

[5] Fullscale gain tolerance measured at 200MHz analog input referenced to 6.7dBm nominal fullscale input power. For the gain measurement test, the input signal level is set to –6dBFS. Tuning port bandwidth is set to 50 MHz.

[6] Main channel set to fullscale input power. Diversity channel swept from –20dBFS to –90dBFS.

[7] Measurement includes thermal and quantization noise at 70MHz analog input. Tuning port bandwidth is set to 50MHz.

[8] Test tones at 160.05MHz and 170.05MHz.

AC SPECIFICATIONS cont.

(AVCC = +5V, DVCC = +3.3V; ENC & $\overline{\text{ENC}}$ = 20 MSPS, Duty Cycle = 50%; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Temp	Test Level	AD6600AST Min	Typ	Max	Units
Signal-to-Noise Ratio (SNR)[1,2,3]						
AIN = 70 MHz						
@ -1dBFS	+25°C	IV	55	59		dB
@ -6dBFS	+25°C	V		54.5		dB
@ -10dBFS	+25°C	IV	45	49		dB
@ -12dBFS to -42dBFS	+25°C	IV	41	48±6		dB
@ -54dBFS	+25°C	IV	31	34		dB
AIN = 150 MHz						
@ -1dBFS	+25°C	IV	55	58		dB
@ -6dBFS	+25°C	V		54		dB
@ -10dBFS	+25°C	IV	45	49		dB
@ -12dBFS to -42dBFS	+25°C	IV	41	48±6		dB
@ -54dBFS	+25°C	IV	31	34		dB
AIN = 200 MHz						
@ -1dBFS[1]	+25°C	I	55	57.5		dB
@ -6dBFS[1]	+25°C	V		53.5		dB
@ -10dBFS[1]	+25°C	I	45	49		dB
@ -12dBFS to -42dBFS[2]	+25°C	I	41	48±6		dB
@ -54dBFS[3]	+25°C	I	31	34		dB
AIN = 250 MHz						
@ -1dBFS	+25°C	IV	52	56		dB
@ -6dBFS	+25°C	V		53.5		dB
@ -10dBFS	+25°C	IV	43	49		dB
@ -12dBFS to -42dBFS	+25°C	IV	40	48±6		dB
@ -54dBFS	+25°C	IV	30	34		dB
2nd HARMONIC						
AIN = 70 MHz						
@ -1dBFS	Full	V		69		dBc
@ -6dBFS	Full	V		68		dBc
@ -12dBFS to -42dBFS	Full	V		68±6		dBc
AIN = 150 MHz						
@ -1dBFS	Full	V		60		dBc
@ -6dBFS	Full	V		59		dBc
@ -12dBFS to -42dBFS	Full	V		67±6		dBc
AIN = 200 MHz[1,2,3]						
@ -1dBFS	+25°C	I	50	60		dBc
@ -6dBFS	Full	V		56		dBc
@ -10dBFS	+25°C	I	48	55		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc
@ -54dBFS	Full	V		50		dBc
AIN = 250 MHz						
@ -1dBFS	Full	V		54		dBc
@ -6dBFS	Full	V		52		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc

NOTES

[1] Measurements at -1dFBS, -6dBFS, and -10dBFS are in highest attenuation mode, RSSI = 101

[2] Each gain-range is checked at ~3dB from RSSI trip point (not in hysterisis); nominally -16dBFS (RSSI = 100), -22dBFS (RSSI = 011), -28dBFS (RSSI = 010), -35dBFS (RSSI = 001).

[3] Measurement at -54 dBFS is in the lowest attenuation mode, RSSI = 000.

AC SPECIFICATIONS cont.

(AVCC = +5V, DVCC = +3.3V; ENC & $\overline{ENC}$ = 20 MSPS, Duty Cycle = 50%; TMIN = -40°C, TMAX = +85°C unless otherwise specified)

Parameter	Temp	Test Level	AD6600AST Min	Typ	Max	Units
3rd HARMONIC						
AIN = 70 MHz						
@ -1dBFS	Full	V		77		dBc
@ -6dBFS	Full	V		76		dBc
@ -12dBFS to -42dBFS	Full	V		67±6		dBc
AIN = 150 MHz						
@ -1dBFS	Full	V		65		dBc
@ -6dBFS	Full	V		70		dBc
@ -12dBFS to -42dBFS	Full	V		66±6		dBc
AIN = 200 MHz[1,2,3]						
@ -1dBFS	+25°C	I	50	55		dBc
@ -6dBFS	Full	V		58		dBc
@ -10dBFS	+25°C	I	55	66		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc
@ -54dBFS	Full	V		62		dBc
AIN = 250 MHz						
@ -1dBFS	Full	V		50		dBc
@ -6dBFS	Full	V		56		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc
WORST OTHER SPUR (4th or higher)						
AIN = 70 MHz						
@ -1dBFS	Full	V		74.5		dBc
@ -6dBFS	Full	V		71		dBc
@ -12dBFS to -42dBFS	Full	V		68±6		dBc
AIN = 150 MHz						
@ -1dBFS	Full	V		67		dBc
@ -6dBFS	Full	V		65		dBc
@ -12dBFS to -42dBFS	Full	V		67±6		dBc
AIN = 200 MHz						
@ -1dBFS	+25°C	I	60	67		dBc
@ -6dBFS	Full	V		66		dBc
@ -10dBFS	+25°C	I	55	66		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc
AIN = 250 MHz						
@ -1dBFS	Full	V		66.5		dBc
@ -6dBFS	Full	V		65		dBc
@ -12dBFS to -42dBFS	Full	V		65±6		dBc

NOTES

[1] Measurements at -1dFBS, -6dBFS, and -10dBFS are in highest attenuation mode, RSSI = 101

[2] Each gain-range is checked at ~3dB from RSSI trip point (not in hysterisis); nominally -16dBFS (RSSI = 100), -22dBFS (RSSI = 011), -28dBFS (RSSI = 010), -35dBFS (RSSI = 001).

[3] Measurement at -54 dBFS is in the lowest attenuation mode, RSSI = 000.

AD6600 – SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
AVCC Voltage	0	7	V
DVCC Voltage	0	7	V
Analog Input Voltage[2]	0	AVCC	V
Analog Input Current[2]		25	mA
Digital Input Voltage[3]	0	AVCC	V
Output Current[4]		4	mA
Resonant Port Voltage[5]	0	AVCC	V
ENVIRONMENTAL[6]			
Operating Temperature Range (Ambient)	-40	+85	°C
Maximum Junction Temperature		+150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	-65	+150	°C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Pins AIN, $\overline{\text{AIN}}$, BIN, $\overline{\text{BIN}}$

[3] Pins ENC, $\overline{\text{ENC}}$, A_SEL, B_SEL

[4] Pins D10:0, RSSI2:0, AB_OUT, CLK2X

[5] Pins FLT, $\overline{\text{FLT}}$

[6] Typical thermal impedance (44-pin TQFP); θ_{JC} = 16°C/W, θ_{JA} = 55°C/W

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at temperature extremes.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6600AST	-40°C to +85°C (Ambient)	44-Terminal TQFP (Thin Quad Plastic Flatpack)	ST-44
AD6600ST/PCB		Evaluation Board with AD6600AST	

CAUTION

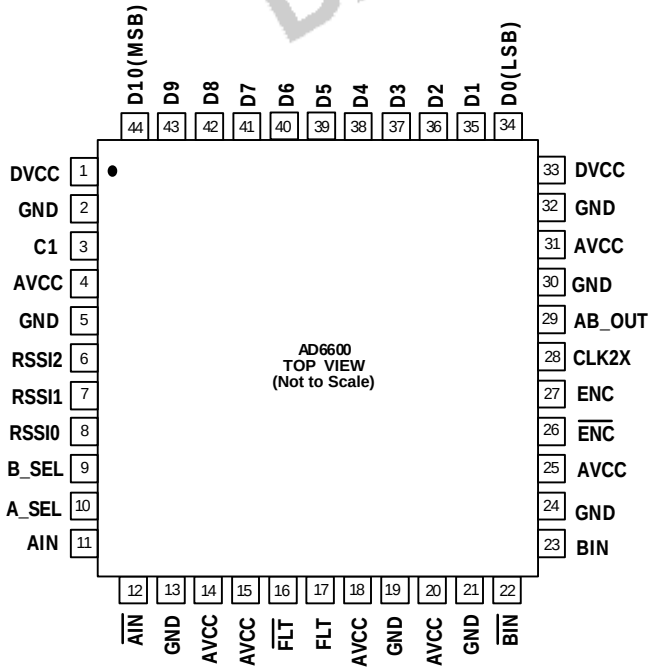
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6600 features proprietary protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Function
1, 33	DVCC	Digital VCC for Digital outputs. Can be +3.3V.
2, 5, 13, 19, 21, 24, 30, 32	GND	Ground.
3	C1	Internal bias point. Bypass by .01 µF to GND.
4, 14, 15, 18, 20, 25, 31	AVCC	+5 V power supply.
6-8	RSSI[2:0]	RSSI digital output bits.
9, 10	B_SEL, A_SEL	Mode Select pins for analog input channel A and B sampling.
11	AIN	True analog input channel A.
12	$\overline{\text{AIN}}$	Complementary analog input channel A.
16, 17	$\overline{\text{FLT}}$, FLT	Resonant Filters pins for external LC noise filter.
22	$\overline{\text{BIN}}$	Complementary analog input channel B.
23	BIN	True analog input channel B.
26	$\overline{\text{ENC}}$	Complementary Encode input.
27	ENC	True Encode input.
28	CLK2X	2 x clock output used for clocking digital filter chips.
29	AB_OUT	Digital output flag indicating whether output is input A (high) or B (low).
34	D0	Digital data output bit (Least significant bit)[1]
35 - 43	D1-D9	Digital data output bits[1]
44	D10	Digital data output bit (Most significant bit)[1]

NOTES
[1]Digital Outputs (D10:D0) in Twos Complement Format

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB. The bandwidth is determined by the internal track-and-hold when the filter node is resonated.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Attenuator 3OIP
The third order intercept point of the front end of the AD6600. It is the point where the third order products would theoretically intercept the input signal level if the input level could increase without bounds. This is measured using the ADC within the AD6600 while the input is stimulated with dual tones in the minimum attenuation (i.e. maximum gain) range.

Channel Isolation
The amount of signal leakage from one channel to the next when one channel is driven with a fullscale input, and the other channel is swept from –20 dBFS to –90dBFS with a frequency offset. The leakage is measured on the side with the smaller signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance and Differential Analog Input Impedance
The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range
The peak to peak differential voltage that must be applied to the converter to generate a fullscale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

Differential Nonlinearity
The deviation of any code width from an ideal 1 LSB step.

Differential Resonant Port Resistance
The resistance shunted across the resonant port (nominally 630 ohms). Used to determine the filter bandwidth and gain of that stage.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a give clock rate, these specs define an acceptable Encode duty cycle.

Fullscale Gain Tolerance
Unit to unit variation in fullscale input power.

Fullscale Input Power
Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10\log\left(\frac{\frac{V^2_{Fullscale_{rms}}}{Z_{Input}}}{.001}\right)$$

Gain Matching (Input A:B)
Variation in fullscale power between A and B inputs.

Harmonic Distortion, 2nd
The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, 3rd
The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Noise (for any range within the ADC)

$$V_{noise} = \sqrt{Z * .001 * 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the fullscale of the device for the frequency in question, SNR is the value for the particular input level and Signal is the signal level within the ADC reported in dB below fullscale. This value includes both thermal and quantization noise.

DEFINITIONS OF SPECIFICATIONS cont.

Range-Range Gain Tolerance
The gain error in the RSSI attenuator ladder from one range to the next.

Range-Range Phase Tolerance
The phase error in the RSSI attenuator ladder from one range to the next.

Differential Resonant Port Capacitance
The capacitance between the two resonant pins. Used to determine filter bandwidth and resonant frequency.

RSSI Gain Step
The input amplitude span between taps of the RSSI (received signal strength) attenuator ladder. Ideally each stage should span 6 dB of input power.

RSSI Hysterisis
The amount of movement in the RSSI switch points depending on the direction of approach. Hysterisis prevents unnecessary RSSI toggling when input signal power is near a threshold.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Worst Other Spur
The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the 2nd and 3rd harmonic) reported in dBc.

AD6600 TRANSFER FUNCTION

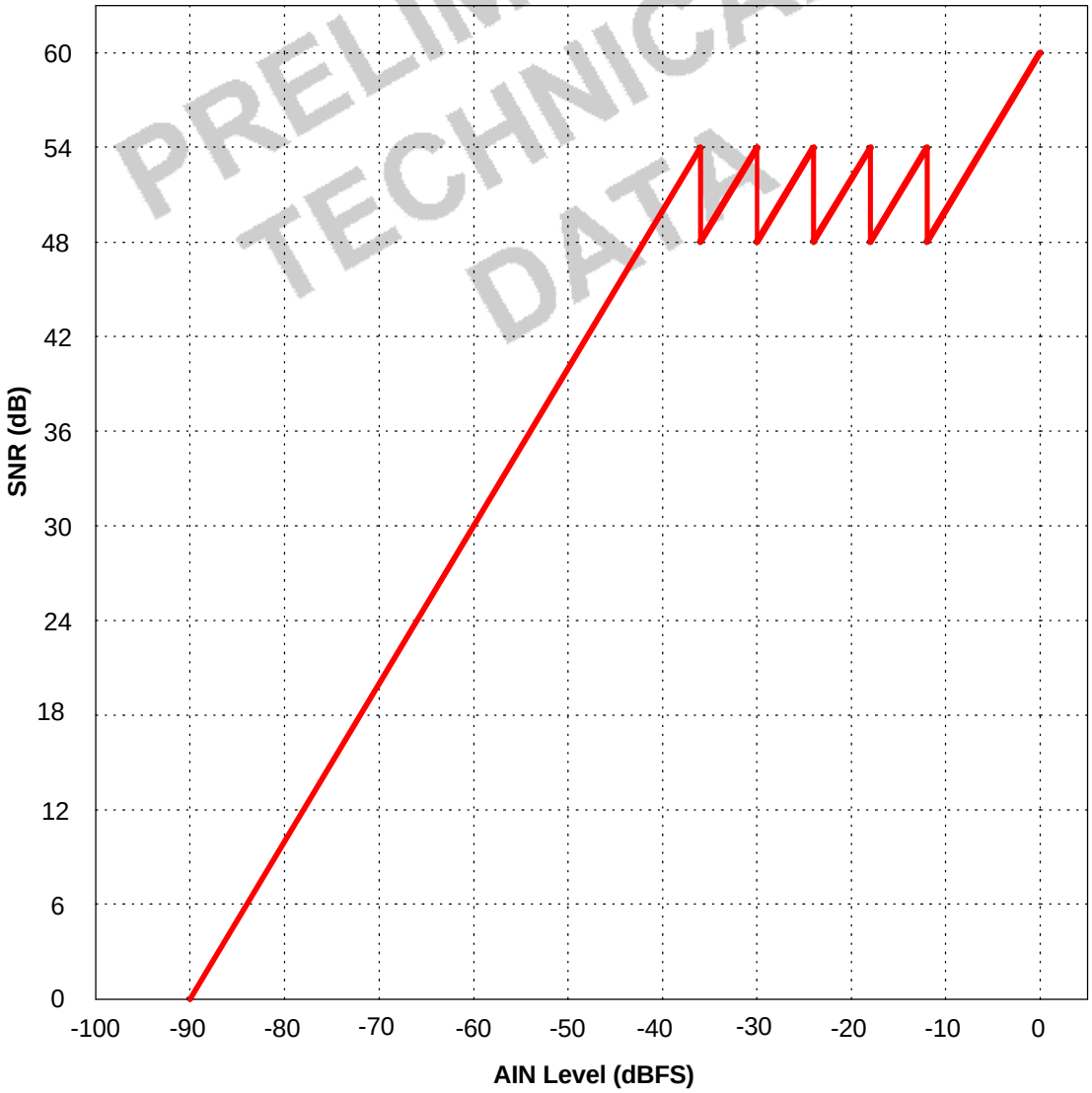


Figure 1. AD6600 SNR versus Input Power

EQUIVALENT CIRCUITS

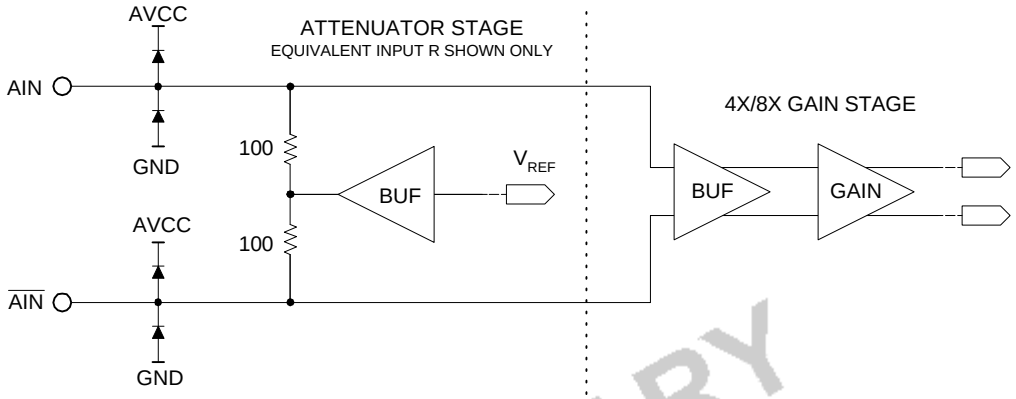


Figure 2. Analog Input Stage (Channel A shown; Channel B is equivalent)

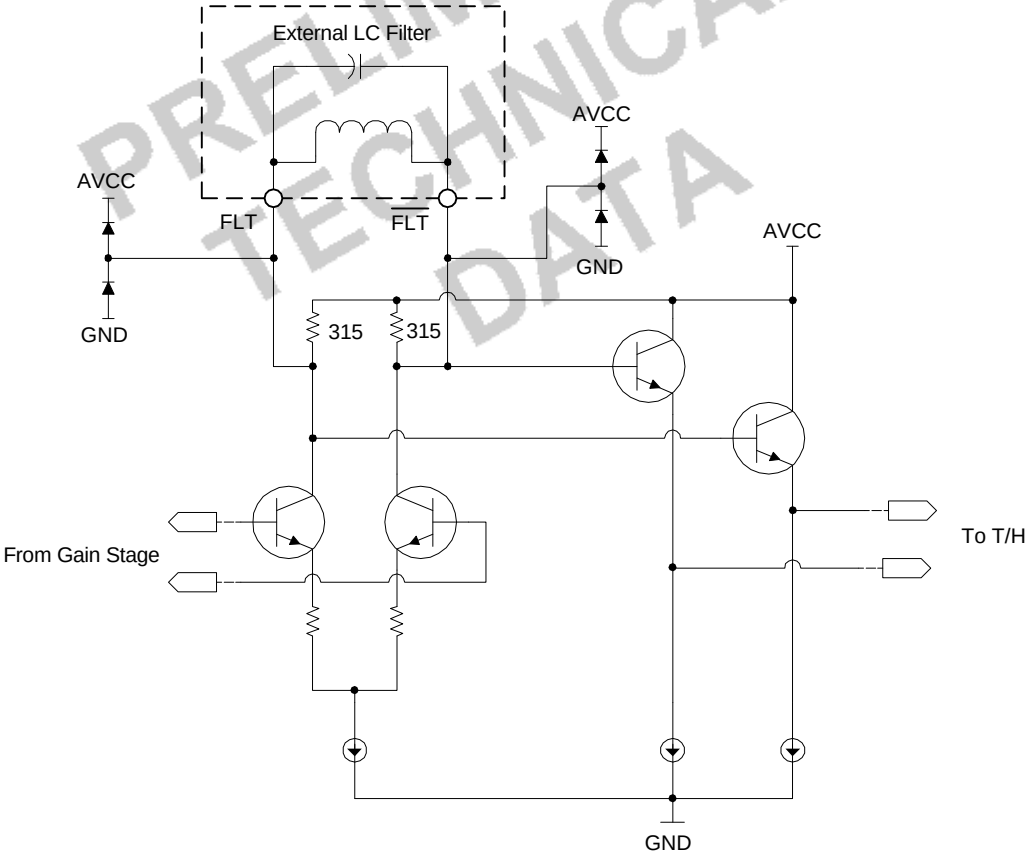


Figure 3. Resonant (LC Noise Filter) Port

EQUIVALENT CIRCUITS cont.

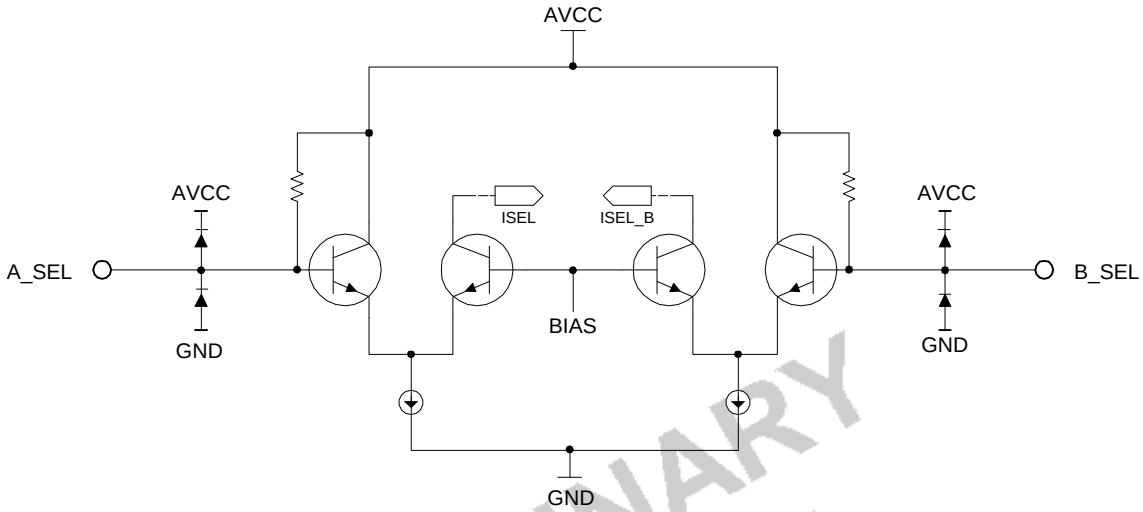


Figure 4. A_SEL, B_SEL Input Mode Pins

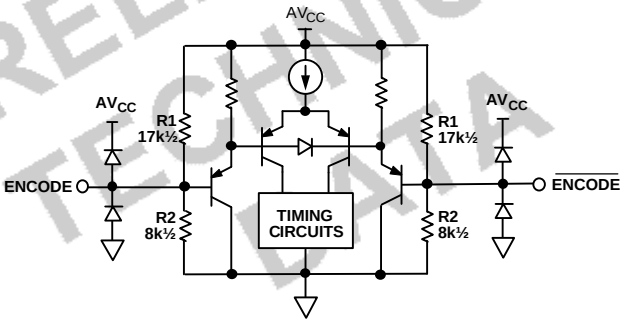


Figure 5. Encode Inputs

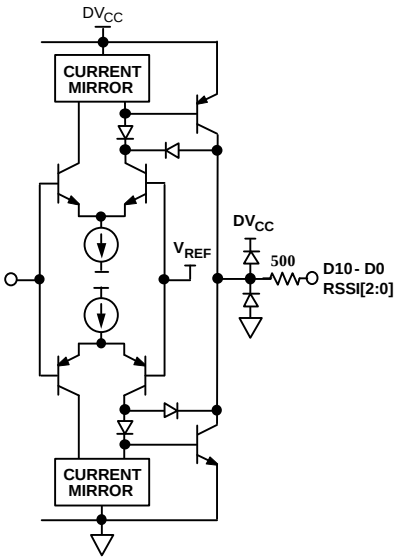


Figure 6. Digital Outputs

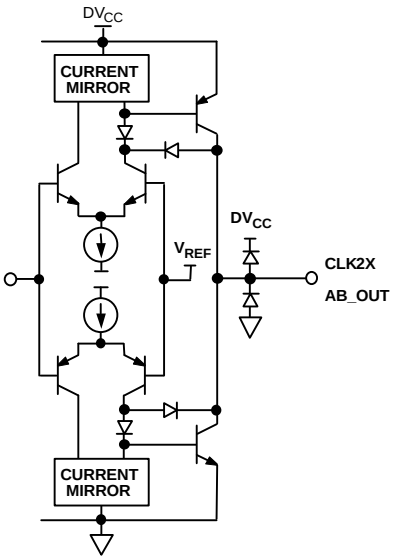


Figure 7. CLK2X, AB_OUT Outputs

AD6600 TIMING DIAGRAMS

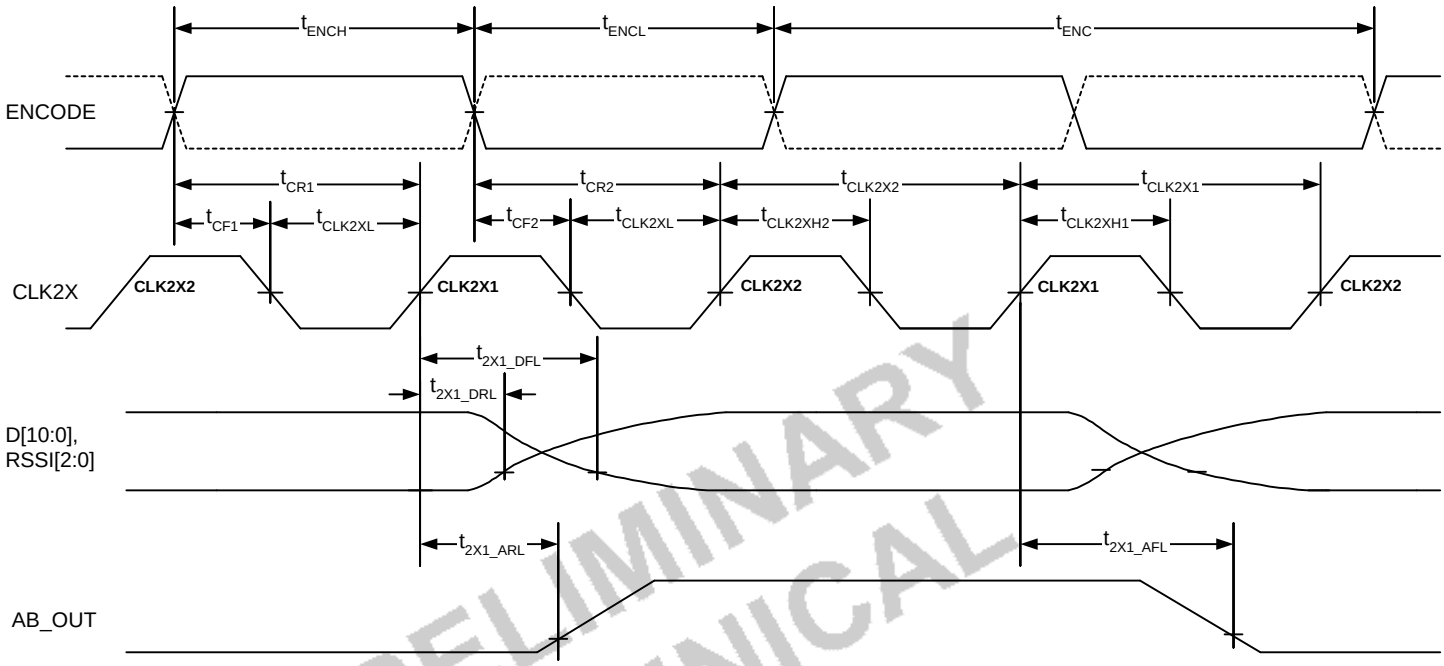


Figure 8. Encode to CLK2X Delays and CLK2X Propagation Delays

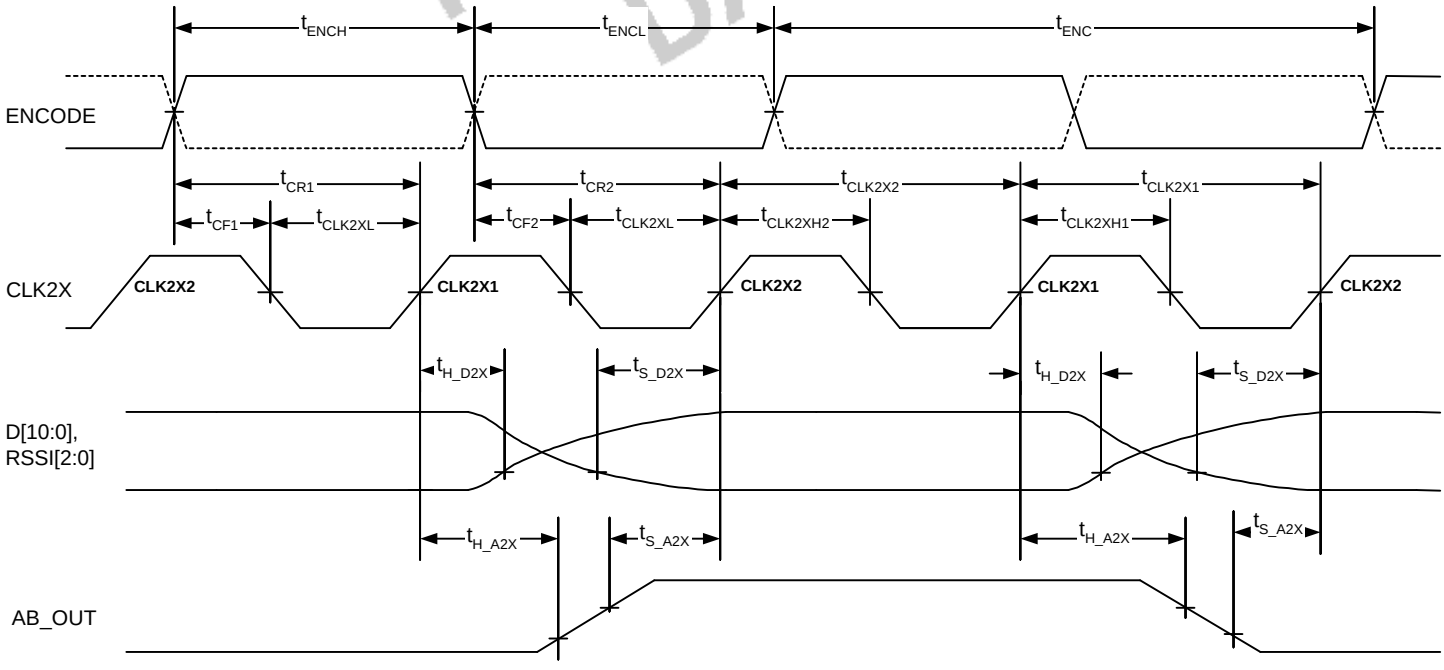


Figure 9. CLK2X Setup and Hold Time Characteristics

AD6600 TIMING DIAGRAMS cont.

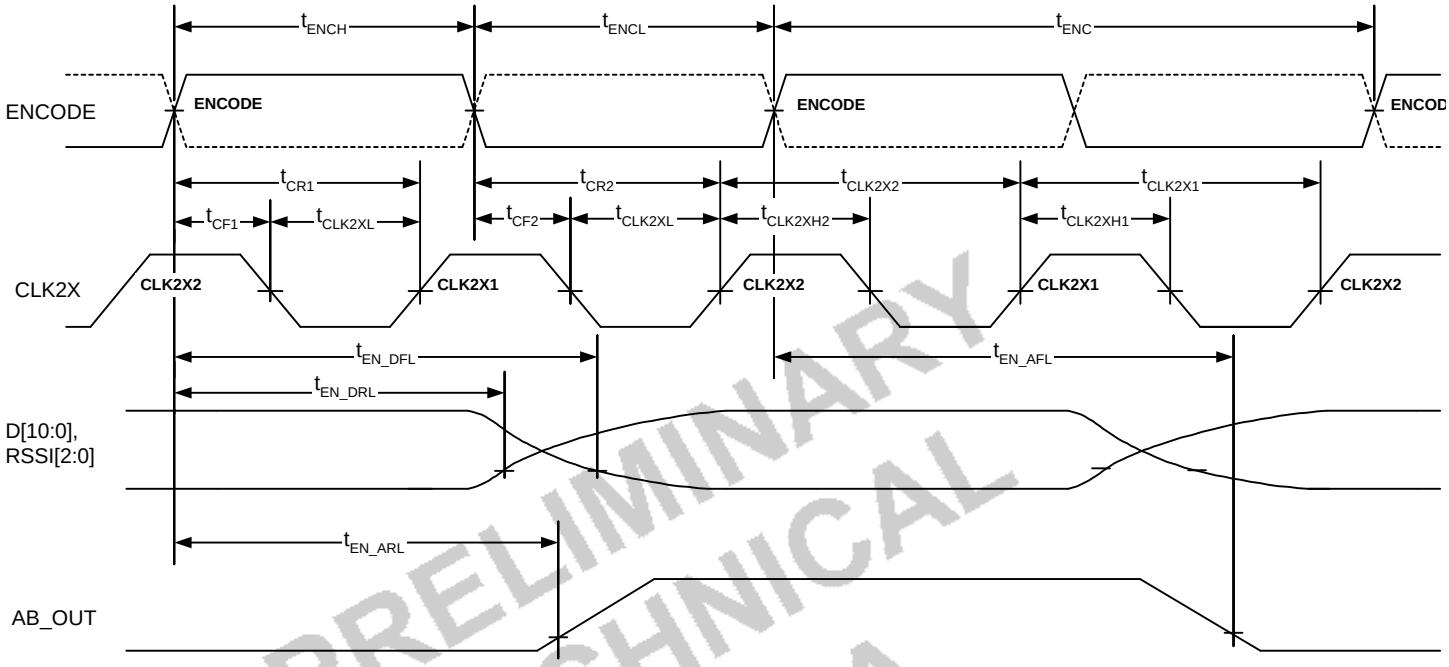


Figure 10. Encode to CLK2X Delays and Encode Propagation Delays

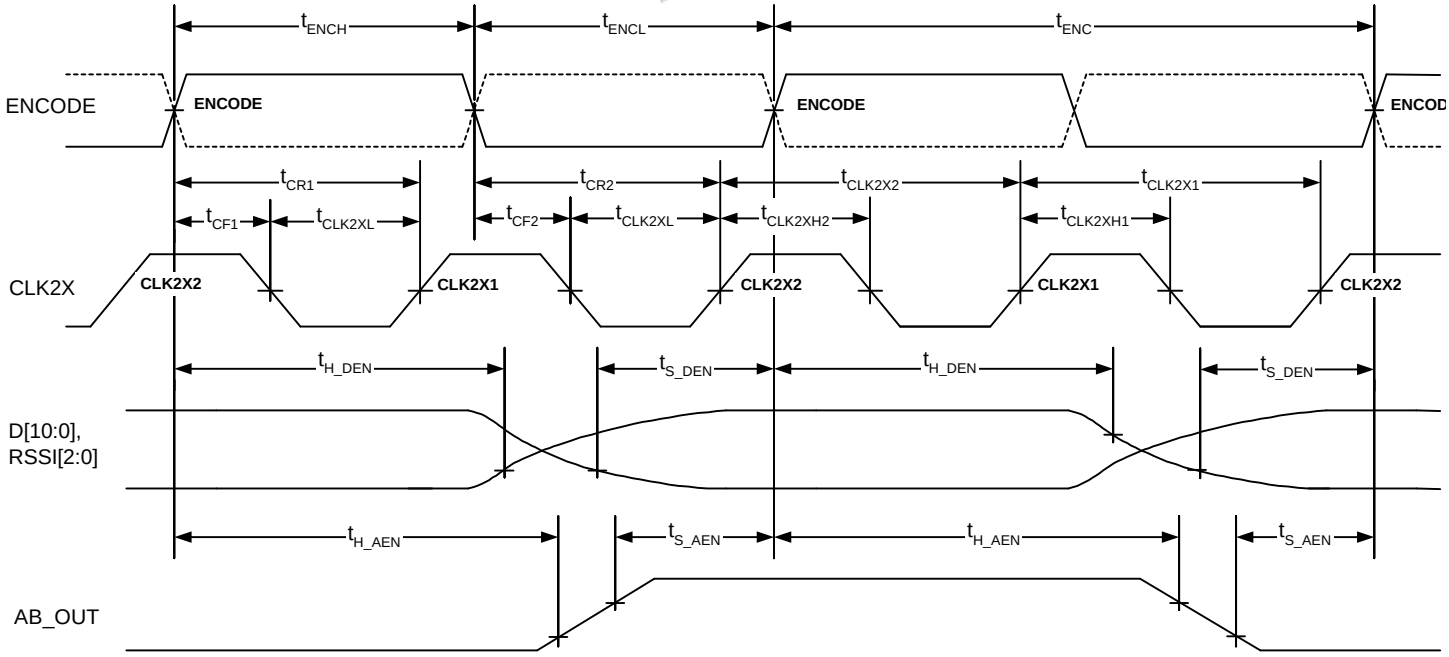


Figure 11. Encode Setup and Hold Time Characteristics

AD6600 TIMING DIAGRAMS cont.

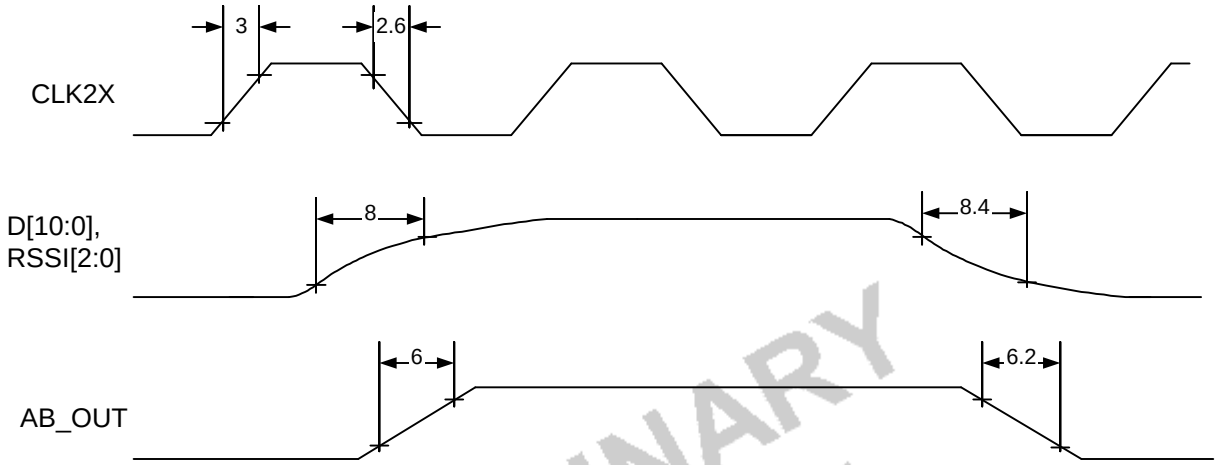


Figure 12. Typical Output Rise and Fall Times

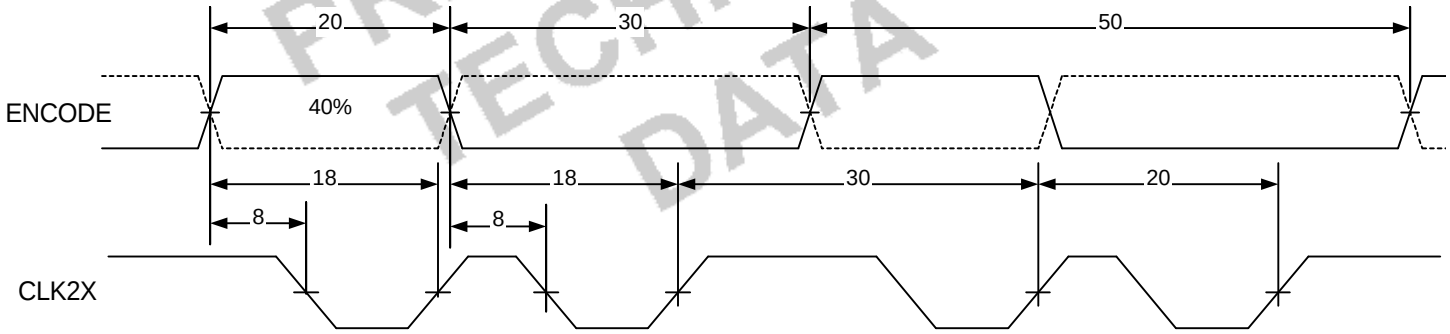


Figure 13. Encode = 20 MSPS, Duty Cycle = 40%

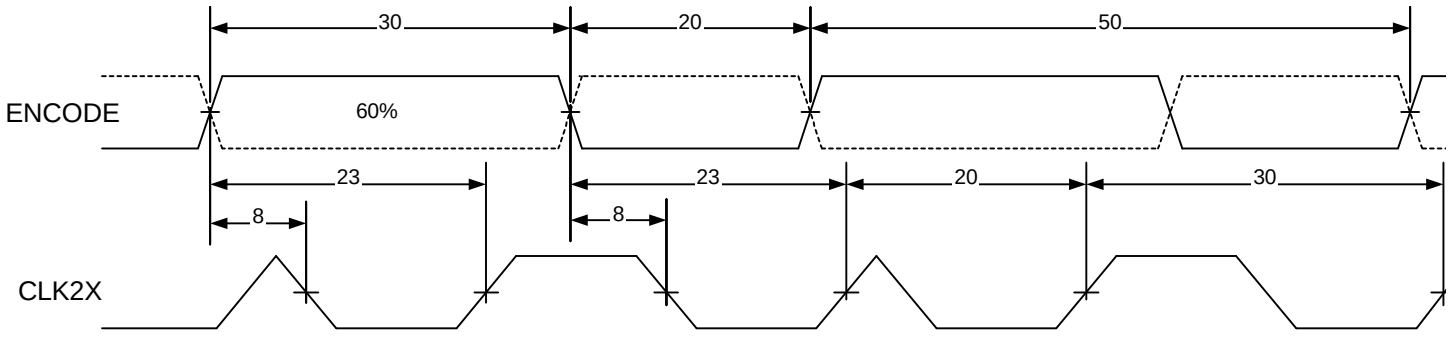
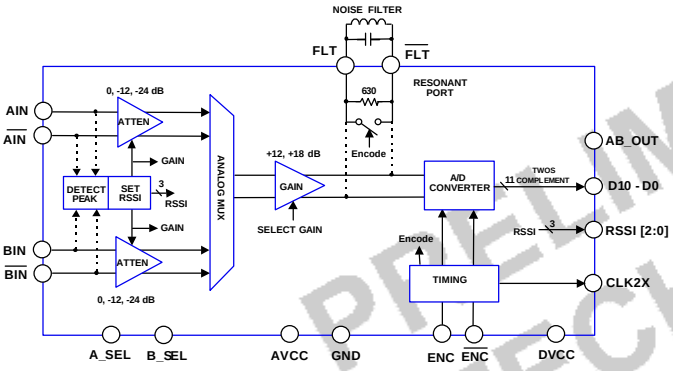


Figure 14. Encode = 20 MSPS, Duty Cycle = 60%

THEORY OF OPERATION

The AD6600, dual-channel, gain-ranging ADC integrates analog IF circuitry with high-speed data conversion. Each analog input stage is a 1GHz, 0 to -24dB, phase-compensated step attenuator; the step size in each attenuator is 12dB. Both input stages drive an analog multiplex function followed by a +12/+18 dB gain amplifier. A simple LC noise filter at the output of the gain amplifier is required to resonate at the desired IF. This resonant filter port precedes a wide input bandwidth (450MHz) track-and-hold followed by an 11-bit analog-to-digital converter (ADC). A high-speed synchronous peak detector monitors signal strength at both input channels. The peak detector drives RSSI circuitry that automatically adjusts attenuation and gain on a clock by clock basis. Both the three RSSI indicator bits and the eleven ADC bits are available at the output providing an exponent and mantissa data format. Together these integrated components form an IF sampling, high dynamic range ADC system.



It is helpful to view this device as a stand-alone ADC using automatic gain control. The gain-control referred to in this data sheet as gain-ranging, works to maintain a constant SNR over as wide a range as possible.

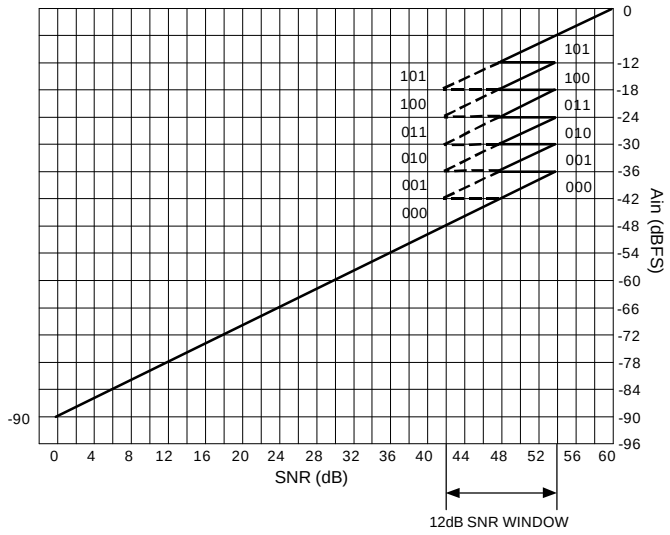


Figure 15. SNR for Gain-Ranging ADC

As stated previously, the AD6600 has a floating-point output: eleven mantissa bits and three exponent bits. As shown in Figure 15, at the lowest input levels SNR increases 1dB for a 1dB increase in input power. In this range, the AD6600 is set for maximum gain. However when the input signal level gets into the gain-ranging section (approx. -42dBFS), the SNR is contained between about 50 and 56 dB or between 44 and 56 including the effects of hysterisis. Although the graph above does not indicate so, there are slight differences between the SNR from one gain range to the next as the gain amp switches between 12dB and 18dB. Once the final RSSI range has been exceeded (approx. -12dBFS), SNR again increases 1 dB per 1 dB input power increase until converter fullscale is reached. Again, this performance is very much like the effects of a typical analog AGC loop.

AD6600 SUBCIRCUITS

Input Step Attenuator and Gain Stage

The AD6600 has two identical input attenuators, channel A and channel B. These dual inputs are typically used as diversity channels but may also process two independent IF signals. For maximum oversampling the device is used in single channel mode; in this case only one input channel is required. The attenuator steps are 0, -12 and -24 dB. The attenuator settings are based on the decisions of the RSSI stage (ref. Peak Detector/RSSI section). The outputs of the attenuators connect to an analog multiplexer that selects either channel A or B for subsequent processing (ref. Input Mode). The selected signal drives a dual-gain amplifier set to either +12 or +18 dB; the selected gain is also determined by the RSSI stage. Therefore, based on all possible combinations of attenuation and gain, the input signal receives -12 to +18 dB of voltage gain in 6 dB steps (Table 1). Overall gain-matching is typically within 0.1dB. And with a bandwidth of 1 GHz, the phase delay through the front-end ranges from 0.2 to 0.5 degrees depending on input frequency. Additionally, the input impedance does not change with attenuator settings so there is no AM to PM distortion.

Attenuator	Gain Amp	Total	RSSI Word
0 dB	+18 dB	+18 dB	000
0 dB	+12 dB	+12 dB	001
-12 dB	+18 dB	+6 dB	010
-12 dB	+12 dB	0 dB	011
-24 dB	+18 dB	-6 dB	100
-24 dB	+12 dB	-12 dB	101

Table 1. Attenuator and Gain Settings

High Speed Peak Detector and RSSI Circuitry

The peak detector along with the attenuator and dual gain amplifier form the control loop within the AD6600.

The peak detector is designed to follow the analog input one clock cycle before the conversion is actually made. Therefore, while the converter section of the AD6600 is converting sample 'n', the peak detector is already looking at sample 'n+1'. While looking at the 'n+1' sample (the calibration period), the peak detector examines the envelope of the input signal. The more of an envelope that is tracked, the more accurate the gain setting. At the very least, the peak detector must be presented either a positive or negative sinusoidal peak, which represents about ½ of a cycle of a sine wave.

Since the peak detector works for a complete cycle prior to conversion, the absolute minimum IF frequency that can be determined is twice the sample rate per channel. Therefore at 15 MSPS, the minimum IF frequency that can be sampled would be 30 MHz.

Note that the more cycles of the input that are monitored by the peak detector, the more accurate the gain setting will be. Therefore, the actual minimum IF frequency recommended is higher than this. The minimum specified frequency is 70 MHz. Since the RSSI control loop is performed on a sample by sample basis, the AD6600 follows the signals into and out of a deep fade very accurately.

Hysterisis
The AD6600 employs hysterisis to prevent the gain-ranging from unnecessarily changing when the signal envelope is near an RSSI threshold. The hysterisis is digital and will account for exactly 6 dB of shift depending on whether the signal is increasing or decreasing. This effect is shown in the dashed lines of the overall transfer function, Figure 15.

External LC Noise Filter, Resonant Port
The output of the attenuator/gain stage drives the wide bandwidth track-and-hold (T/H), followed by the ADC encoder. Because the attenuator/gain stage has a very wide bandwidth (~1 GHz), an LC filter or "resonant port" is provided to limit the amount of wideband noise delivered to the ADC. The simple LC filter does not provide signal selectivity and should typically be 35 to 50 MHz wide. However, because the ADC's track-and-hold itself has a wide bandwidth (~450MHz), this noise-limiting filter is critical to meeting overall sensitivity. Specific details on selecting components for the resonant port are provided later in the text (Understanding the External Analog Filter).

ADC Encoder
After the calibration period is complete (one clock cycle), the appropriate gain and attenuator settings are determined and set. Once settled, the internal track-and-hold freezes the input signal so that the ADC encoder may digitize the signal. During digitization, the peak detector/RSSI circuitry is already looking at the next sample. When the AD6600 is in dual channel mode, the process is interleaved: while channel B is monitored for signal strength, channel A is digitized. This allows the RSSI to update on a clock by clock basis.

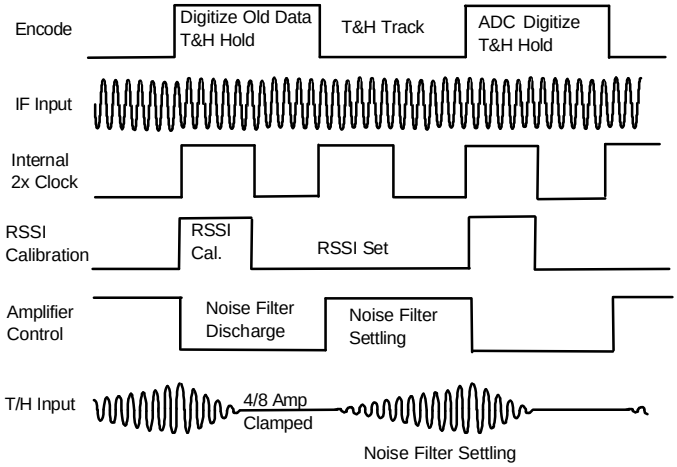


Figure 16. AD6600 Internal Timing

Figure 16 shows internal timing of how the chip works. The encode applied to the device initiates several actions. The first and most important is that the track-and-hold is placed in hold thus sampling the analog input at that instant. The second action is that the peak detector of the RSSI circuitry is initialized. During this period, the analog input envelope is monitored to determine signal power. The AD6600 is in calibration mode for about one quarter of the encode period.

While the AD6600 is in calibration, the external noise filter is discharged and the amplifier driving the filter disabled. Since this filter is shared between the two input channels in dual channel mode, this greatly reduces the feed-though between the channels that would otherwise exist. One quarter of an encode period after the calibration is complete, the amplifier is re-enabled and allowed to settle to its new signal conditions for sampling by the wideband T/H on the next encode signal. The final action is that the signal on the resonant port is sampled by the track-and-hold. This happens on the next rising edge of the encode.

Input Mode Select
The AD6600 has two operating modes: single channel and dual channel. In single channel mode, the ADC always samples channel A or always samples channel B. In dual channel mode, the ADC converter is sampling channel A and channel B on alternating Encode cycles. Two control pins are provided to select the desired mode of operation. A_SEL and B_SEL arbitrate the selection of how these input channels are connected to the output. Table 2 shows the truth table for selection of the input.

Mode	A_SEL	B_SEL	Output vs. Encode Clock n	n+1	n+2	n+3
Dual: A/B	1	1	A	B	A	B
Single: A	1	0	A	A	A	A
Single: B	0	1	B	B	B	B
Not Valid	0	0	-	-	-	-

Table 2. Selecting AD6600 Operating Mode

A_SEL and B_SEL are not logic inputs and should be tied directly to ground or analog VCC (+5 volts analog).

In dual channel mode, the AB_OUT signal indicates which input is currently available on the digital output. When the AB_OUT is 1, the digital output is the digitized version of channel A. Likewise, when AB_OUT is 0, the channel B is available on the digital output (Table 3).

A_SEL & B_SEL = 1	Outputs Data vs. Encode Clock			
	n	n+1	n+2	n+3
D[10:0], RSSI[2:0]	A	B	A	B
ABOUT	1	0	1	0

Table 3. ABOUT for Dual Channel Operation

Data Output Stage
The output stage provides data in the form of mantissa, D[10:0], and exponent, RSSI[2:0] where D[10:0] represents the output of the 11-bit ADC coded as twos complement, and RSSI[2:0] represents the gain-range setting coded in offset binary. Table 4 shows the nominal gain-ranges for a nominal, 2Vpp differential fullscale input. Keep in mind that the actual fullscale input voltage and power will vary with input frequency.

Differential Analog Input Voltage (V_{PP})	RSSI [2:0]		Attenuation or Gain (dB)
	Binary	Decimal Equiv.	
0.5 < Vin	101	5	-12
0.25 < Vin < 0.5	100	4	-6
0.125 < Vin < 0.25	011	3	0
0.0625 < Vin < 0.125	010	2	+6
0.03125 < Vin < 0.0625	001	1	+12
Vin < 0.03125	000	0	+18

Table 4. Interpreting the RSSI Bits

The digital processing chip which follows the AD6600 can combine the 11 bits of twos complement data, with the 3 RSSI bits to form a 16-bit equivalent output word. Table 5 explains how the RSSI data can be interpreted when using a PLD or ASIC. Basically, the circuit performs right shifts of the data depending on the RSSI word. This can also be performed in software using the following pseudo code fragment.

```
r0=dm(rssi);
r2=5;
r0=r2-r0;
r1=dm(adc);(11 bits, MSB justified into DSP word)
rshift r1, r0;(arithmetic shift to extend the sign bit)
```

The result of the shifted data is a 16 bit fixed-point word that can be used as any normal 16-bit word.

RSSI	11-Bit Word	16-bit Data Format	Corresponds to a shift right of
101	DATA	DATA x 32	5
100	DATA	DATA x 16	4
011	DATA	DATA x 8	3
010	DATA	DATA x 4	2
001	DATA	DATA x 2	1
000	DATA	DATA x 1	0

Table 5. 16-Bit, Fixed-Point Data Format

When mated with the AD6620, Digital Receive Processor chip, the AD6600 floating point data (mantissa + exponent) is automatically converted to 16-bit twos complement format by the AD6620.

APPLYING THE AD6600
Encoding the AD6600
The AD6600 encode signal must be a high quality, extremely low phase noise source to prevent degradation of performance. Digitizing high frequency signals (IF range 70-250MHz) places a premium on encode clock phase noise. SNR performance can easily degrade by 3-4dB with 70MHz input signals when using a questionable clock source. At higher IFs (up to 250MHz) and with questionable clock sources the higher slew rates of the input signals reduce performance even further. See AN501, "Aperture Uncertainty and ADC System Performance" for complete details.

For optimum performance the AD6600 must be clocked differentially. The encode signal is usually ac-coupled into the ENC and $\overline{\text{ENC}}$ pins via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 17 shows one preferred method for clocking the AD6600. The sine source (low jitter) is converted from single-ended to differential using a RF transformer. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD6600 to approximately 0.8Vp-p differential. This helps prevent the sharp edges of the clock from feeding to other portions of the AD6600, and limit the noise presented to the encode inputs. A crystal clock oscillator can also be used to drive the RF transformer if an appropriate limiting resistor (typically 100Ω) is placed in the series with the primary.

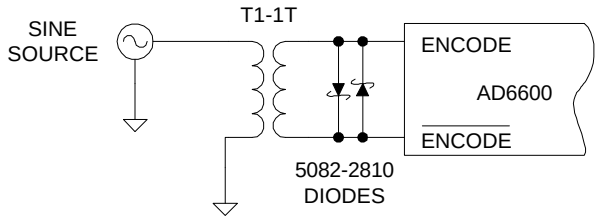


Figure 17. Transformer-Coupled Sine Source

If a low jitter ECL/PECL clock is available, another option is to ac-couple a differential ECL/PECL signal to the encode input pins as shown in Figure 18.

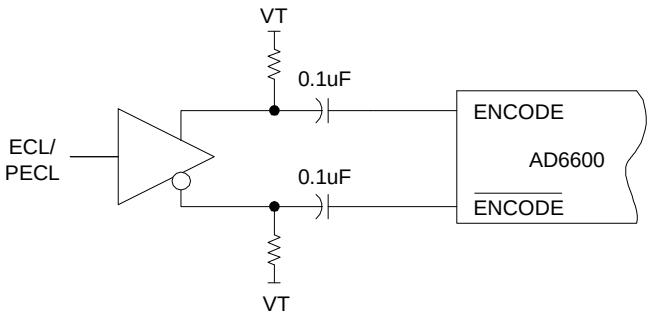


Figure 18. AC-Coupled ECL/PECL Encode

Driving the Analog Inputs

As with most new high-speed, high dynamic range analog-to-digital converters, the analog input to the AD6600 is differential. Differential inputs allow much improvement in performance on-chip as IF signals are processed through attenuation and gain stages. Most of the improvement is a result of differential analog stages having high rejection of even order harmonics. There are also benefits at the PCB level. First, differential inputs have high common mode rejection to stray signals such as ground and power noise. Also, they provide good rejection to common mode signals such as local oscillator feed-through.

Driving a differential analog input introduces some new challenges. Most RF/IF amplifiers are single-ended and may not obviously interface to the AD6600. However, using simple techniques, a clean interface is possible. The recommended method to drive the analog input port is shown below. The AD6600 input is actually designed to match easily to a SAW filter such as SAWTEK 855297. This allows the SAW filter to be used in a differential mode, which often improves the operations of a SAW filter. Using network analyzer data for both the SAW filter output and the AD6600 input ports (see data tables for AD6600 S11 data), a conjugate match can be used for maximum power transfer. Often an adequate match can be achieved simply by using a shunt inductor to make the port look real (Figure 19). For more details on how to exactly match networks, see RF Circuit Design by Chris Bowick, ISBN: 0-672-21868-2.

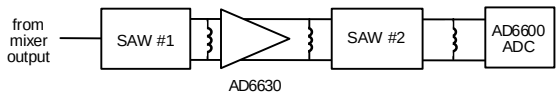


Figure 19. Cascaded SAW Filters with AD6630

Where gain is required, the AD6630 differential, low noise, IF gain block is recommended. This amplifier provides 24 dB of gain and provides limiting to prevent damage to the SAW filter and AD6600. The AD6630 is designed to reside between two SAW filters. This low noise device is ideally suited to many application of the AD6600. For more information on the AD6630, reference the AD6630 datasheet.

When general purpose gain blocks are used, matching can easily be achieved using a transformer. Most gain blocks are available with 50ohm input and output ports. Thus matching to the 200ohm impedance of the AD6600 requires only a 1:4(impedance ratio) transformer as shown in Figure 20.

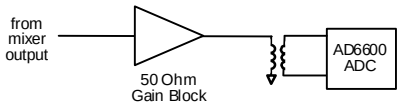


Figure 20. Transformer-Coupled Gain Block

In the rare case that better matching is required, a conjugate match between the amplifier selected and the transformer-coupled analog input can be achieved by placing the matching network between the amplifier and the transformer (Figure 21). For more details on matching, see the reference mentioned above for more details.

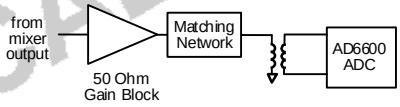


Figure 21. Gain Block and Matching Network

Understanding the External Analog Filter

Two primary tradeoffs must be made when designing the external resonant filter. The obvious one is the bandwidth of the filter. The second not so obvious tradeoff is settling time of the filter nodes.

Resonant Filter Bandwidth determines the amount of noise that is limited at the center frequency chosen. If the resonant filter is too wide, little noise improvement is seen. If the resonant filter is too narrow, amplitude variation can be seen due to the tolerance of filter components. If the narrow filter is off center due to these tolerances (or drift), the 4x/8x signal will fall on the transition band of the filter. An optimum starting point for this filter is approximately 50MHz.

Resonant Filter Settling limits the amount of capacitance of this filter. The output of the 4x/8x amplifier is clamped when the ADC is processing its input (encode high time). This prevents the amp output from feeding through to the ADC (T/H) and corrupting the ADC results. But, upon the falling edge of encode, the amp must now come out of clamp and present an accurate signal to the ADC T/H. The RC of the external filter determines the settling of the amp. If the amp output does not settle, the ADC sees an attenuated signal. So obviously a narrow bandwidth is desired to improve noise performance, but if the filter is too narrow, the amp will not settle and the ADC will see an attenuated signal.

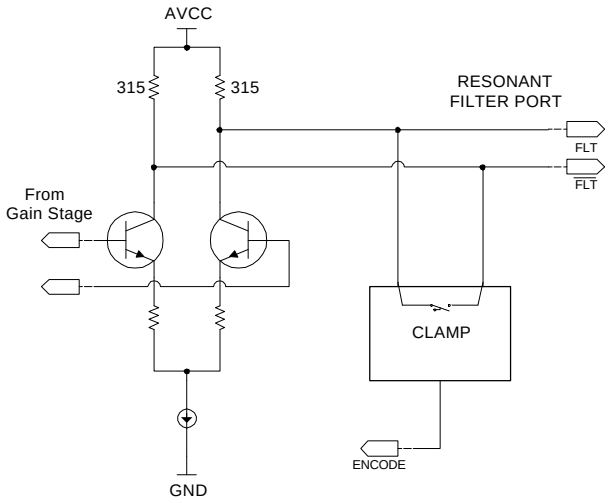


Figure 22. 4x/8x Amplifier Clamp Circuitry

Figure 22 shows a simplified model of the 4x/8x amplifier. A key point to note is the resistor values in the collector legs are 315 ohms nominal with tolerance of +/-20%. The filter performance is determined by these values in conjunction with the internal parasitic capacitance, board parasitics, and the external filter components.

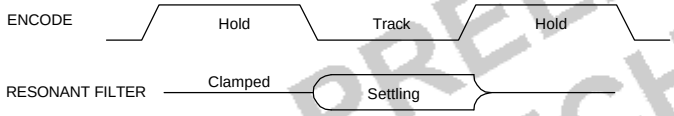


Figure 23. 4x/8x Amplifier Settling

Figure 23 shows why settling is important for this circuit. If the 4x/8x amp doesn't settle (come out of clamp) then the amplitude presented to the ADC will be decreased. This results in decreased gain when the filter capacitance is too high.

This explains why the total capacitance that is allowed for the external filter varies depending on the clock rate (actually encode clock high time). If the encode is 13MSPS and the duty cycle is 50% then the allowable settling time is 38.5ns (1/2 of the encode time). Our assumption is that the amp should be allowed to settle to ¼ lsb in this time period. This has been proven with both simulation and empirical analysis. If the settling is assumed to be an RC circuit, then:

T = RC; t = time; n = number of bits

$$Vo = A(1 - e^{t/T})$$

$$A - A/2^n = A(1 - e^{t/T})$$

$$1 - \frac{1}{2^n} = 1 - e^{t/T}$$

$$\frac{1}{2^n} = e^{t/T}$$

$$\frac{t}{T} = \ln\left(\frac{1}{2^n}\right)$$

$$T = \frac{t}{\ln(2^n)}$$

$$C_{total} = \frac{(T_{encode} * 0.5)}{R * \ln(8192)} = \frac{38.5ns}{315 * \ln(8192)} = 13.6\,pF$$

In this case, C_{total} includes all parasitics and external capacitance. R is nominally the 315 ohms. The 8192 is (4*2048), which is ¼ lsb of the converter (11 bits, 2048).

So for settling purposes, with 13MSPS encode and 50% duty cycle, the maximum allowable capacitance for proper settling is C_{total} = 13.6pF.

As stated above this C_{total} includes the external capacitors, the board parasitics, and the AD6600 parasitics. The parasitics of the AD6600 (lead, internal bond pad, and internal connections) at FLT and $\overline{FLT}$ are 1.75pF +/- 0.35pF (differential).

If the resistors are at maximum value (315 +20%), the maximum allowable capacitance is C_{total} = 11.3pF. If the duty cycle is less than 50% then the maximum allowable capacitance is decreased further, to allow for settling.

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended. Switching supplies tend to have radiated components that may be "received" by the AD6600. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1uF chip capacitors.

The AD6600 has separate digital and analog power supply pins. The analog supplies are denoted AVCC and the digital supply pins are denoted DVCC. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching back into the analog supplies. Note that AVCC must be held within 5% of 5 Volts; however the DVCC supply may be varied according to output digital logic family. The AD6600 is specified for DVCC = 3.3V as this is a common supply for digital ASICS.

Output Loading
Care must be taken when designing the data receivers for the AD6600. Note from the equivalent circuits shown earlier (ref. Equivalent Circuits) that D[10:0] and RSSI[2:0] contain a 500-ohm output series resistor. To minimize capacitive loading, there should only be one gate on each output pin. Extra capacitive loading will increase output timing and invalidate timing specifications. CLK2X and AB_OUT do not contain the output series resistors. Testing for digital output timing is performed with 10pF loads.

Layout Information
The schematic of the evaluation board (Figures 24, 25) represents a typical implementation of the AD6600. A multilayer board is recommended to achieve best results. It is highly recommended that high quality, ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. The pinout of the AD6600 facilitates ease of use in the implementation of high frequency, high resolution design practices. All of the digital outputs are segregated to two sides of the chip, with the inputs on the opposite side for isolation purposes.

Care should be taken when routing the digital output traces. To prevent coupling through the digital outputs into the analog portion of the AD6600, minimal capacitive loading should be placed on these outputs. It is recommended that a fan-out of only one be used for all AD6600 digital outputs.

The layout of the analog inputs and the external resonant filter are critical. No digital traces must be routed near, under, or above these portions of the circuit. The transformers used for coupling into the analog inputs must be located as close as possible to the analog inputs of the AD6600. The external resonant filter components must be physically close to the filter-input pins, yet separated from the analog inputs.

The layout of the Encode circuit is equally critical. Any noise received on this circuitry will result in corruption in the digitization process and lower overall performance. The Encode clock must be isolated from the digital outputs and the analog inputs.

Evaluation Board
The evaluation board for the AD6600 is straightforward, containing all required circuitry for evaluating the device. The only external connections required are power supplies, clock, and the analog inputs. The evaluation board includes the option for an onboard, clock oscillator for encode.

Power to the analog supply pins of the AD6600 is connected via the power terminal block (TB1). Power for the digital interface is supplied via pin 1 of J201, or the VDD e-hole located adjacent to J201. The VDD supply can vary between +3.3V to 5.0V and sets the level for the output digital data (J201). The J201 connector mates directly with the AD6620 (Receive Signal Processor) evaluation board, part# AD6620S/PCB, allowing complete evaluation of system performance.

The two analog inputs are connected via SMA connectors AIN and BIN, which are transformer-coupled to the AD6600 inputs. The transformers have a turns-ratio of 1:4 to match the input resistance of the AD6600 (200 ohms) to 50 ohms at the SMA connectors.

The Encode signal may be generated using an onboard crystal oscillator, U100. If an onboard crystal is used, R104 must be removed from the board to prevent loading of the oscillator's output. The on-board oscillator may be replaced by an external encode source via the SMA connector labeled ENCODE. If an external source is used, it must be a high quality and very low phase noise source. The high-IF range of the AD6600 (70-250MHz) demands that the Encode clock be sufficiently pure to maintain performance.

The AD6600 output data is latched using 74LCX574 (U201, U202) latches. The clock for these latches is determined by jumper selection on header J1. The clock can be a delayed version of the encode clock (CLKA, CLKB), or the CLK2X generated by the AD6600. A clock is also distributed with the output data (J201) that is labeled CLKX (pin 11, J201). The CLKX is selected with jumpers on header J1 and can be CLKA, CLKB, or CLK2X.

The resonant LC filter components (SEL2, C2 and C3) are omitted. The user must install proper values based on the IF chosen. See "Understanding the External Analog Filter" section of the data sheet for guidelines on selecting these components.

Item	Quantity	Reference	Description
1	3	AIN, BIN, ENCODE	SMA Connector
2	15	C1, C102-108, C111, C114, C117-118, C120-121, C299	0.1uF Chip Cap
3	4	C112-113, C115-116	Low Inductance 0.1uF Chip Cap
4	2	CR2-3	1N2810 Schottky Diode
5	1	DUT	AD6600AST
6	1	J1	20-Pin Double Row Male Header
7	1	J201	50-Pin Double Row Male Header, Right Angle
8	2	R1-2	Omitted
9	2	R100-101	Surface Mount Resistor 1206, 10kΩ
10	1	R103	Surface Mount Resistor 1206, 100Ω
11	1	R104	Surface Mount Resistor 1206, 50Ω
12	1	R298	Surface Mount Resistor 1206, 3.9kΩ
13	1	R299	Surface Mount Resistor 1206, 2kΩ
14	3	T1-2, T4	Surface Mount Transformer Mini-Circuits T4-1T

Table 6. AD6600ST/PCB Bill of Material

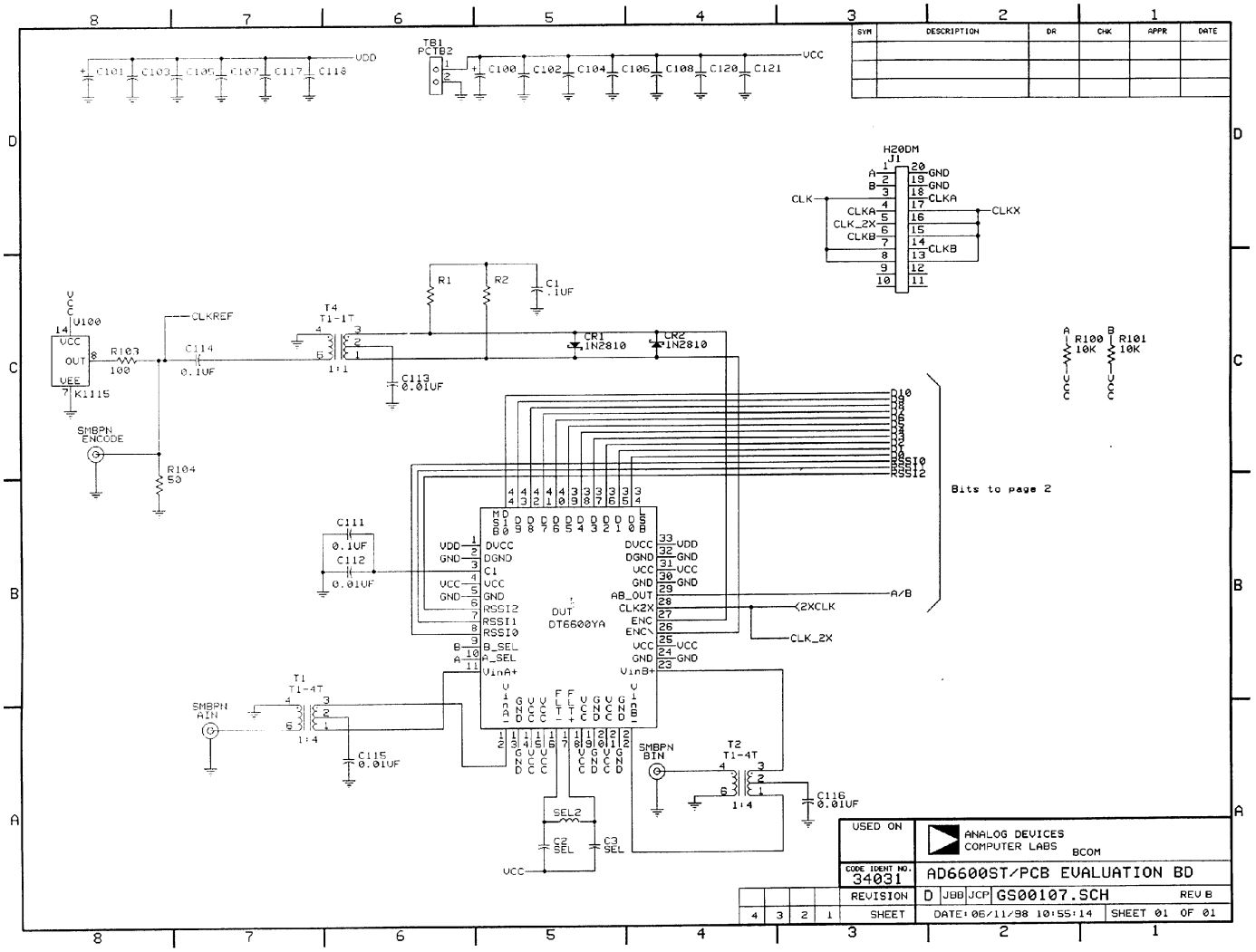


Figure 24. AD6600ST/PCB Schematic Diagram, Page 1

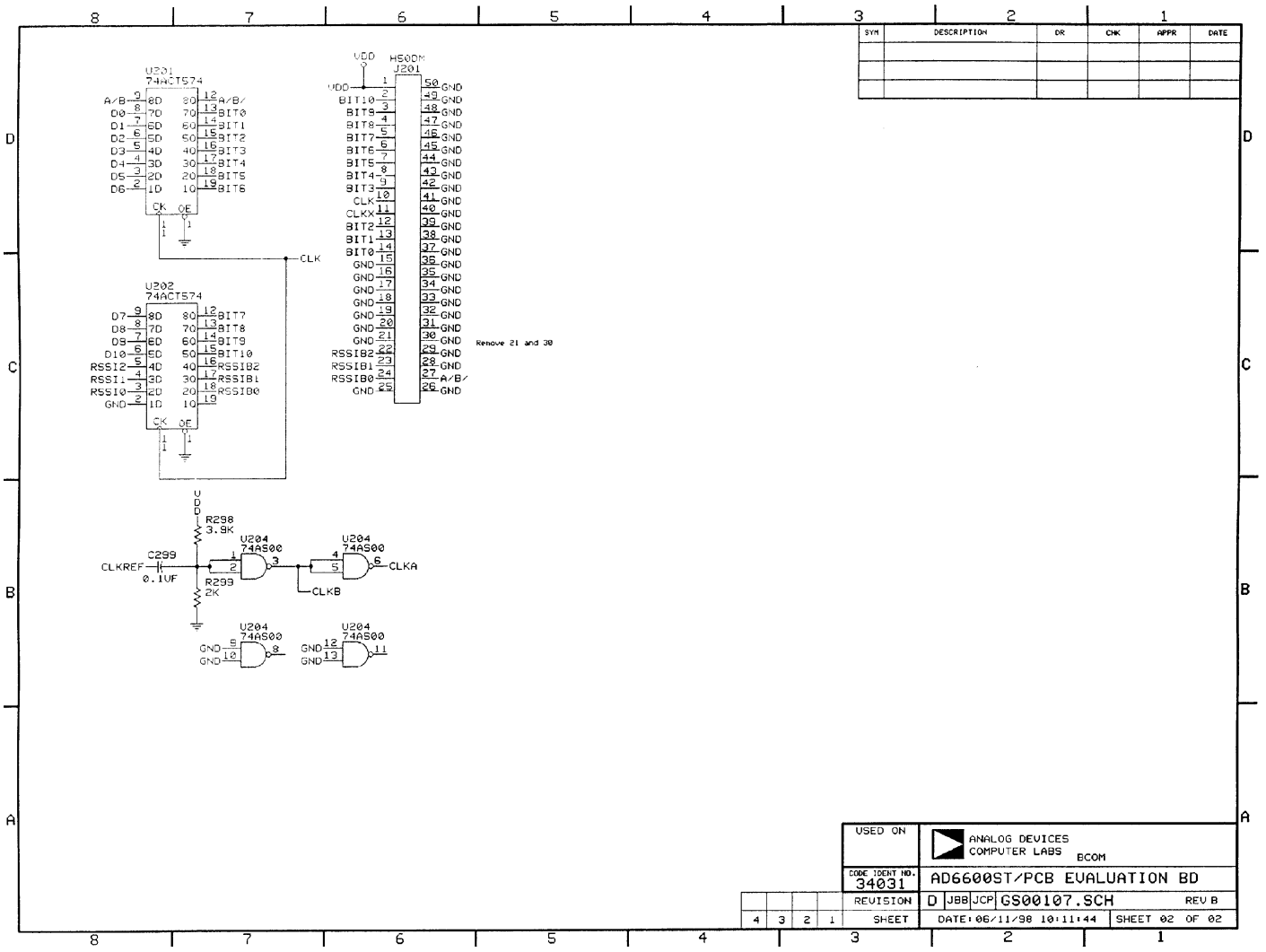


Figure 25. AD6600ST/PCB Schematic Diagram, Page 2

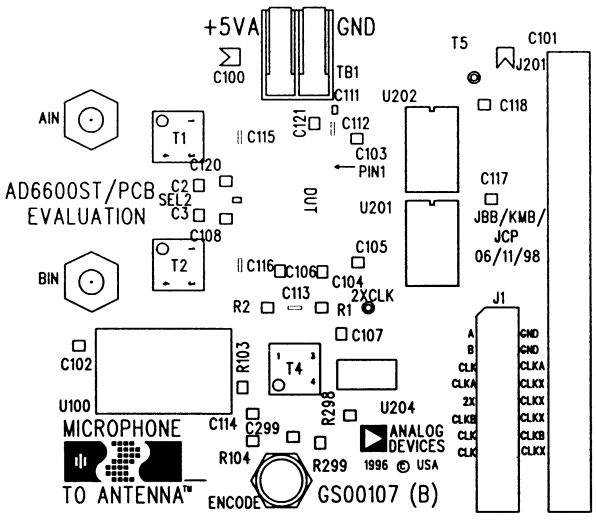


Figure 26. AD6600ST/PCB Top Side Silk Screen

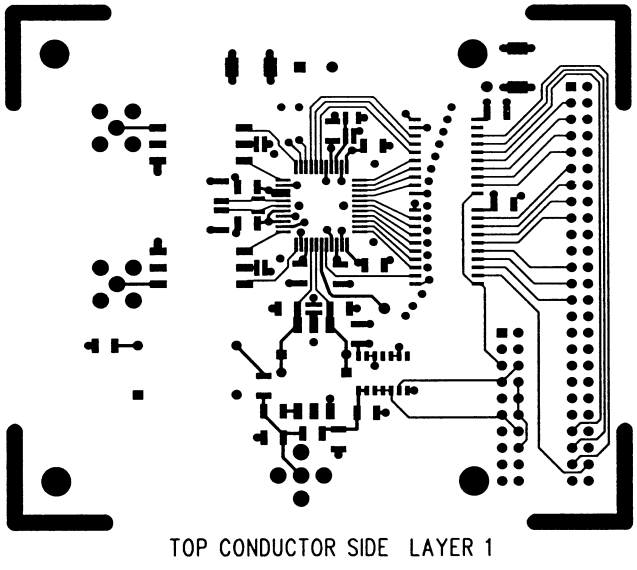


Figure 27. AD6600ST/PCB Top Side Copper

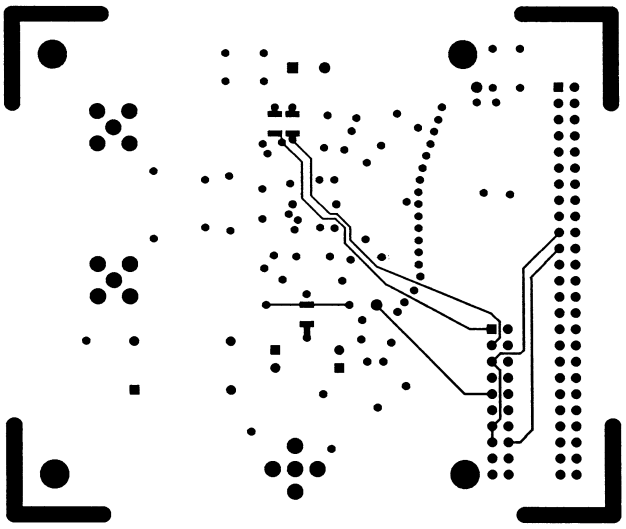


Figure 28. AD6600ST/PCB Bottom Side Copper

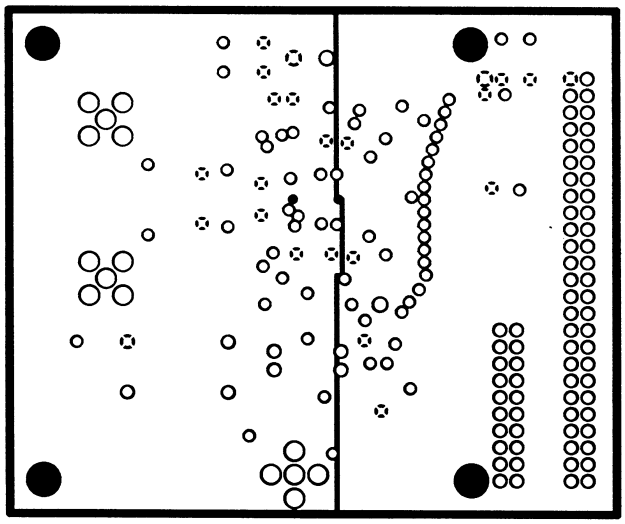


Figure 29. AD6600ST/PCB Power Supply Layer (Negative)

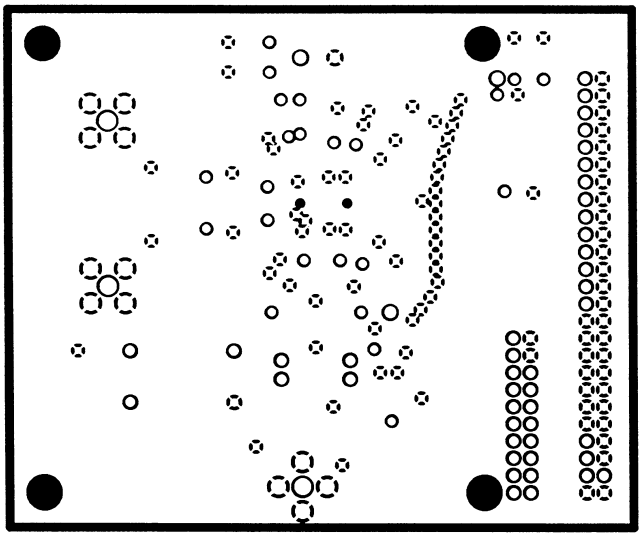


Figure 30. AD6600ST/PCB Ground Layer (Negative)

Connecting the AD6600 with the AD6620

The AD6600 interfaces directly to the AD6620 Digital Receive Signal Processor as shown in the Figure 31. No addition external components are required. Note that the layout requirements discussed previously do apply and deviations can result in degraded performance. The digital outputs of the AD6600 must connect directly to the AD6620 inputs with no additional fan-out. Additional loading on the outputs will compromise timing performance.

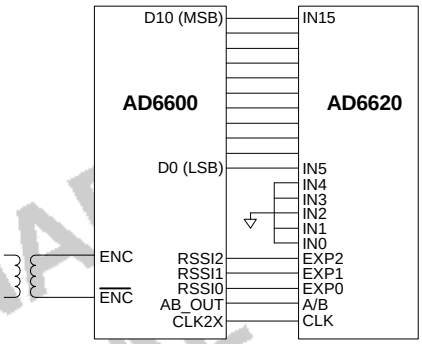


Figure 31. AD6600/AD6620 Connections

Figure 32 shows the timing details between the AD6600 and the AD6620. On Clock 1, D[10:0], RSSI[2:0], and AB_OUT are captured by the AD6620. Since AB_OUT has changed state from the previous clock, the D[10:0] and RSSI[2:0] are processed by the AD6620. This clock allows adequate setup and hold time for AB_OUT, D[10:0], and RSSI[2:0] to be captured by the AD6620.

On Clock2, D[10:0], RSSI[2:0], and AB_OUT are captured by the AD6620. Since AB_OUT has not changed from the previous clock, the D[10:0] and RSSI[2:0] are ignored by the AD6620. This clock is concerned only with the AB_OUT setup and hold time.

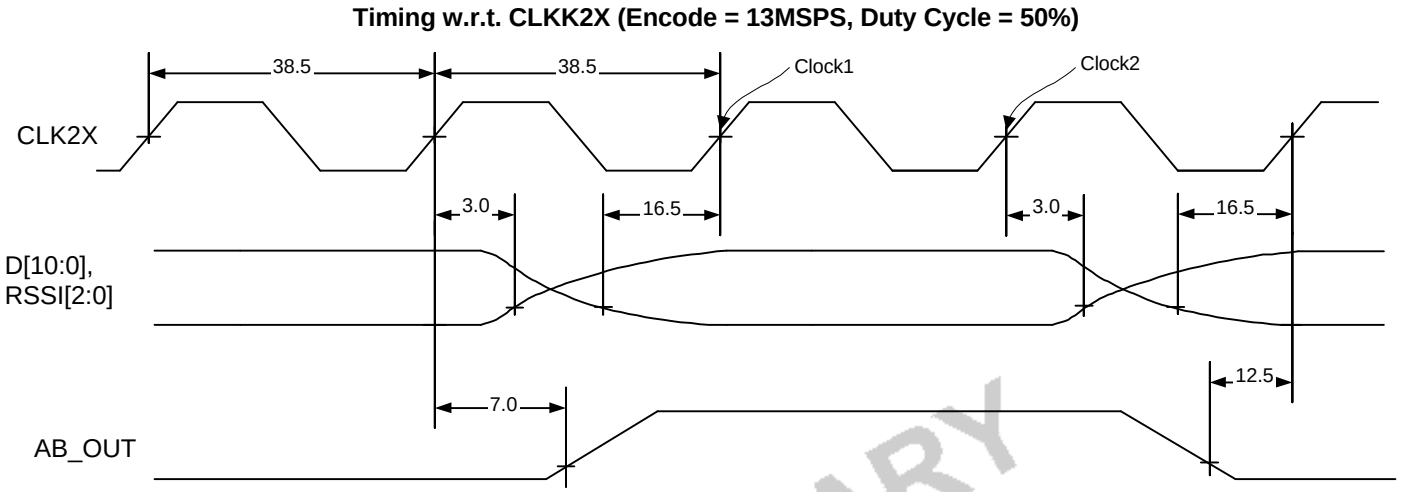


Figure 32. AD6600 to AD6620 Timing at 13MSPS

AD6600AST OUTLINE DIMENSIONS