



Low Cost, Low Power CMOS General Purpose Dual Analog Front End

Preliminary Technical Data

AD73322

FEATURES

- Two 16-Bit A/D Converters
- Two 16-Bit D/A Converters
- Programmable Input/Output Sample Rates
- 75 dB ADC SNR
- 70 dB DAC SNR
- 64 kS/s Maximum Sample Rate
- 90 dB Crosstalk
- Low Group Delay (25 μ s typ per ADC Channel, 50 μ s typ per DAC Channel)
- Programmable Input/Output Gain
- Flexible Serial Port which Allows up to 4 Dual Codecs to be Connected in Cascade giving 8 I/O channels
- Single (+2.7 V to +5.5 V) Supply Operation
- 80 mW Max Power Consumption at 2.7 V
- On-Chip Reference
- 28-Pin SOIC & 44-Pin LQFP Packages

APPLICATIONS

- General Purpose Analog I/O
- Speech Processing
- Cordless and Personal Communications
- Telephony
- Active Control of Sound & Vibration
- Data Communications

GENERAL DESCRIPTION

The AD73322 is a dual front-end processor for general purpose applications including speech and telephony. It features two 16-bit A/D conversion channels and two 16-bit D/A conversion channels. Each channel provides 70 dB signal-to-noise ratio over a voiceband signal bandwidth. It also features an input to

output gain network in both the analog and digital domains. This is featured on both codecs and can be used for impedance matching or scaling when interfacing to Subscriber Line Interface Circuits (SLICs)

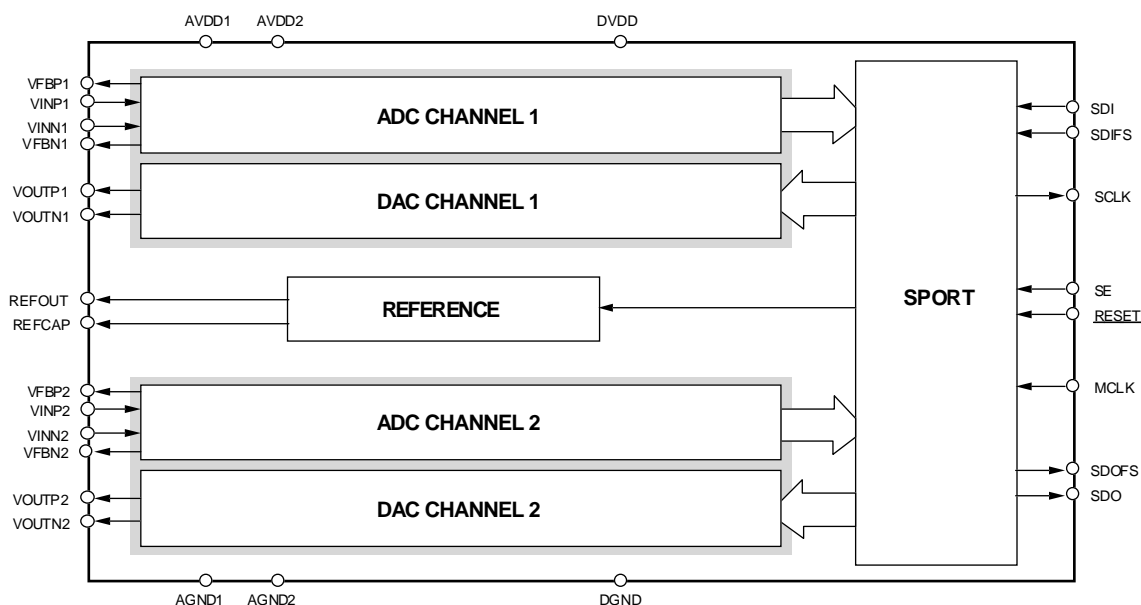
The AD73322 is particularly suitable for a variety of applications in the speech and telephony area including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multichannel active control applications.

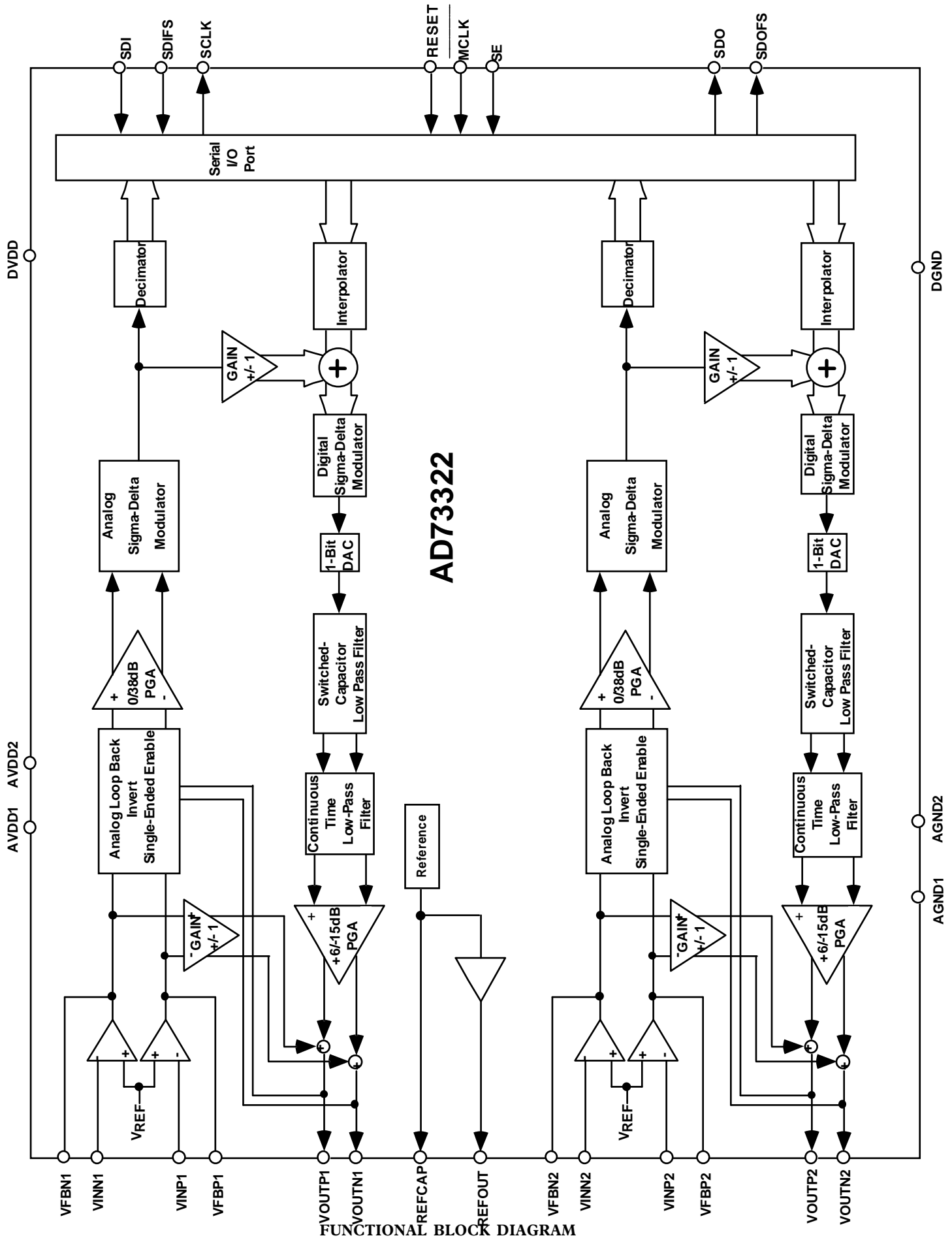
The A/D and D/A conversion channels feature programmable input/output gains with ranges 38 dB and 21 dB respectively. An on-chip reference voltage is included to allow single supply operation. This reference is programmable to accommodate either 3V or 5V operation.

The sampling rate of the codecs is programmable with four separate settings offering 64, 32, 16 and 8 kHz sampling rates (from a master clock of 16.384 MHz).

A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines. The SPORT transfer rate is programmable to allow interfacing to both fast and slow DSP engines.

The AD73322 is available in 28-pin SOIC and 44-pin LQFP packages.





AD73322—SPECIFICATIONS¹

(AVDD = +3 V ± 10%; DVDD = +3 V ± 10%; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, f_S = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

| Parameter | AD73322A | | | Units | Test Conditions/Comments |
|---|----------|-------------------------|----------------|----------------------|---|
| | Min | Typ | Max | | |
| REFERENCE | | | | | 5VEN = 0 |
| REFCAP | | | | | |
| Absolute Voltage, V _{REFCAP} | 1.08 | 1.2 | 1.32 | V | |
| REFCAP TC | | 50 | | ppm/°C | 0.1 μF Capacitor Required from REFCAP to AGND2 |
| REFOUT | | | | | |
| Typical Output Impedance | | 68 | | Ω | |
| Absolute Voltage, V _{REFOUT} | 1.08 | 1.2 | 1.32 | V | Unloaded |
| Minimum Load Resistance | 1 | | | kΩ | |
| Maximum Load Capacitance | | | 100 | pF | |
| INPUT AMPLIFIER | | | | | |
| Offset | | | TBD | mV | |
| Maximum Output swing | | | TBD | V | |
| Feedback Resistance | | | TBD | Ω | |
| Feedback Capacitance | | | TBD | pF | |
| ANALOG GAIN TAP | | | | | |
| Tap Gain | -1 | | +1 | V/V | |
| Gain Resolution | | 5 | | Bits | Step Size = |
| Output Offset | TBD | | TBD | mV | |
| Gain Accuracy | | | | % | |
| Settling Time | | | | μs | Tap Gain Change of -FS to +FS |
| Delay | | | | μs | |
| ADC SPECIFICATIONS | | | | | |
| Maximum Input Range at VIN ^{2,3} | | | 1.578 -2.85 | V p-p dBm | 5VEN = 0, Measured Differentially |
| Nominal Reference Level at VIN (0 dBm0) | | 1.0954 -6.02 | | V p-p dBm | 5VEN = 0, Measured Differentially |
| Absolute Gain | | | | | |
| PGA = 0 dB | -0.75 | 0.1 | +1.0 | dB | 1.0 kHz, 0 dBm0 |
| PGA = 38 dB | -1.5 | -0.5 | +0.5 | dB | 1.0 kHz, 0 dBm0 |
| Gain Tracking Error | | ±0.1 | | dB | 1.0 kHz, +3 dBm0 to -50 dBm0 |
| Signal to (Noise + Distortion) PGA = 0 dB | 70 | 76 | | dB | 0 Hz to Fs/2; Fs = 8 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 16 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 32 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 64 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 8 kHz |
| PGA = 38 dB | 61 | 65 | | dB | |
| Total Harmonic Distortion | | | | | |
| PGA = 0 dB | | -83 | -70 | dB | |
| PGA = 38 dB | | -83 | -70 | dB | |
| Intermodulation Distortion | | -78 | | dB | PGA = 0 dB |
| Idle Channel Noise | | -76 | | dBm0 | PGA = 0 dB |
| Crosstalk ADC-to-DAC | | -100 | | dB | ADC Input Signal Level: 1.0 kHz, 0 dBm0 DAC Input at Idle |
| ADC-to-ADC | | | | dB | ADC1 Input Signal Level: 1.0 kHz, 0 dBm0 ADC2 Input at Idle |
| DC Offset | -20 | +15 | +50 | mV | PGA = 0 dB |
| Power Supply Rejection | | -55 | | dB | Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine Wave |
| Group Delay ^{4,5} | | 25 TBD TBD TBD | | μs μs μs μs | 64 kHz Output Sample Rate 32 kHz Output Sample Rate 16 kHz Output Sample Rate 8 kHz Output Sample Rate |
| Input Resistance at VIN ^{2,4} | | 25 | | kΩ ⁶ | DMCLK = 16.384 MHz |
| DIGITAL GAIN TAP | | | | | |
| Tap Gain | -1 | | +1 | V/V | |
| Gain Resolution | | 5 | | Bits | Step Size = |
| Delay | TBD | | TBD | μs | |
| Settling Time | | | TBD | μs | Tap Gain Change from -FS to +FS |

Preliminary Technical Data

AD73322

| Parameter | AD73322A | | | Units | Test Conditions/Comments |
|---|----------|---------|-------|-------|---|
| | Min | Typ | Max | | |
| DAC SPECIFICATIONS | | | | | |
| Maximum Voltage Output Swing ² | | | | | |
| Single Ended | | | 1.578 | V p-p | 5VEN = 0, PGA = 6 dB |
| Differential | | | -2.85 | dBm | |
| | | | 3.156 | V p-p | 5VEN = 0, PGA = 6 dB |
| | | | 3.17 | dBm | |
| Nominal Voltage Output Swing (0 dBm0) | | | | | |
| Single-Ended | | 1.0954 | | V p-p | 5VEN = 0, PGA = 6 dB |
| | | -6.02 | | dBm | |
| Differential | | 2.1909 | | V p-p | 5VEN = 0, PGA = 6 dB |
| | | 0 | | dBm | |
| Output Bias Voltage | 1.08 | 1.2 | 1.32 | V | 5VEN = 0, REFOUT Unloaded |
| Absolute Gain | -0.75 | +0.2 | +1.0 | dB | 1.0 kHz, 0 dBm0 |
| Gain Tracking Error | | ± 0.1 | | dB | 1.0 kHz, +3 dBm0 to -50 dBm0 |
| Signal to (Noise + Distortion) | | | | | Refer to Figure 5 |
| PGA = 0 dB | 62.5 | 70 | | dB | 300 Hz to 3.4 kHz Frequency Range |
| | | 62.5 | | dB | 0 Hz to 32 kHz Frequency Range |
| PGA = 6 dB | 62.5 | 71 | | dB | 300 Hz to 3.4 kHz Frequency Range |
| | | 62.5 | | dB | 0 Hz to 32 kHz Frequency Range |
| Total Harmonic Distortion | | | | | |
| PGA = 0 dB | | -70 | -62.5 | dB | |
| PGA = 6 dB | | -70 | -62.5 | dB | |
| Intermodulation Distortion | | | | dB | PGA = 0 dB |
| Idle Channel Noise | | | | dBm0 | PGA = 0 dB |
| Crosstalk DAC-to-ADC | | | -100 | dB | ADC Input Signal Level: AGND; DAC Output Signal Level: 1.0 kHz, 0 dBm0 |
| DAC-to-DAC | | | -100 | dB | DAC1 Output Signal Level: AGND; DAC2 Output Signal Level: 1.0 kHz, 0 dBm0 |
| Power Supply Rejection | | | -55 | dB | Input Signal Level at AVDD and DVDD |
| Group Delay ^{4,5} | | 25 | | µs | Pins: 1.0 kHz, 100 mV p-p Sine Wave |
| | | 50 | | µs | 64 kHz Sample Rate (Interpolator Bypassed) |
| | | TBD | | µs | 64 kHz Sample Rate |
| | | TBD | | µs | 32 kHz Input Sample Rate |
| | | TBD | | µs | 16 kHz Input Sample Rate |
| | | TBD | | µs | 8 kHz Input Sample Rate |
| Output DC Offset ^{2,7} | -30 | +20 | +70 | mV | PGA = 6 dB |
| Minimum Load Resistance, R _L ^{2,8} | | | | | |
| Single-Ended | 150 | | | Ω | |
| Differential | 150 | | | Ω | |
| Maximum Load Capacitance, C _L ^{2,8} | | | | | |
| Single-Ended | | | 500 | pF | |
| Differential | | | 100 | pF | |
| FREQUENCY RESPONSE | | | | | |
| (ADC AND DAC) ⁹ Typical Output Frequency (Normalised to F _S) | | | | | |
| 0 | | 0 | | dB | |
| 0.03125 | | -0.1 | | dB | |
| 0.0625 | | -0.25 | | dB | |
| 0.125 | | -0.6 | | dB | |
| 0.1875 | | -1.4 | | dB | |
| 0.25 | | -2.8 | | dB | |
| 0.3125 | | -4.5 | | dB | |
| 0.375 | | -7.0 | | dB | |
| 0.4375 | | -9.5 | | dB | |
| > 0.5 | | < -12.5 | | dB | |

| Parameter | AD73322A | | | Units | Test Conditions/Comments |
|---------------------------------------|-----------------------|-----|-----------------|-------|--------------------------|
| | Min | Typ | Max | | |
| LOGIC INPUTS | | | | | |
| V _{INH} , Input High Voltage | V _{DD} - 0.8 | | V _{DD} | V | |
| V _{INL} , Input Low Voltage | 0 | | 0.8 | V | |
| I _{IH} , Input Current | | | 10 | μA | |
| C _{IN} , Input Capacitance | | | 10 | pF | |
| LOGIC OUTPUT | | | | | |
| V _{OH} , Output High Voltage | V _{DD} - 0.4 | | V _{DD} | V | IOUT - 100 μA |
| V _{OL} , Output Low Voltage | 0 | | 0.4 | V | IOUT - 100 μA |
| Three-State Leakage Current | -10 | | +10 | μA | |
| POWER SUPPLIES | | | | | |
| AVDD1, AVDD2 | 2.7 | | 3.3 | V | |
| DVDD | 2.7 | | 3.3 | V | |
| I _{DD} ¹⁰ | | | | | See Table I |

NOTES

¹ Operating temperature range is as follows: -40°C to +85°C. Therefore, T_{MIN} = -40°C and T_{MAX} = +85°C.

² Test conditions: Input PGA set for 0 dB gain, Output PGA set for 6 dB gain, no load on analog outputs (unless otherwise noted).

³ At input to sigma-delta modulator of ADC.

⁴ Guaranteed by design.

⁵ Overall group delay will be affected by the sample rate and the external digital filtering.

⁶ The ADC's input impedance is inversely proportional to DMCLK and is approximated by: (4 * 10¹¹)/DMCLK.

⁷ Between VOUTP1 and VOUTN1 or between VOUTP2 and VOUTN2.

⁸ At VOUT output.

⁹ Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of -10 dBm₀), with 38 dB preamplifier bypassed and input gain of 0 dB.

¹⁰ Test Conditions: no load on digital inputs, analog inputs ac coupled to ground, no load on analog outputs.

Specifications subject to change without notice.

Table I. Current Summary (AVDD = DVDD = +3.3 V)

| Conditions | Analog Current | Internal Digital Current | External Interface Current | Total Current (Max) | SE | MCLK ON | Comments |
|---------------------------------|----------------|--------------------------|----------------------------|---------------------|----|---------|--|
| ADCs On Only | 7 | 3 | 0.5 | 23 | 1 | YES | REFOUT Disabled |
| ADCs and DACs On | 10 | 5 | 0.5 | 35 | 1 | YES | REFOUT Disabled |
| ADCs and DACs and Input Amps On | 10 | 5 | 0.5 | TBD | 1 | YES | REFOUT Disabled |
| ADCs and DACs and AGT On | 10 | 5 | 0.5 | TBD | 1 | YES | REFOUT Disabled |
| All Sections On | | | | TBD | 1 | YES | |
| REFCAP On Only | 0.75 | 0 | 0 | 1.0 | 0 | NO | REFOUT Disabled |
| REFCAP and REFOUT On Only | 3.0 | 0 | 0 | 4.5 | 0 | NO | |
| All Sections Off | 0 | 0.85 | 0 | 1.0 | 0 | YES | MCLK Active Levels Equal to 0 V and DVDD |
| All Sections Off | 0.00 | 0.007 | 0 | 0.04 | 0 | NO | Digital Inputs Static and Equal to 0 V or DVDD |

The above values are in mA and are typical values unless otherwise noted.

AD73322—SPECIFICATIONS¹ (AVDD = +5 V ± 10%; DVDD = +5 V ± 10%; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, F_S = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

| Parameter | AD73322A | | | Units | Test Conditions/Comments |
|--|----------|--------|-----|-----------------|---|
| | Min | Typ | Max | | |
| REFERENCE | | | | | |
| REFCAP | | | | | |
| Absolute Voltage, V _{REFCAP} | | 1.2 | | V | 5VEN = 0 |
| REFCAP TC | | 2.4 | | V | 5VEN = 1 |
| REFOUT | | 50 | | ppm/°C | 0.1 μF Capacitor Required from REFCAP to AGND2 |
| Typical Output Impedance | | 68 | | Ω | |
| Absolute Voltage, V _{REFOUT} | | 1.2 | | V | 5VEN = 0, Unloaded |
| Minimum Load Resistance | 2 | 2.4 | | V | 5VEN = 1, Unloaded |
| Maximum Load Capacitance | | | 100 | kΩ | 5VEN = 1 |
| | | | | pF | |
| INPUT AMPLIFIER | | | | | |
| Offset | | | TBD | mV | |
| Maximum Output swing | | | TBD | V | |
| Feedback Resistance | | | TBD | Ω | |
| Feedback Capacitance | | | TBD | pF | |
| ANALOG GAIN TAP | | | | | |
| Tap Gain | -1 | | +1 | V/V | |
| Gain Resolution | | 5 | | Bits | Step Size = |
| Output Offset | TBD | | TBD | mV | |
| Gain Accuracy | | | | % | |
| Settling Time | | | | μs | Tap Gain Change of -FS to +FS |
| Delay | | | | μs | |
| ADC SPECIFICATIONS | | | | | |
| Maximum Input Range at VIN ^{2, 3} | | 3.156 | | V p-p | 5VEN = 1, Measured Differentially |
| | | 3.17 | | dBm | |
| Nominal Reference Level at VIN (0 dBm0) | | 2.1908 | | V p-p | 5VEN = 1, Measured Differentially |
| | | 0 | | dBm | |
| Absolute Gain | | | | | |
| PGA = 0 dB | | 0.1 | | dB | 1.0 kHz, 0 dBm0 |
| PGA = 38 dB | | -0.5 | | dB | 1.0 kHz, 0 dBm0 |
| Gain Tracking Error | | ±0.1 | | dB | 1.0 kHz, +3 dBm0 to -50 dBm0 |
| Signal to (Noise + Distortion) PGA = 0 dB | 70 | 76 | | dB | 0 Hz to Fs/2; Fs = 8 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 16 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 32 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 64 kHz |
| | | | | dB | 0 Hz to Fs/2; Fs = 8 kHz |
| PGA = 38 dB | 61 | 65 | | dB | |
| Total Harmonic Distortion | | | | | |
| PGA = 0 dB | | -76 | | dB | |
| PGA = 38 dB | | -69 | | dB | |
| Intermodulation Distortion | | -69 | | dB | PGA = 0 dB |
| Idle Channel Noise | | -67 | | dBm0 | PGA = 0 dB |
| Crosstalk ADC-to-DAC | | -100 | | dB | ADC Input Signal Level: 1.0 kHz, 0 dBm0 DAC Input at Idle |
| ADC-to-ADC | | | | dB | ADC1 Input Signal Level: 1.0 kHz, 0 dBm0 ADC2 Input at Idle |
| DC Offset | | +20 | | mV | PGA = 0 dB |
| Power Supply Rejection | | -55 | | dB | Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine Wave |
| Group Delay ^{4, 5} | | 25 | | μs | 64 kHz Output Sample Rate |
| | | TBD | | μs | 32 kHz Output Sample Rate |
| | | TBD | | μs | 16 kHz Output Sample Rate |
| | | TBD | | μs | 8 kHz Output Sample Rate |
| Input Resistance at VIN ^{2, 4} | | 25 | | kΩ ⁶ | DMCLK = 16.384 MHz |
| DIGITAL GAIN TAP | | | | | |
| Tap Gain | -1 | | +1 | V/V | |
| Gain Resolution | | 5 | | Bits | Step Size = |
| Delay | TBD | | TBD | μs | |
| Settling Time | | | TBD | μs | Tap Gain Change from -FS to +FS |

Preliminary Technical Data

AD73322

| Parameter | AD73322A | | | Units | Test Conditions/Comments |
|--|----------|---------------------|-----|-------|--|
| | Min | Typ | Max | | |
| DAC SPECIFICATIONS | | | | | |
| Maximum Voltage Output Swing ² Single Ended | | 3.156 | | V p-p | 5VEN = 1, PGA = 6 dB |
| | | 3.17 | | dBm | |
| Differential | | 6.312 | | V p-p | 5VEN = 1, PGA = 6 dB |
| | | 9.19 | | dBm | |
| Nominal Voltage Output Swing (0 dBm0) Single-Ended | | 2.1908 | | V p-p | 5VEN = 1, PGA = 6 dB |
| | | 0 | | dBm | |
| Differential | | 4.3918 | | V p-p | 5VEN = 1, PGA = 6 dB |
| | | 6.02 | | dBm | |
| Output Bias Voltage | | V _{REFOUT} | | V typ | 5VEN = 1, REFOUT Unloaded |
| Absolute Gain | | ±0.4 | | dB | 1.0 kHz, 0 dBm0 |
| Gain Tracking Error | | ±0.1 | | dB | 1.0 kHz, +3 dBm0 to -50 dBm0 |
| Signal to (Noise + Distortion) PGA = 0 dB | | 66 | | dB | Refer to Figure 5 300 Hz to 3.4 kHz Frequency Range |
| | | 64 | | dB | 0 Hz to 32 kHz Frequency Range |
| PGA = 6 dB | | 66 | | dB | 300 Hz to 3.4 kHz Frequency Range |
| | | 64 | | dB | 0 Hz to 32 kHz Frequency Range |
| Total Harmonic Distortion PGA = 0 dB | | -62.5 | | dB | |
| PGA = 6 dB | | -62.5 | | dB | |
| Intermodulation Distortion | | -60 | | dB | PGA = 0 |
| Idle Channel Noise | | -75 | | dBm0 | PGA = 0 |
| Crosstalk DAC-to-ADC | | -100 | | dB | ADC Input Signal Level: AGND; DAC Output Signal Level: 1.0 kHz, 0 dBm0 |
| | | | | | DAC1 Output Signal Level: AGND; DAC2 Output Signal Level: 1.0 kHz, 0 dBm0 |
| DAC-to-DAC | | -100 | | dB | Input Signal Level at AVDD and DVDD Pins: 1.0 kHz, 100 mV p-p Sine Wave |
| Power Supply Rejection | | -55 | | dB | 64 kHz Input Sample Rate, Interpolator Bypassed (CRE:5 = 1) |
| Group Delay ^{4,5} | | 25 | | µs | PGA = 6 dB |
| Output DC Offset ^{2,7} | | +30 | | mV | |
| Minimum Load Resistance, R _L ^{2,8} Single-Ended | 150 | | | Ω | |
| Differential | 150 | | | Ω | |
| Maximum Load Capacitance, C _L ^{2,8} Single-Ended | | | 500 | pF | |
| Differential | | | 100 | pF | |
| FREQUENCY RESPONSE | | | | | |
| (ADC AND DAC) ⁹ Typical Output Frequency (Normalised to F _S) | | | | | |
| 0 | | 0 | | dB | |
| 0.03125 | | -0.1 | | dB | |
| 0.0625 | | -0.25 | | dB | |
| 0.125 | | -0.6 | | dB | |
| 0.1875 | | -1.4 | | dB | |
| 0.25 | | -2.8 | | dB | |
| 0.3125 | | -4.5 | | dB | |
| 0.375 | | -7.0 | | dB | |
| 0.4375 | | -9.5 | | dB | |
| > 0.5 | | < -12.5 | | dB | |

LOGIC INPUTS

| | | | |
|--------------------------------|----------------|----------|---------------|
| V_{INH} , Input High Voltage | $V_{DD} - 0.8$ | V_{DD} | V |
| V_{INL} , Input Low Voltage | 0 | 0.8 | V |
| I_{IH} , Input Current | -0.5 | | μA |
| C_{IN} , Input Capacitance | 10 | | pF |

LOGIC OUTPUT

| | | | | |
|--------------------------------|----------------|----------|---------------|----------------------------------|
| V_{OH} , Output High Voltage | $V_{DD} - 0.4$ | V_{DD} | V | $ I_{OUT} \leq 100 \mu\text{A}$ |
| V_{OL} , Output Low Voltage | 0 | 0.4 | V | $ I_{OUT} \leq 100 \mu\text{A}$ |
| Three-State Leakage Current | -0.3 | | μA | |

POWER SUPPLIES

| | | | | |
|---------------|-----|-----|---|--------------|
| AVDD1, AVDD2 | 4.5 | 5.5 | V | See Table II |
| DVDD | 4.5 | 5.5 | V | |
| I_{DD}^{10} | | | | |

NOTES

- ¹Operating temperature range is as follows: -40°C to $+85^{\circ}\text{C}$. Therefore, $T_{MIN} = -40^{\circ}\text{C}$ and $T_{MAX} = +85^{\circ}\text{C}$.
 - ²Test conditions: Input PGA set for 0 dB gain, Output PGA set for 6 dB gain, no load on analog outputs (unless otherwise stated).
 - ³At input to sigma-delta modulator of ADC.
 - ⁴Guaranteed by design.
 - ⁵Overall group delay will be affected by the sample rate and the external digital filtering.
 - ⁶The ADC's input impedance is inversely proportional to DMCLK and is approximated by: $(4 \times 10^{11})/\text{DMCLK}$.
 - ⁷Between VOUTP and VOUTN.
 - ⁸At VOUT output.
 - ⁹Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of -10 dBm_0), with 38 dB preamplifier bypassed and input gain of 0 dB.
 - ¹⁰Test conditions: no load on digital inputs, analog inputs ac coupled to ground, no load on analog outputs.
- Specifications subject to change without notice.

Table II. Current Summary (AVDD = DVDD = +5.5 V)

| Conditions | Analog Current | Internal Digital Current | External Interface Current | Total Current | SE | MCLK ON | Comments |
|---------------------------------|----------------|--------------------------|----------------------------|---------------|----|---------|--|
| ADC On Only | 8.5 | 6 | 2 | 33.0 | 1 | YES | REFOUT Disabled |
| ADC and DAC On | 14.5 | 6 | 2 | 45.0 | 1 | YES | REFOUT Disabled |
| ADCs and DACs and Input Amps On | 10 | 5 | 0.5 | TBD | 1 | YES | REFOUT Disabled |
| ADCs and DACs and AGT On | 10 | 5 | 0.5 | TBD | 1 | YES | REFOUT Disabled |
| All Sections On | | | | TBD | 1 | YES | |
| REFCAP On Only | 0.8 | 0 | 0 | 0.8 | 0 | NO | REFOUT Disabled |
| REFCAP and REFOUT On Only | 3.5 | 0 | 0 | 3.5 | 0 | NO | |
| All Sections Off | 0 | 1.5 | 0 | 1.5 | 0 | YES | MCLK Active Levels Equal to 0 V and DVDD |
| All Sections Off | 0 | 0.01 | 0 | 0.01 | 0 | NO | Digital Inputs Static and Equal to 0 V or DVDD |

The above values are in mA and are typical values unless otherwise noted.

Table III. Signal Ranges

| | | 3 V Power Supply 5VEN = 0 | 5 V Power Supply 5VEN = 0 5VEN = 1 | |
|--------------|---|--|--|--|
| V_{REFCAP} | | 1.2 V \pm 10% | 1.2 V | 2.4 V |
| V_{REFOUT} | | 1.2 V \pm 10% | 1.2 V | 2.4 V |
| ADC | Maximum Input Range at V_{IN} Nominal Reference Level | 1.578 V p-p 1.0954 V p-p | 1.578 V p-p 1.0954 V p-p | 3.156 V p-p 2.1908 V p-p |
| DAC | Maximum Voltage Output Swing Single-Ended Differential Nominal Voltage Output Swing Single-Ended Differential Output Bias Voltage | 1.578 V p-p 3.156 V p-p 1.0954 V p-p 2.1909 V p-p V_{REFOUT} | 1.578 V p-p 3.156 V p-p 1.0954 V p-p 2.1909 V p-p V_{REFOUT} | 3.156 V p-p 6.312 V p-p 2.1908 V p-p 4.3818 V p-p V_{REFOUT} |

TIMING CHARACTERISTICS (AVDD = +3 V \pm 10%; DVDD = +3 V \pm 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted)

| Parameter | Limit at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | Units | Description |
|---------------|--|--------|---------------------------------|
| Clock Signals | | | See Figure 1 |
| t_1 | 61 | ns min | MCLK Period |
| t_2 | 24.4 | ns min | MCLK Width High |
| t_3 | 24.4 | ns min | MCLK Width Low |
| Serial Port | | | See Figures 3 and 4 |
| t_4 | t_1 | ns min | SCLK Period |
| t_5 | $0.4 * t_1$ | ns min | SCLK Width High |
| t_6 | $0.4 * t_1$ | ns min | SCLK Width Low |
| t_7 | 20 | ns min | SDI/SDIFS Setup Before SCLK Low |
| t_8 | 0 | ns min | SDI/SDIFS Hold After SCLK Low |
| t_9 | 10 | ns max | SDOFS Delay From SCLK High |
| t_{10} | 10 | ns min | SDOFS Hold After SCLK High |
| t_{11} | 10 | ns min | SDO Hold After SCLK High |
| t_{12} | 10 | ns max | SDO Delay From SCLK High |
| t_{13} | 30 | ns max | SCLK Delay from MCLK |

TIMING CHARACTERISTICS (AVDD = +5 V ± 10%; DVDD = +5 V ± 10%; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

| Parameter | Limit at T _A = -40°C to +85°C | Units | Description |
|-----------------|---|--------|---------------------------------|
| Clock Signals | | | See Figure 1 |
| t ₁ | 61 | ns min | MCLK Period |
| t ₂ | 24.4 | ns min | MCLK Width High |
| t ₃ | 24.4 | ns min | MCLK Width Low |
| Serial Port | | | See Figures 3 and 4 |
| t ₄ | t ₁ | ns min | SCLK Period |
| t ₅ | 0.4 * t ₁ | ns min | SCLK Width High |
| t ₆ | 0.4 * t ₁ | ns min | SCLK Width Low |
| t ₇ | 20 | ns typ | SDI/SDIFS Setup Before SCLK Low |
| t ₈ | 0 | ns typ | SDI/SDIFS Hold After SCLK Low |
| t ₉ | 10 | ns typ | SDOFS Delay From SCLK High |
| t ₁₀ | 10 | ns typ | SDOFS Hold After SCLK High |
| t ₁₁ | 10 | ns typ | SDO Hold After SCLK High |
| t ₁₂ | 10 | ns typ | SDO Delay From SCLK High |
| t ₁₃ | 30 | ns typ | SCLK Delay from MCLK |

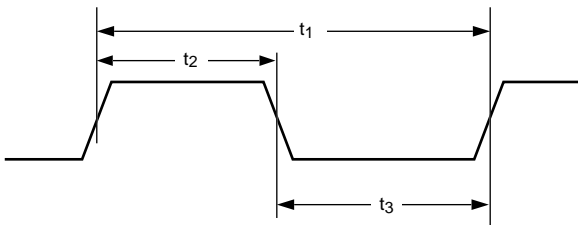


Figure 1. MCLK Timing

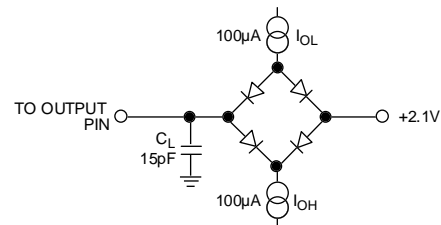


Figure 2. Load Circuit for Timing Specifications

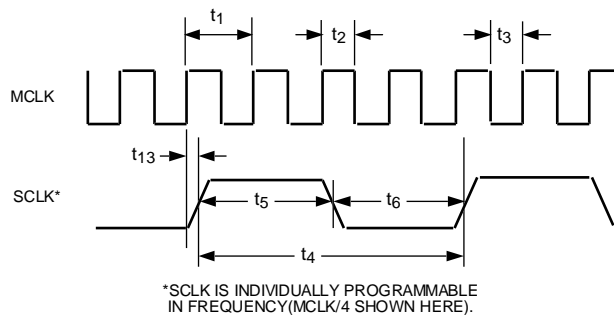


Figure 3. SCLK Timing

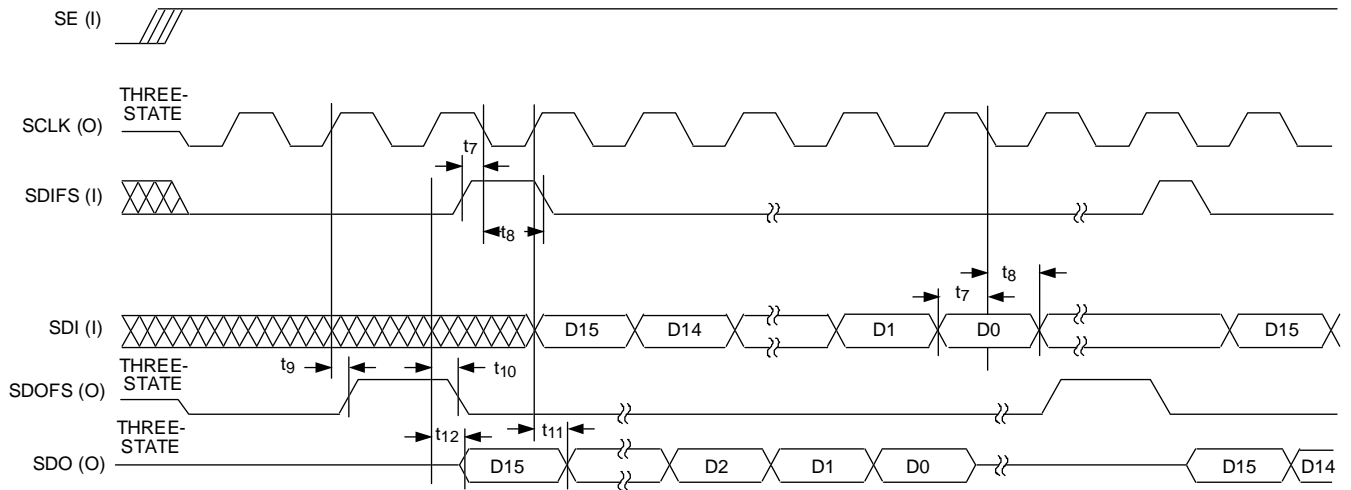


Figure 4. Serial Port (SPORT)

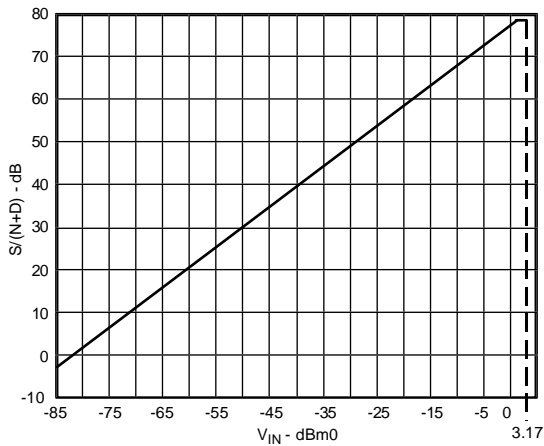


Figure 5a. S/(N+D) vs. VIN (ADC @ 3 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

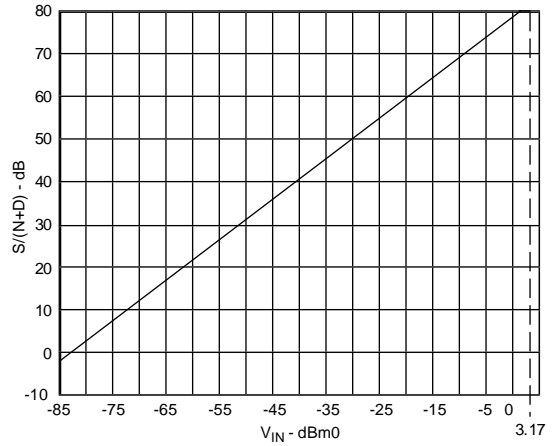


Figure 5c. S/(N+D) vs. VIN (ADC @ 5 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

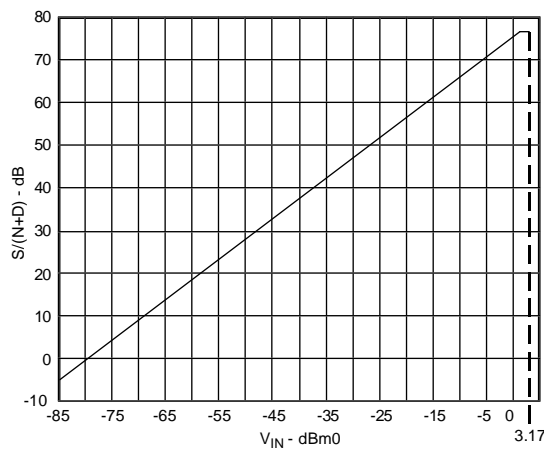


Figure 5b. S/(N+D) vs. VIN (DAC @ 3 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

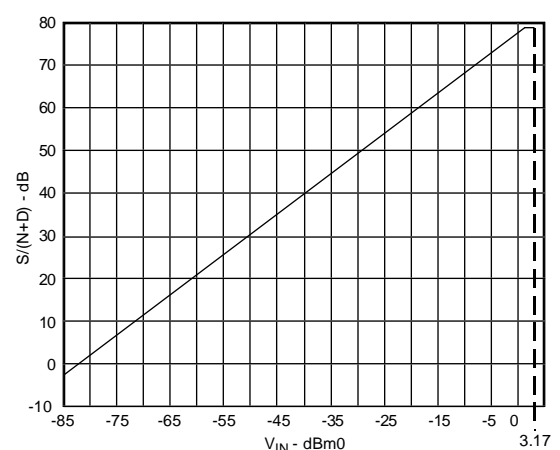


Figure 5d. S/(N+D) vs. VIN (DAC @ 5 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

| | |
|---|------------------------|
| AVDD, DVDD to GND | −0.3 V to +7 V |
| AGND to DGND | −0.3 V to +0.3 V |
| Digital I/O Voltage to DGND | −0.3 V to DVDD + 0.3 V |
| Analog I/O Voltage to AGND | −0.3 V to AVDD + 0.3 V |
| Operating Temperature Range | |
| Industrial (A Version) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Junction Temperature | +150°C |
| SOIC, θ _{JA} Thermal Impedance | 75°C/W |
| Lead Temperature, Soldering | |
| Vapor Phase (60 sec) | +215°C |
| Infrared (15 sec) | +220°C |

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

| Model | Temperature Range | Package Option ¹ |
|-----------------------------|--|-----------------------------|
| AD73322AR EVAL-AD73322EB | −40°C to +85°C Evaluation Board ² +EZ-Kit Lite Upgrade ³ | R-28 |
| EVAL-AD73322EZ | Evaluation Board ² +EZ-Kit Lite ⁴ | |

NOTES

¹R = 0.3" Small Outline IC (SOIC).

²The AD73322 evaluation board features a selectable number of codecs in cascade (from 1 to 4). It can be interfaced to an ADSP-2181 EZ-KIT Lite or to a Texas Instruments EVM kit.

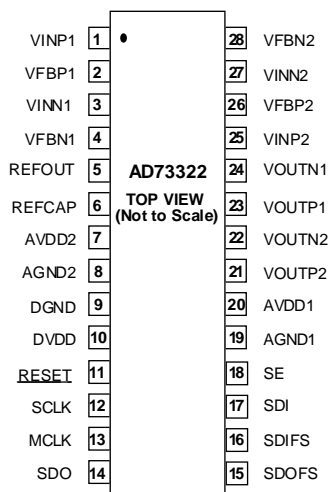
³The upgrade consists of a replacement PROM and connector. This option is intended for existing owners of EZ-Kit Lite.

⁴The EZ-Kit Lite has been modified to allow it to interface with the AD73322 evaluation board. This option is intended for users who do not already have an EZ-Kit Lite.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73322 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PRELIMINARY

PIN FUNCTION DESCRIPTION

| Pin Number | Mnemonic | Function |
|------------|---------------------------|---|
| 1 | VINP1 | Analog Input to the Positive Terminal of Input Channel 1. |
| 2 | VFBP1 | Analog Output forming the feedback path from the output of the positive input inverting amplifier on Channel 1. |
| 3 | VINN1 | Analog Input to the Positive Terminal of Input Channel 1. |
| 4 | VFBN1 | Analog Output forming the feedback path from the output of the negative input inverting amplifier on Channel 1. |
| 5 | REFOUT | Buffered Reference Output, which has a nominal value of 1.2 V or 2.4 V, the value being dependent on the status of Bit 5VEN (CRC:7). |
| 6 | REFCAP | A Bypass Capacitor to AGND2 of 0.1 μ F is required for the on-chip reference. The capacitor should be fixed to this pin. |
| 7 | AVDD2 | Analog Power Supply Connection for Codec 2. |
| 8 | AGND2 | Analog Ground/Substrate Connection for Codec 2. |
| 9 | DGND | Digital Ground/Substrate Connection. |
| 10 | DVDD | Digital Power Supply Connection. |
| 11 | $\overline{\text{RESET}}$ | Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry. |
| 12 | SCLK | Output Serial Clock whose rate determines the serial transfer rate to/from the codec. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider. |
| 13 | MCLK | Master Clock Input. MCLK is driven from an external clock signal. |
| 14 | SDO | Serial Data Output of the Codec. Both data and control information may be output on this pin and is clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low. |
| 15 | SDOFS | Framing Signal Output for SDO Serial Transfers. The frame sync is one-bit wide and it is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low. |
| 16 | SDIFS | Framing Signal Input for SDI Serial Transfers. The frame sync is one-bit wide and it is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low. |
| 17 | SDI | Serial Data Input of the Codec. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low. |
| 18 | SE | SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low), however the timing counters and other internal registers are at their reset values. |
| 19 | AGND1 | Analog Ground Connection for Codec 1. |
| 20 | AVDD1 | Analog Power Supply Connection for Codec 1. |
| 21 | VOUTP2 | Analog Output from the Positive Terminal of Output Channel 2. |
| 22 | VOUTN2 | Analog Output from the Negative Terminal of Output Channel 2. |
| 23 | VOUTP1 | Analog Output from the Positive Terminal of Output Channel 1. |
| 24 | VOUTN1 | Analog Output from the Negative Terminal of Output Channel 1. |
| 25 | VINP2 | Analog Input to the Positive Terminal of Input Channel 2. |
| 26 | VFBP2 | Analog Output forming the feedback path from the output of the positive input inverting amplifier on Channel 2. |
| 27 | VINN2 | Analog Input to the Negative Terminal of Input Channel 2. |
| 28 | VFBN2 | Analog Output forming the feedback path from the output of the negative input inverting amplifier on Channel 2. |

TERMINOLOGY

Absolute Gain

Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured (differentially) with a 1 kHz sine wave at 0 dBm0 for the DAC and with a 1 kHz sine wave at 0 dBm0 for the ADC. The absolute gain specification is used for gain tracking error specification.

Crosstalk

Crosstalk is due to coupling of signals from a given channel to an adjacent channel. It is defined as the ratio of the amplitude of the coupled signal to the amplitude of the input signal. Crosstalk is expressed in dB.

Gain Tracking Error

Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 0 dBm0 (equal to absolute gain) at 1 kHz for the DAC and 0 dBm0 (equal to absolute gain) at 1 kHz for the ADC. Gain tracking error at 0 dBm0 (ADC) and 0 dBm0 (DAC) is 0 dB by definition.

Group Delay

Group Delay is defined as the derivative of radian phase with respect to radian frequency, $d\phi(f)/df$. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay from a constant indicates the degree of nonlinear phase response of the system.

Idle Channel Noise

Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300 Hz–3400 Hz).

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where $m, n = 0, 1, 2, 3$, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For final testing, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$.

Power Supply Rejection

Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Sample Rate

The sample rate is the rate at which the ADC updates its output register and the DAC updates its output from its input register. It is fixed relative to the DMCLK ($= DMCLK/256$) and therefore may only be changed by changing the DMCLK.

SNR+THD

Signal-to-noise ratio plus harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300 Hz–3400 Hz, including harmonics but excluding dc.

ABBREVIATIONS

| | |
|--------------|---|
| ADC | Analog-to-Digital Converter. |
| AGT | Analog Gain Tap |
| ALB | Analog Loop-Back. |
| BW | Bandwidth. |
| CR x | A Control Register where x is a placeholder for an alphabetic character (A–E). There are five read/write control registers on the AD73322—designated CRA through CRE. |
| CR x : n | A bit position, where n is a placeholder for a numeric character (0–7), within a control register; where x is a placeholder for an alphabetic character (A–E). Position 7 represents the MSB and Position 0 represents the LSB. |
| DAC | Digital-to-Analog Converter. |
| DGT | Digital Gain Tap |
| DLB | Digital Loop-Back. |
| DMCLK | Device (Internal) Master Clock. This is the internal master clock resulting from the external master clock (MCLK) being divided by the on-chip master clock divider. |
| FSLB | Frame Sync Loop Back—where the SDOFS of the final device in a cascade is connected to the RFS and TFS of the DSP and the SDIFS of first device in the cascade. Data input and output occur simultaneously. In the case of Non-FSLB, SDOFS and SDO are connected to the Rx Port of the DSP while SDIFS and SDI are connected to the Tx Port. |
| PGA | Programmable Gain Amplifier. |
| SC | Switched Capacitor. |
| SNR | Signal-to-Noise Ratio. |
| SPORT | Serial Port. |
| THD | Total Harmonic Distortion. |
| VBW | Voice Bandwidth. |

FUNCTIONAL DESCRIPTION

Encoder Channel

The encoder channel consists of a pair of inverting op-amps with feedback connections which can be bypassed if required, a switched capacitor PGA and a sigma-delta analog-to-digital converter (ADC). An on-board digital filter, which forms part of the sigma-delta ADC, also performs critical system-level filtering. Due to the high level of oversampling, the input antialias requirements are reduced such that a simple single pole RC stage is sufficient to give adequate attenuation in the band of interest.

Programmable Gain Amplifier

The encoder section's analog front end comprises a switched capacitor PGA which also forms part of the sigma-delta modulator. The SC sampling frequency is $DMCLK/8$. The PGA, whose programmable gain settings are shown in Table IV, may be used to increase the signal level applied to the ADC from low output sources such as microphones, and can be used to avoid placing external amplifiers in the circuit. The input signal level to the sigma-delta modulator should not exceed the maximum input voltage permitted.

The PGA gain is set by bits IGS0, IGS1 and IGS2 (CRD:0-2) in control register D.

Table IV. PGA Settings for the Encoder Channel

| IGS2 | IGS1 | IGS0 | Gain (dB) |
|------|------|------|-----------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 6 |
| 0 | 1 | 0 | 12 |
| 0 | 1 | 1 | 18 |
| 1 | 0 | 0 | 20 |
| 1 | 0 | 1 | 26 |
| 1 | 1 | 0 | 32 |
| 1 | 1 | 1 | 38 |

ADC

The ADC consists of an analog sigma-delta modulator and a digital antialiasing decimation filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a $DMCLK/8$ rate. This bit-stream, representing the analog input signal, is input to the antialiasing decimation filter. The decimation filter reduces the sample rate and increases the resolution.

Analog Sigma-Delta Modulator

The AD73322 input channel employs a sigma-delta conversion technique, which provides a high resolution 16-bit output with system filtering being implemented on-chip.

Sigma-delta converters employ a technique known as oversampling where the sampling rate is many times the highest frequency of interest. In the case of the AD73322, the initial sampling rate of the sigma-delta modulator is $DMCLK/8$. The main effect of oversampling is that the quantization noise is spread over a very

wide bandwidth, up to $F_S/2 = DMCLK/16$ (Figure 6a). This means that the noise in the band of interest is much reduced. Another complementary feature of sigma-delta converters is the use of a technique called noise-shaping. This technique has the effect of pushing the noise from the band of interest to an out-of-band position (Figure 6b). The combination of these techniques, followed by the application of a digital filter, reduces the noise in band sufficiently to ensure good dynamic performance from the part (Figure 6c).

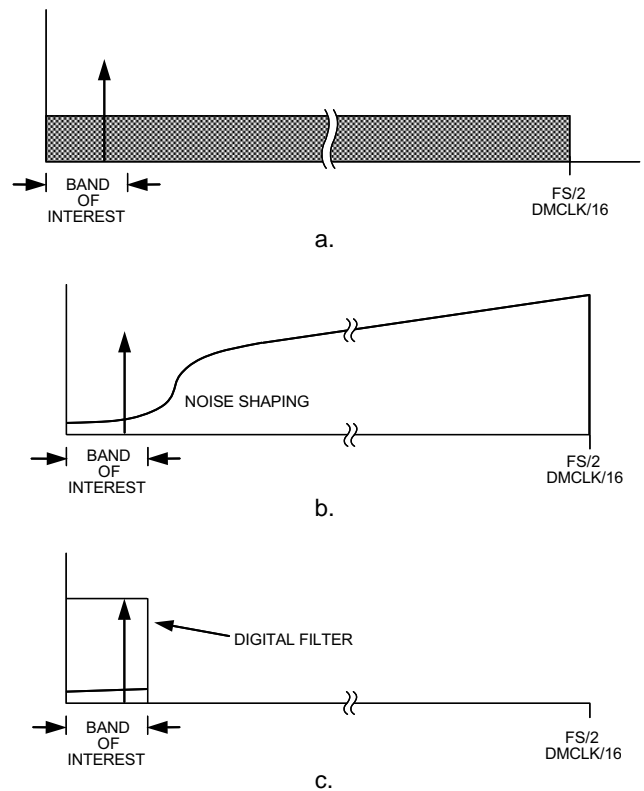
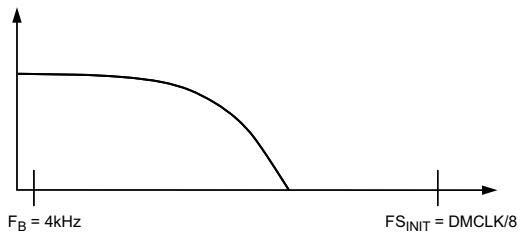
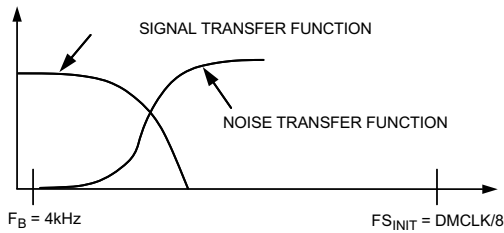


Figure 6. Sigma-Delta Noise Reduction

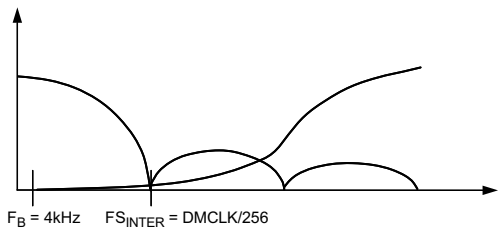
Figure 7 shows the various stages of filtering that are employed in a typical AD73322 application. In Figure 7a we see the transfer function of the external analog antialias filter. Even though it is a single RC pole, its cutoff frequency is sufficiently far away from the initial sampling frequency ($DMCLK/8$) that it takes care of any signals that could be aliased by the sampling frequency. This also shows the major difference between the initial oversampling rate and the bandwidth of interest. In Figure 7b, the signal and noise shaping responses of the sigma-delta modulator are shown. The signal response provides further rejection of any high frequency signals while the noise shaping will push the inherent quantization noise to an out-of-band position. The detail of Figure 7c shows the response of the digital decimation filter (Sinc-cubed response) with nulls every multiple of $DMCLK/256$, which is the decimation filter update rate. The final detail in Figure 7d shows the application of a final antialias filter in the DSP engine. This has the advantage of being implemented according to the user's requirements and available MIPS. The filtering in Figures 7a through 7c is implemented in the AD73322.



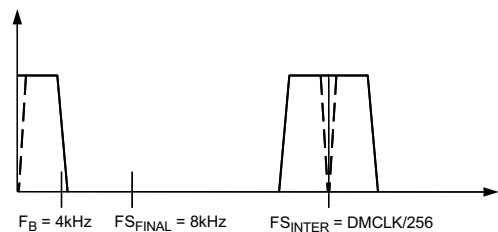
a. Analog Antialias Filter Transfer Function



b. Analog Sigma-Delta Modulator Transfer Function



c. Digital Decimator Transfer Function



d. Final Filter LPF (HPF) Transfer Function
Figure 7. AD73322 ADC Frequency Responses

Decimation Filter

The digital filter used in the AD73322 carries out two important functions. Firstly, it removes the out-of-band quantization noise, which is shaped by the analog modulator and secondly, it decimates the high frequency bit-stream to a lower rate 15-bit word.

The antialiasing decimation filter is a sinc-cubed digital filter that reduces the sampling rate from DMCLK/8 to DMCLK/256, and increases the resolution from a single bit to 15 bits. Its Z transform is given as: $[(1-Z^{-32})/(1-Z^{-1})]^3$. This ensures a minimal group delay of 25 μ s.

ADC Coding

The ADC coding scheme is in twos complement format (see Figure 8). The output words are formed by the decimation filter, which grows the word length from the single-bit output of the sigma-delta modulator to a 15-bit word, which is the final output of the ADC block. In 16-bit Data Mode this value is left shifted with the LSB being set to 0. For input values equal to or greater than positive full scale, however, the output word is set at 0x7FFF, which has the LSB set to 1. In mixed Control/Data

Mode, the resolution is fixed at 15 bits, with the MSB of the 16-bit transfer being used as a flag bit to indicate either control or data in the frame.

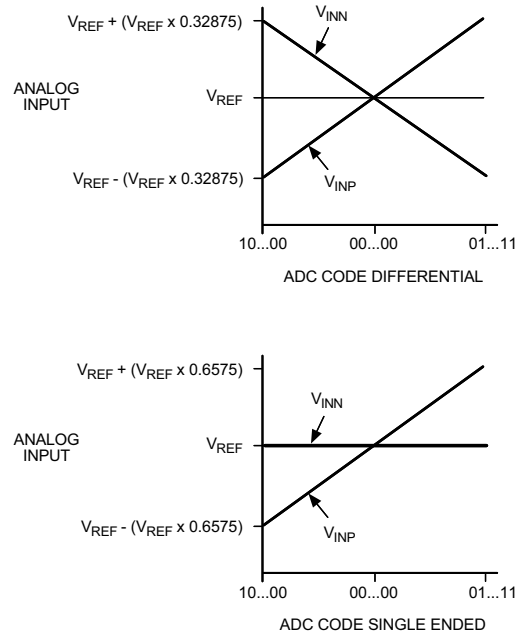


Figure 8. ADC Transfer Function

Decoder Channel

The decoder channel consists of a digital interpolator, digital sigma-delta modulator, a single bit digital-to-analog converter (DAC), an analog smoothing filter and a programmable gain amplifier with differential output.

DAC Coding

The DAC coding scheme is in twos complement format with 0x7FFF being full-scale positive and 0x8000 being full-scale negative.

Interpolation Filter

The anti-imaging interpolation filter is a sinc-cubed digital filter which up-samples the 16-bit input words from a rate of DMCLK/256 to a rate of DMCLK/8 while filtering to attenuate images produced by the interpolation process. Its Z transform is given as: $[(1-Z^{-32})/(1-Z^{-1})]^3$. The DAC receives 16-bit samples from the host DSP processor at a rate of DMCLK/256. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered by the anti-imaging interpolation filter, but there is an option to bypass the interpolator for the minimum group delay configuration by setting the IBYP bit (CRE:5) of Control register E. The interpolation filter has the same characteristics as the ADC's antialiasing decimation filter.

The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples at a rate of DMCLK/8. The modulator noise-shapes the signal so that errors inherent to the process are minimized in the passband of the converter. The bit-stream output of the sigma-delta modulator is fed to the single bit DAC where it is converted to an analog voltage.

Analog Smoothing Filter & PGA

The output of the single-bit DAC is sampled at DMCLK/8, therefore it is necessary to filter the output to reconstruct the

low frequency signal. The decoder's analog smoothing filter consists of a continuous-time filter preceded by a third-order switched-capacitor filter. The continuous-time filter forms part of the output programmable gain amplifier (PGA). The PGA can be used to adjust the output signal level from -15 dB to +6 dB in 3 dB steps, as shown in Table V. The PGA gain is set by bits OGS0, OGS1 and OGS2 (CRD:4-6) in Control Register D.

Table V. PGA Settings for the Decoder Channel

| OG2 | OG1 | OG0 | Gain (dB) |
|-----|-----|-----|-----------|
| 0 | 0 | 0 | +6 |
| 0 | 0 | 1 | +3 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | -3 |
| 1 | 0 | 0 | -6 |
| 1 | 0 | 1 | -9 |
| 1 | 1 | 0 | -12 |
| 1 | 1 | 1 | -15 |

Differential Output Amplifiers

The decoder has a differential analog output pair (VOUTP and VOUTN). The output channel can be muted by setting the MUTE bit (CRD:7) in Control Register D. The output signal is dc-biased to the codec's on-chip voltage reference.

Voltage Reference

The AD73322 reference, REFCAP, is a bandgap reference that provides a low noise, temperature-compensated reference to the DAC and ADC. A buffered version of the reference is also made available on the REFOUT pin and can be used to bias other external analog circuitry. The reference has a default nominal value of 1.2 V but can be set to a nominal value of 2.4 V by setting the 5VEN bit (CRC:7) of CRC. The 5 V mode is generally only usable when V_{DD} = 5 V.

The reference output (REFOUT) can be enabled for biasing external circuitry by setting the RU bit (CRC:6) of CRC.

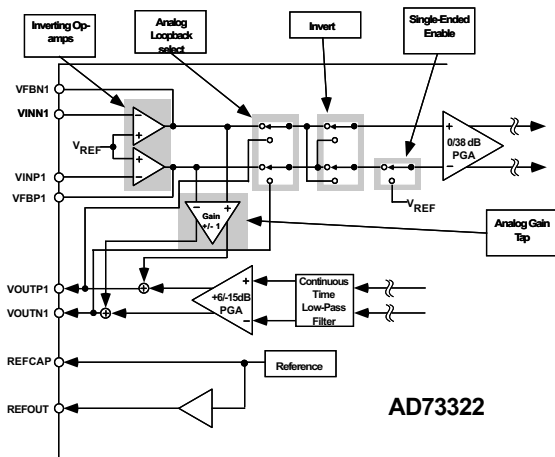


Figure 9. Analog Input/Output Section

Analog and Digital Gain Taps

The AD73322 features analog and digital feedback paths between input and output. The amount of feedback is determined by the gain setting which is programmed in the control registers. This feature can typically be used for balancing the effective impedance between input and output when used in Subscriber Line Interface Circuit (SLIC) interfacing.

Analog Gain Tap

The analog gain tap is configured as a programmable differential amplifier whose input is taken from the ADC's input signal path. The output of the analog gain tap is summed with the output of the DAC. The gain is programmable using Control Register F (CRF:0-4) to achieve a gain of -1 to +1 in 32 steps with muting being achieved through a separate control setting (Control Register F Bit). The gain increment per step is 0.0625. The AGT is enabled by powering-up the AGT control bit in the power control register (CRC:1). When this bit is set (=1) CRF becomes an AGT control register with CRF:0-4 holding the AGT coefficient, CRF:5 becomes an AGT enable and CRF:7 becomes an AGT mute control bit. Control bit CRF:5 connects/disconnects the AGT output to the summer block at the output of the DAC section while control bit CRF:7 overrides the gain tap setting with a mute, or zero gain, setting (which is omitted from the gain settings). Table VI shows the gain versus digital setting for the AGT.

Table VI. Analog Gain Tap Settings

| AGTC4 | AGTC3 | AGTC2 | AGTC1 | AGTC0 | Gain |
|-------|-------|-------|-------|-------|---------|
| 0 | 0 | 0 | 0 | 0 | +1.00 |
| 0 | 0 | 0 | 0 | 1 | +0.9375 |
| 0 | 0 | 0 | 1 | 0 | +0.875 |
| 0 | 0 | 0 | 1 | 1 | +0.8125 |
| 0 | 0 | 1 | 0 | 0 | +0.75 |
| - | - | - | - | - | - |
| 0 | 1 | 1 | 1 | 1 | +0.0625 |
| 1 | 0 | 0 | 0 | 0 | -0.0625 |
| - | - | - | - | - | - |
| 1 | 1 | 1 | 0 | 1 | -0.875 |
| 1 | 1 | 1 | 1 | 0 | -0.9375 |
| 1 | 1 | 1 | 1 | 1 | -1.00 |

Digital Gain Tap

The digital gain tap features a programmable gain block whose input is taken from the bitstream from the ADC's sigma-delta modulator. This single bit input (1 or 0) is used to add or subtract a programmable value, which is the digital gain tap setting, to the output of the DAC section's interpolator. The programmable setting has 16 bit resolution and is programmed using the settings in Control Registers and .

Serial Port (SPORT)

The codecs communicate with a host processor via the bidirectional synchronous serial port (SPORT) which is compatible with most modern DSPs. The SPORT is used to transmit and receive digital data and control information. The dual codec is implemented using two separate codec blocks which are internally cascaded with serial port access to the input of codec1 and the output of codec2. This allows other single or dual codec devices to be cascaded together (up to a limit of 8 codec units).

In both transmit and receive modes, data is transferred at the serial clock (SCLK) rate with the MSB being transferred first. Due to the fact that the SPORT of each codec block uses a common serial register for serial input and output, communications between an AD73322 codec and a host processor (DSP engine) must always be initiated by the codecs themselves. In this configuration the codecs are described as being in Master mode. This ensures that there is no collision between input data and output samples.

SPORT Overview

The AD73322 SPORT is a flexible, full-duplex, synchronous serial port whose protocol has been designed to allow up to four AD73322 devices (or combinations of AD73322 dual codecs and AD73311 single codecs up to 8 codec blocks) to be connected, in cascade, to a single DSP via a six-wire interface. It has a very flexible architecture that can be configured by programming two of the internal control registers in each codec block. The AD73322 SPORT has three distinct modes of operation: Control Mode, Data Mode and Mixed Control/Data Mode.

NOTE: As each codec has its own SPORT section, the register settings in both SPORTs must be programmed. The registers which control SPORT and sample rate operation (CRA & CRB) must be programmed with the same values, otherwise incorrect operation may occur.

In Control Mode (CRA:0 = 0), the device's internal configuration can be programmed by writing to the five internal control registers. In this mode, control information can be written to or read from the codec. In Data Mode (CRA:0 = 1), information that is sent to the device is used to update the decoder section (DAC), while the encoder section (ADC) data is read from the device. In this mode, only DAC and ADC data is written to or read from the device. Mixed mode (CRA:0 = 1 and CRA:1 = 1) allows the user to choose whether the information being sent to the device contains either control information or DAC data. This is achieved by using the MSB of the 16-bit frame as a flag bit. Mixed mode reduces the resolution to 15 bits with the MSB being used to indicate whether the information in the 16-bit frame is control information or DAC/ADC data.

The SPORT features a single 16-bit serial register that is used for both input and output data transfers. As the input and output data must share the same register there are some precautions that must be observed. The primary precaution is that no information must be written to the SPORT without reference to an output sample event, which is when the serial register will be overwritten with

the latest ADC sample word. Once the SPORT starts to output the latest ADC word then it is safe for the DSP to write new control or data words to the codec. In certain configurations, data can be written to the device to coincide with the output sample being shifted out of the serial register—see section on interfacing devices. The serial clock rate (CRB:2–3) defines how many 16-bit words can be written to a device before the next output sample event will happen.

The SPORT block diagram, shown in Figure 10, details the blocks associated with codecs 1 and 2 including the eight control registers (A–H), external MCLK to internal DMCLK divider and serial clock divider. The divider rates are controlled by the setting of Control Register B. The AD73322 features a master clock divider that allows users the flexibility of dividing externally available high frequency DSP or CPU clocks to generate a lower frequency master clock internally in the codec which may be more suitable for either serial transfer or sampling rate requirements. The master clock divider has five divider options ($\div 1$ default condition, $\div 2$, $\div 3$, $\div 4$, $\div 5$) that are set by loading the master clock divider field in Register B with the appropriate code (see table VI). Once the internal device master clock (DMCLK) has been set using the master clock divider, the sample rate and serial clock settings are derived from DMCLK.

The SPORT can work at four different serial clock (SCLK) rates: chosen from DMCLK, DMCLK/2, DMCLK/4 or DMCLK/8, where DMCLK is the internal or device master clock resulting from the external or pin master clock being divided by the master clock divider. When working at the lower SCLK rate of DMCLK/8, which is intended for interfacing with slower DSPs, the SPORT will support a maximum of two codecs in cascade (a single AD73322 or two AD73311s) with the sample rate of DMCLK/256.

SPORT Register Maps

There are two register banks for each codec in the AD73322: the control register bank and the data register bank. The control register bank consists of eight read/write registers, each 8 bits wide. Table IX shows the control register map for the AD73322. The first two control registers, CRA and CRB, are reserved for controlling the SPORT. They hold settings for parameters such as bit rate, internal master clock rate and device count. As both codecs are internally cascaded, registers CRA and CRB on each codec must be programmed with the same setting to ensure correct operation (this is shown in the programming examples). The other five registers; CRC through CRH are used to hold control settings for the ADC, DAC, Reference, Power Control and Gain Tap sections of the device. It is not necessary that the contents of CRC through CRH on each codec are similar. Control registers are written to on the negative edge of SCLK. The data register bank consists of two 16-bit registers that are the DAC and ADC registers.

Master Clock Divider

The AD73322 features a programmable master clock divider that allows the user to reduce an externally available master clock, at pin MCLK, by one of the ratios 1,

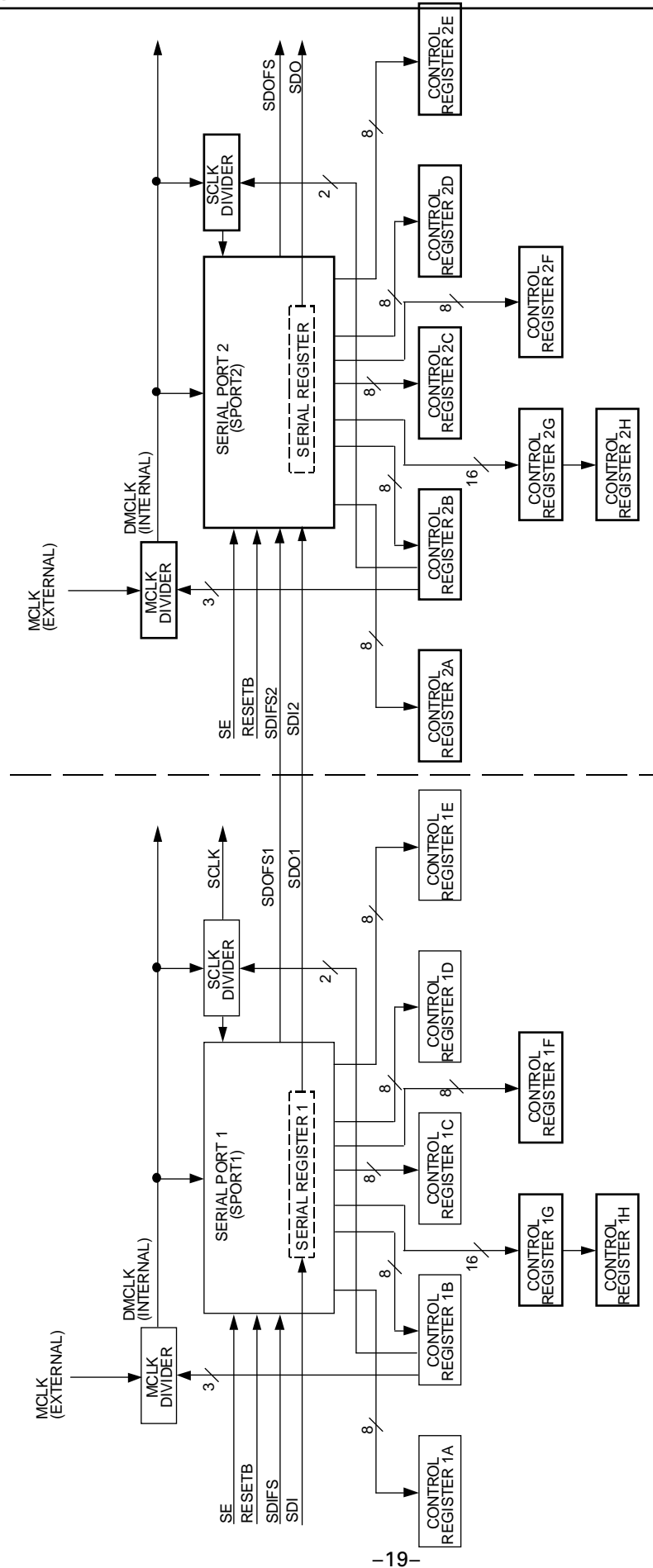


Figure 10. SPORT Block Diagram

2, 3, 4 or 5 to produce an internal master clock signal (DMCLK) that is used to calculate the sampling and serial clock rates. The master clock divider is programmable by setting CRB:4-6. Table VII shows the division ratio corresponding to the various bit settings. The default divider ratio is divide by one.

Table VII. DMCLK (Internal) Rate Divider Settings

| MCD2 | MCD1 | MCD0 | DMCLK Rate |
|------|------|------|------------|
| 0 | 0 | 0 | MCLK |
| 0 | 0 | 1 | MCLK/2 |
| 0 | 1 | 0 | MCLK/3 |
| 0 | 1 | 1 | MCLK/4 |
| 1 | 0 | 0 | MCLK/5 |
| 1 | 0 | 1 | MCLK |
| 1 | 1 | 0 | MCLK |
| 1 | 1 | 1 | MCLK |

Serial Clock Rate Divider

The AD73322 features a programmable serial clock divider that allows users to match the serial clock (SCLK) rate of the data to that of the DSP engine or host processor. The maximum SCLK rate available is DMCLK and the other available rates are: DMCLK/2, DMCLK/4 and DMCLK/8. The slowest rate (DMCLK/8) is the default SCLK rate. The serial clock divider is programmable by setting bits CRB:2-3. Table VIII shows the serial clock rate corresponding to the various bit settings.

Table VIII. SCLK Rate Divider Settings

| SCDI | SCD0 | SCLK Rate |
|------|------|-----------|
| 0 | 0 | DMCLK/8 |
| 0 | 1 | DMCLK/4 |
| 1 | 0 | DMCLK/2 |
| 1 | 1 | DMCLK |

Sample Rate Divider

The AD73322 features a programmable sample rate divider that allows users flexibility in matching the codec's ADC and DAC sample rates to the needs of the DSP software. The maximum sample rate available is DMCLK/256 and the other available rates are: DMCLK/512, DMCLK/1024 and DMCLK/2048. The slowest rate (DMCLK/2048) is the default sample rate. The sample rate divider is programmable by setting bits CRB:0-1. Table IX shows the sample rate corresponding to the various bit settings.

Table IX. Sample Rate Divider Settings

| SRDI | SRD0 | SCLK Rate |
|------|------|------------|
| 0 | 0 | DMCLK/2048 |
| 0 | 1 | DMCLK/1024 |
| 1 | 0 | DMCLK/512 |
| 1 | 1 | DMCLK/256 |

DAC Advance Register

The loading of the DAC is internally synchronized with the unloading of the ADC data in each sampling interval. The default DAC load event happens one SCLK cycle before the SDOFS flag is raised by the ADC data being ready. However, this DAC load position can be advanced before this time by modifying the contents of the DAC Advance field in Control Register E (CRE:0-4). The field is five-bits wide, allowing 31 increments of weight $1/(F_S*32)$; see Table X. The sample rate F_S is dependent on the setting of both the MCLK divider and the Sample Rate divider; see Tables VII and IX. In certain circumstances this DAC update adjustment can reduce the group delay when the ADC and DAC are used to process data in series. Appendix _ details how the DAC advance feature can be used.

NOTE: The DAC advance register should not be changed while the DAC section is powered up.

Table X. DAC Timing Control

| DA4 | DA3 | DA2 | DA1 | DA0 | Time Advance |
|-----|-----|-----|-----|-----|-----------------|
| 0 | 0 | 0 | 0 | 0 | 0 s |
| 0 | 0 | 0 | 0 | 1 | $1/(F_S*32)$ s |
| 0 | 0 | 0 | 1 | 0 | $2/(F_S*32)$ s |
| 1 | 1 | 1 | 1 | 0 | $30/(F_S*32)$ s |
| 1 | 1 | 1 | 1 | 1 | $31/(F_S*32)$ s |

Table XI. Control Register Map

| Address (Binary) | Name | Description | Type | Width | Reset Setting (Hex) |
|------------------|------|--------------------|------|-------|---------------------|
| 000 | CRA | Control Register A | R/W | 8 | 0x00 |
| 001 | CRB | Control Register B | R/W | 8 | 0x00 |
| 010 | CRC | Control Register C | R/W | 8 | 0x00 |
| 011 | CRD | Control Register D | R/W | 8 | 0x00 |
| 100 | CRE | Control Register E | R/W | 8 | 0x00 |
| 101 to 111 | | Reserved | | | |

OPERATION

Resetting the AD73322

The pin RESET resets all the control registers. All registers are reset to zero indicating that the default SCLK rate (DMCLK/8) and sample rate (DMCLK/2048) are at a minimum to ensure that slow speed DSP engines can communicate effectively. As well as resetting the control registers using the RESET pin, the device can be reset using the RESET bit (CRA:7) in Control Register A. Both hardware and software resets require 4 DMCLK cycles. On reset, DATA/PGM (CRA:0) is set to 0 (default condition) thus enabling Program Mode. The reset conditions ensure that the device must be programmed to the correct settings after power-up or reset. Following a reset, the SDOFS will be asserted 280 DMCLK cycles after RESET going high. The data that is output following RESET and during Program Mode is random and contains no valid information until either data or mixed mode is set.

Power Management

The individual functional blocks of the AD73322 can be enabled separately by programming the power control register CRC. It allows certain sections to be powered down if not required, which adds to the device's flexibility in that the user

need not incur the penalty of having to provide power for a certain section if it is not necessary to their design. The power control registers provides individual control settings for the major functional blocks on each codec unit and also a global override that allows all sections to be powered up by setting the bit. Using this method the user could, for example, individually enable a certain section, such as the reference (CRC:5), and disable all others. The global power-up (CRC:0) can be used to enable all sections but if power-down is required using the global control, the reference will still be enabled, in this case, because its individual bit is set. Refer to Table XIII for details of the settings of CRC.

NOTE: As both codec units share a common reference, the reference control bits (CRC:5-7) in each SPORT are wire ORed to allow either device to control the reference. Hence the reference is only in a reset state when the relevant control bit of both codec units is set to 0.

Operating Modes

There are five operating modes available on the AD73322. Two of these—SPORT Loop-Back and Digital Loop-Back—are reserved as diagnostic modes with the other three, Program, Data and Mixed Program/Data, being available for general

Table XII. Control Word Description

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|----------------|----|----|------------------|---|---|---------------|---|---|---|---|---|---|---|
| C/D | R/W | DEVICE ADDRESS | | | REGISTER ADDRESS | | | REGISTER DATA | | | | | | | |

| Control | Frame | Description |
|-----------|------------------|--|
| Bit 15 | Control/Data | When set high, it signifies a control word in Program or Mixed Program/Data Modes. When set low, it signifies a data word in Mixed Program/Data Mode or an invalid control word in Program Mode. |
| Bit 14 | Read/Write | When set low, it tells the device that the data field is to be written to the register selected by the register field setting provided the address field is zero. When set high, it tells the device that the selected register is to be written to the data field in the input serial register and that the new control word is to be output from the device via the serial output. |
| Bit 13–11 | Device Address | This 3-bit field holds the address information. Only when this field is zero is a device selected. If the address is not zero, it is decremented and the control word is passed out of the device via the serial output. |
| Bits 10–8 | Register Address | This 3-bit field is used to select one of the five control registers on the AD73322. |
| Bits 7–0 | Register Data | This 8-bit field holds the data that is to be written to or read from the selected register provided the address field is zero. |

Table XIII. Control Register A Description

CONTROL REGISTER A

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|----|--------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESET | DC2 | DC1 | DC0 | SLB | DLB | MM | DATA/ PGM |

| Bit | Name | Description |
|-----|----------|---|
| 0 | DATA/PGM | Operating Mode (0 = Program; 1 = Data Mode) |
| 1 | MM | Mixed Mode (0 = Off; 1 = Enabled) |
| 2 | DLB | Digital Loop-Back Mode (0 = Off; 1 = Enabled) |
| 3 | SLB | SPORT Loop-Back Mode (0 = Off; 1 = Enabled) |
| 4 | DC0 | Device Count (Bit 0) |
| 5 | DC1 | Device Count (Bit 1) |
| 6 | DC2 | Device Count (Bit 2) |
| 7 | RESET | Software Reset (0 = Off; 1 = Initiates Reset) |

Table XIV. Control Register B Description

CONTROL REGISTER B

| | | | | | | | |
|-----|------|------|------|------|------|------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CEE | MCD2 | MCD1 | MCD0 | SCD1 | SCD0 | DIR1 | DIR0 |

| Bit | Name | Description |
|-----|------|--|
| 0 | DIR0 | Decimation/Interpolation Rate (Bit 0) |
| 1 | DIR1 | Decimation/Interpolation Rate (Bit 1) |
| 2 | SCD0 | Serial Clock Divider (Bit 0) |
| 3 | SCD1 | Serial Clock Divider (Bit 1) |
| 4 | MCD0 | Master Clock Divider (Bit 0) |
| 5 | MCD1 | Master Clock Divider (Bit 1) |
| 6 | MCD2 | Master Clock Divider (Bit 2) |
| 7 | CEE | Control Echo Enable (0 = Off; 1 = Enabled) |

Table XV. Control Register C Description

CONTROL REGISTER C

| | | | | | | | |
|------|----|-------|-------|-------|------|-------|----|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 5VEN | RU | PUREF | PUDAC | PUADC | PUIA | PUAGT | PU |

| Bit | Name | Description |
|-----|-------|---|
| 0 | PU | Power-Up Device (0 = Power Down; 1 = Power On) |
| 1 | PUAGT | Analog Gain Tap Power (0 = Power Down; 1 = Power On) |
| 2 | PUIA | Input Amplifier Power (0 = Power Down; 1 = Power On) |
| 3 | PUADC | ADC Power (0 = Power Down; 1 = Power On) |
| 4 | PUDAC | DAC Power (0 = Power Down; 1 = Power On) |
| 5 | PUREF | REF Power (0 = Power Down; 1 = Power On) |
| 6 | RU | REFOUT Use (0 = Disable REFOUT; 1 = Enable REFOUT) |
| 7 | 5VEN | Enable 5 V Operating Mode (0 = Disable 5 V Mode; 1 = Enable 5 V Mode) |

Table XVI. Control Register D Description

CONTROL REGISTER D

| | | | | | | | |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MUTE | OGS2 | OGS1 | OGS0 | RMOD | IGS2 | IGS1 | IGS0 |

| Bit | Name | Description |
|-----|------|--|
| 0 | IGS0 | Input Gain Select (Bit 0) |
| 1 | IGS1 | Input Gain Select (Bit 1) |
| 2 | IGS2 | Input Gain Select (Bit 2) |
| 3 | RMOD | Reset ADC Modulator (0 = Off; 1 = Reset Enabled) |
| 4 | OGS0 | Output Gain Select (Bit 0) |
| 5 | OGS1 | Output Gain Select (Bit 1) |
| 6 | OGS2 | Output Gain Select (Bit 2) |
| 7 | MUTE | Output Mute (0 = Mute Off; 1 = Mute Enabled) |

Table XVII. Control Register E Description

CONTROL REGISTER E

| | | | | | | | |
|------------|-------------|-------------|------------|------------|------------|------------|------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TME | DGTE | IBYP | DA4 | DA3 | DA2 | DA1 | DA0 |

| Bit | Name | Description |
|-----|------|---|
| 0 | DA0 | DAC Advance Setting (Bit 0) |
| 1 | DA1 | DAC Advance Setting (Bit 1) |
| 2 | DA2 | DAC Advance Setting (Bit 2) |
| 3 | DA3 | DAC Advance Setting (Bit 3) |
| 4 | DA4 | DAC Advance Setting (Bit 4) |
| 5 | IBYP | Interpolator Bypass (0 = Bypass Disabled; 1 = Bypass Enabled) |
| 6 | DGTE | Digital Gain Tap Enable (0 = Disabled; 1 = Enabled) |
| 7 | TME | Test Mode Enable (0 = Disabled; 1 = Enabled) |

Table XVIII. Control Register F Description

CONTROL REGISTER F

| | | | | | | | |
|-----------------|------------|------------------|--------------|--------------|--------------|--------------|--------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ALB/AGTM | INV | SEEN/AGTE | AGTC4 | AGTC3 | AGTC2 | AGTC1 | AGTC0 |

| Bit | Name | Description |
|-----|-------|--|
| 0 | AGTC0 | Analog Gain Tap Coefficient (Bit 0) |
| 1 | AGTC1 | Analog Gain Tap Coefficient (Bit 1) |
| 2 | AGTC2 | Analog Gain Tap Coefficient (Bit 2) |
| 3 | AGTC3 | Analog Gain Tap Coefficient (Bit 3) |
| 4 | AGTC4 | Analog Gain Tap Coefficient (Bit 4) |
| 5 | SEEN | Single-Ended Enable (0 = Disabled; 1 = Enabled) |
| | AGTE | Analog Gain Tap Enable (0 = Disabled; 1 = Enabled) |
| 6 | INV | Input Invert(0 = Disabled; 1 = Enabled) |
| 7 | ALB | Analog Loopback of Output to Input (0 = Disabled; 1 = Enabled) |
| | AGTM | Analog Gain Tap Mute (0 = Off; 1 = Muted) |

Table XIX. Control Register G Description

CONTROL REGISTER G

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DGTC7 | DGTC6 | DGTC5 | DGTC4 | DGTC3 | DGTC2 | DGTC1 | DGTC0 |

| Bit | Name | Description |
|-----|-------|--------------------------------------|
| 0 | DGTC0 | Digital Gain Tap Coefficient (Bit 0) |
| 1 | DGTC1 | Digital Gain Tap Coefficient (Bit 1) |
| 2 | DGTC2 | Digital Gain Tap Coefficient (Bit 2) |
| 3 | DGTC3 | Digital Gain Tap Coefficient (Bit 3) |
| 4 | DGTC4 | Digital Gain Tap Coefficient (Bit 4) |
| 5 | DGTC5 | Digital Gain Tap Coefficient (Bit 5) |
| 6 | DGTC6 | Digital Gain Tap Coefficient (Bit 6) |
| 7 | DGTC7 | Digital Gain Tap Coefficient (Bit 7) |

Table XX. Control Register H Description

CONTROL REGISTER H

| | | | | | | | |
|--------|--------|--------|--------|--------|--------|-------|-------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DGTC15 | DGTC14 | DGTC13 | DGTC12 | DGTC11 | DGTC10 | DGTC9 | DGTC8 |

| Bit | Name | Description |
|-----|--------|---------------------------------------|
| 0 | DGTC8 | Digital Gain Tap Coefficient (Bit 8) |
| 1 | DGTC9 | Digital Gain Tap Coefficient (Bit 9) |
| 2 | DGTC10 | Digital Gain Tap Coefficient (Bit 10) |
| 3 | DGTC11 | Digital Gain Tap Coefficient (Bit 11) |
| 4 | DGTC12 | Digital Gain Tap Coefficient (Bit 12) |
| 5 | DGTC13 | Digital Gain Tap Coefficient (Bit 13) |
| 6 | DGTC14 | Digital Gain Tap Coefficient (Bit 14) |
| 7 | DGTC15 | Digital Gain Tap Coefficient (Bit 15) |

purpose use. The device configuration—register settings—can be changed only in Program and Mixed Program/Data Modes. In all modes, transfers of information to or from the device occur in 16-bit packets, therefore the DSP engine’s SPORT will be programmed for 16-bit transfers.

Program (Control) Mode

In Program Mode, CRA:0 = 0, the user writes to the control registers to set up the device for desired operation—SPORT operation, cascade length, power management, input/output gain, etc. In this mode, the 16-bit information packet sent to the device by the DSP engine is interpreted as a control word whose format is shown in Table X. In this mode, the user must address the device to be programmed using the address field of the control word. This field is read by the device and if it is zero (000 bin) then the device recognizes the word as being addressed to it. If the address field is not zero, it is then decremented and the control word is passed out of the device—either to the next device in a cascade or back to the DSP engine. This 3-bit address format allows the user to uniquely address any one of up to eight devices in a cascade; please note that this addressing scheme is valid only in sending control information to the device—a different format is used to send DAC data to the device(s). As the AD73322 is a dual codec, it features two separate device addresses for program-

ming purposes. If the AD73322 is used in a standalone configuration connected to a DSP, the two device addresses correspond to 0 and 1. If on the otherhand the AD73322 is configured in a cascade of multiple dual or single codecs (AD73322 or AD73311), then its device addresses correspond with its hardwired position in the cascade.

Following reset, when the SE pin is enabled, the codec responds by raising the SDOFS pin to indicate that an output sample event has occurred. Control words can be written to the device to coincide with the data being sent out of the SPORT, as shown in Figure 12, or they can lag the output words by a time interval that should not exceed the sample interval. After reset, output frame sync pulses will occur at a slower default sample rate, which is DMCLK/2048, until Control Register B is programmed after which the SDOFS pulses will revert to the DMCLK/256 rate. This is to allow slow controller devices to establish communication with the AD73322. During Program Mode, the data output by the device is random and should not be interpreted as ADC data.

Data Mode

Once the device has been configured by programming the correct settings to the various control registers, the device may exit Program Mode and enter Data Mode. This is done by programming the DATA/PGM (CRA:0) bit to a 1 and MM (CRA:1) to 0. Once the device is in Data Mode, the 16-bit input data frame is now interpreted as DAC data rather than a control frame. This data is therefore loaded directly to the DAC register. In Data Mode, as the entire input data frame contains DAC data, the device relies on counting the number of input frame syncs received at the SDIFS pin. When that number equals the device count stored in the device count field of CRA, the device knows that the present data frame being received is its own DAC update data. When the device is in normal Data Mode (i.e., mixed mode disabled), it must receive a hardware reset to reprogram any of the control register settings. In a single codec configuration, each 16-bit data frame sent from the DSP to the device is interpreted as DAC data. The default device count is 1, therefore each input frame sync will cause the 16-bit data frame to be loaded to the DAC register.

Appendix C details the initialization and operation of a dual codec cascade in normal Data Mode.

Mixed Program/Data Mode

This mode allows the user to send control words to the device along with the DAC data. This permits adaptive control of the device whereby control of the input/output gains can be effected by interleaving control words along with the normal flow of DAC data. The standard data frame remains 16 bits, but now the MSB is used as a flag bit to indicate whether the remaining 15 bits of the frame represent DAC data or control information. In the case of DAC data, the 15 bits are loaded with MSB justification and LSB set to 0 to the DAC register. Mixed mode is enabled by setting the MM bit (CRA:1) to 1 and the DATA/PGM bit (CRA:0) to 1. In the case where control setting changes will be required during normal operation, this mode allows the ability to load both control and data information with the slight inconvenience of formatting the data. Note that the output samples from the ADC will also have the MSB set to zero to indicate it is a data word.

A description of a single device operating in mixed mode is detailed in Appendix B, while Appendix D details the initialization and operation of a dual codec cascade operating in mixed mode. Note that it is not essential to load the control registers in Program Mode before setting mixed mode active. It is also possible to initiate mixed mode by programming CRA with the first control word and then interleaving control words with DAC data.

Digital Loop-Back

This mode can be used for diagnostic purposes and allows the user to feed the ADC samples from the ADC register directly to the DAC register. This forms a loop-back of the analog input to the analog output by reconstructing the encoded signal using the decoder channel. The serial interface will continue to work, which allows the user to control gain settings, etc. Only when DLB is enabled with mixed mode operation can the user disable the DLB, otherwise the device must be reset.

SPORT Loop-Back

This mode allows the user to verify the DSP interfacing and connection by writing words to the SPORT of the devices and have them returned back unchanged after a delay of 16 SCLK cycles. The frame sync and data word that are sent to the Prelim B 11/97

device are returned via the output port. Again, SLB mode can only be disabled when used in conjunction with mixed mode, otherwise the device must be reset.

Analog Loop-Back

In Analog Loop-Back mode, the differential DAC output is connected, via a loopback switch, to the ADC input. This mode allows the ADC channel to check functionality of the DAC channel as the reconstructed output signal can be monitored using the ADC as a sampler. Analog Loop-Back is enabled by setting the ALB bit (CRF:7)

NOTE: Analog Loop-Back can only be enabled if the Analog Gain Tap is powered-down (CRC:1 = 0).

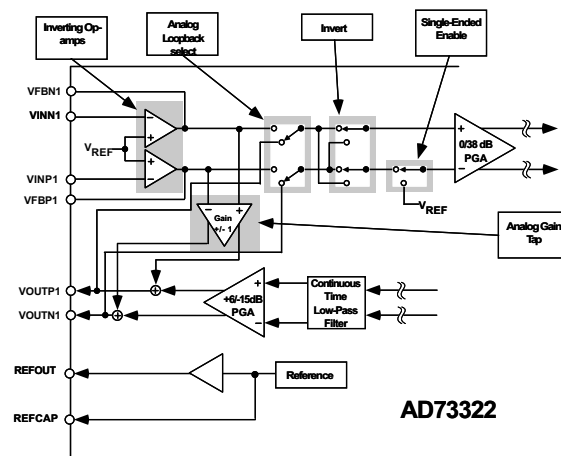


Figure 11. Analog Loop-Back Connectivity

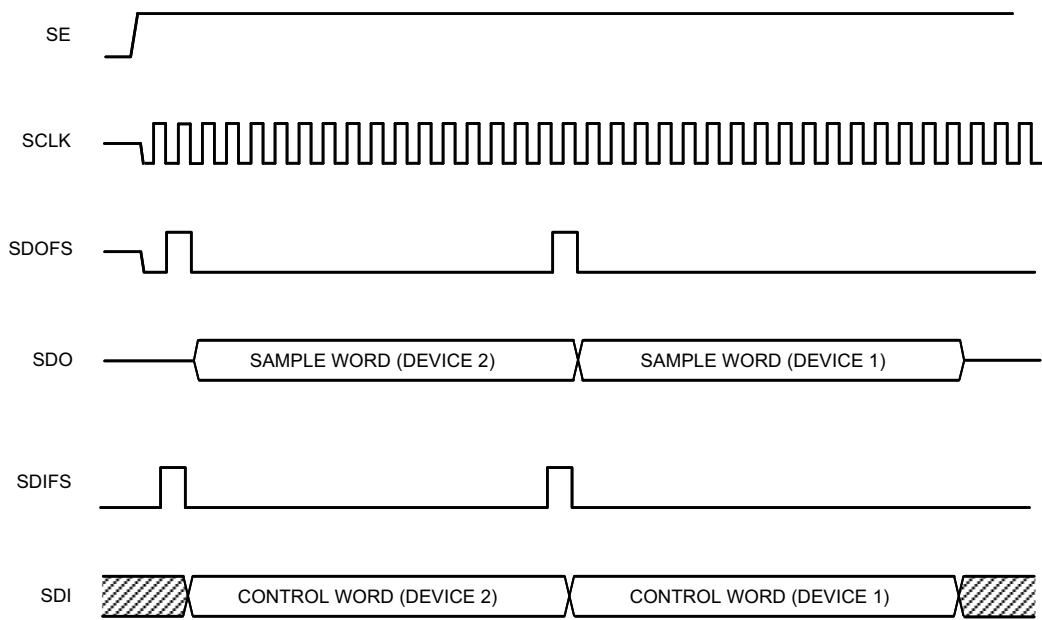


Figure 12. Interface Signal Timing for Control Mode Operation

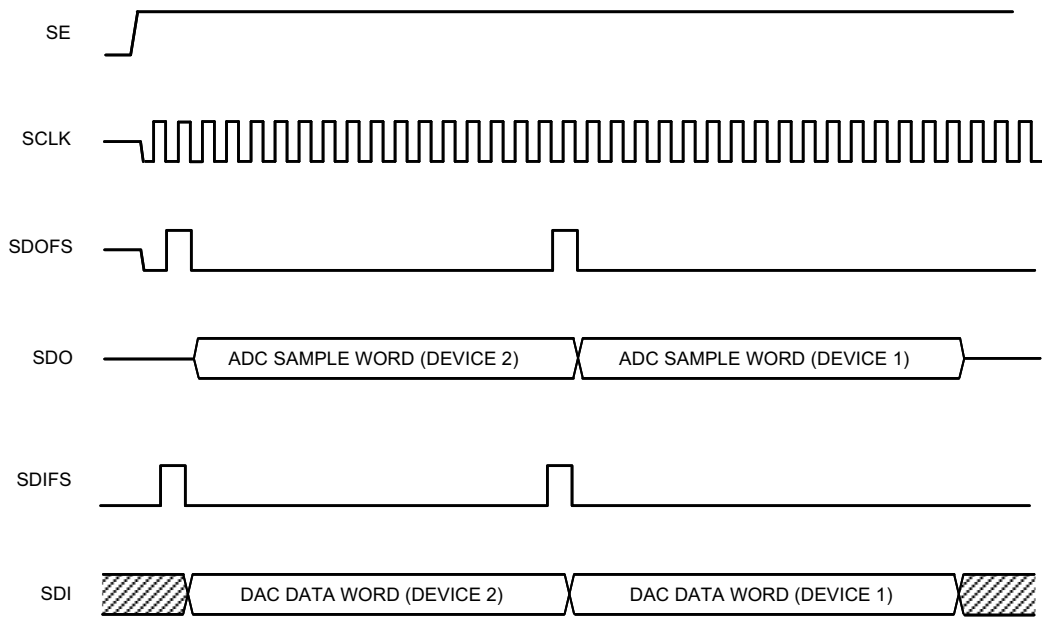


Figure 13. Interface Signal Timing for Data Mode Operation

INTERFACING

The AD73322 can be interfaced to most modern DSP engines using conventional serial port connections and an extra enable control line. Both serial input and output data use an accompanying frame synchronization signal which is active high one clock cycle before the start of the 16-bit word or during the last bit of the previous word if transmission is continuous. The serial clock (SCLK) is an output from the codec and is used to define the serial transfer rate to the DSP's Tx and Rx ports. Two primary configurations can be used: the first is shown in Figure 14 where the DSP's Tx data, Tx frame sync, Rx data and Rx frame sync are connected to the codec's SDI, SDIFS, SDO and SDOFS respectively. This configuration, referred to as indirectly coupled or non frame sync loop-back, has the effect of decoupling the transmission of input data from the receipt of output data. The delay between receipt of codec output data and transmission of input data for the codec is determined by the DSP's software latency. When programming the DSP serial port for this con-

figuration, it is necessary to set the Rx FS as an input and the Tx FS as an output generated by the DSP. This configuration is most useful when operating in mixed mode, as the DSP has the ability to decide how many words (either DAC or control) can be sent to the codec(s). This means that full control can be implemented over the device configuration as well as updating the DAC in a given sample interval. The second configuration (shown in Figure 15) has the DSP's Tx data and Rx data connected to the codec's SDI and SDO, respectively while the DSP's Tx and Rx frame syncs are connected to the codec's SDIFS and SDOFS. In this configuration, referred to as directly coupled or frame sync loop-back, the frame sync signals are connected together and the input data to the codec is forced to be synchronous with the output data from the codec. The DSP must be programmed so that both the Tx FS and Rx FS are inputs as the codec SDOFS will be input to both. This configuration guarantees that input and output events occur simultaneously and is the simplest configuration for operation in normal Data Mode. Note that when programming the DSP in this configuration it is advisable to preload the Tx register with the first control word to be sent before the codec is taken out of reset. This ensures that this word will be transmitted to coincide with the first output word from the device(s).

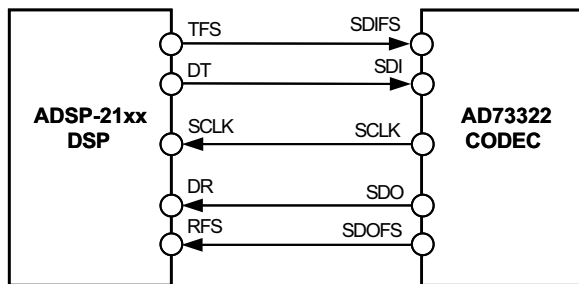


Figure 14. Indirectly Coupled or Non Frame Sync Loop-Back Configuration

Cascade Operation

The AD73322 has been designed to support up to eight codecs in a cascade connected to a single serial port, see Figure 31. The SPORT interface protocol has been designed so that device addressing is built into the packet of information sent to the device. This allows the cascade to be formed with no extra

hardware overhead for control signals or addressing. A cascade can be formed in either of the two modes previously discussed.

There may be some restrictions in cascade operation due to the number of devices configured in the cascade and the serial clock rate chosen. Table XXI details the requirements for SCLK rate for cascade lengths from 1 to 8 devices. This assumes a directly coupled frame sync arrangement as shown in Figure 15.

Table XXI. Cascade Options

| SCLK | Number of Codec Units* in Cascade | | | | | | | |
|---------|-----------------------------------|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| DMCLK | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| DMCLK/2 | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ |
| DMCLK/4 | ✓ | ✓ | ✓ | ✓ | X | X | X | X |
| DMCLK/8 | ✓ | ✓ | X | X | X | X | X | X |

*The AD73322 contains two (2) codec units

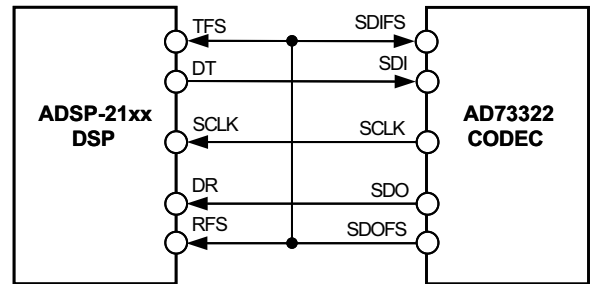


Figure 15. Directly Coupled or Frame Sync Loop-Back Configuration

When using the indirectly coupled frame sync configuration in cascaded operation it is necessary to be aware of the restrictions in sending data to all devices in the cascade. Effectively the time allowed is given by the sampling interval (256/DMCLK) which is 15.625 μs for a sample rate of 64 kHz. In this interval, the DSP must transfer $N \times 16$ bits of information where N is the number of devices in the cascade. Each bit will take 1/SCLK and, allowing for any latency between the receipt of the RX interrupt and the transmission of the TX data, the relationship for successful operation is given by:

$$256/DMCLK > ((N/SCLK) + T_{INTERRUPT\ LATENCY})$$

The interrupt latency will include the time between the ADC sampling event and the RX interrupt being generated in the DSP—this should be 16 SCLK cycles.

In Cascade Mode, each device must know the number of devices in the cascade because the Data and Mixed modes use a method of counting input frame sync pulses to decide when they should update the DAC register from the serial input register. Control Register A contains a 3-bit field (DC0–2) that is pro-programmed by the DSP during the programming phase. The default condition is that the field contains 000b, which is equivalent to a single device in cascade (see Table XVII). However, for cascade operation this field must contain a binary value that is one less than the number of devices in the cascade.

Table XVII. Device Count Settings

| DC2 | DC1 | DC0 | Cascade Length |
|------------|------------|------------|-----------------------|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |