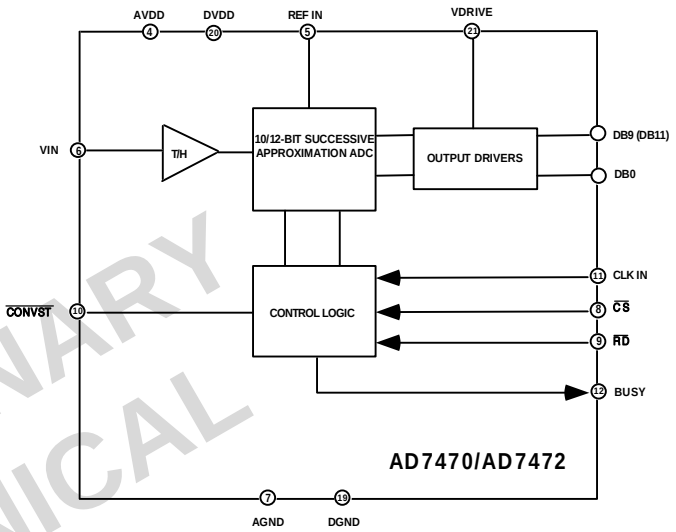
1.75MSPS, 4mW 10-Bit/12-Bit Parallel ADC

Preliminary Technical Data — AD7470/72

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
1.75MSPS for AD7470 (10-Bit)
1.5MSPS for AD7472 (12-Bit)
Low Power:
AD7470:- 3mW typ at 1.75MSPS with 3V Supplies
9mW typ at 1.75MSPS with 5V Supplies
AD7472:- tbdmW typ at 1.5MSPS with 3V Supplies
tbdmW typ at 1.5MSPS with 5V Supplies
Wide Input Bandwidth:
68dB SNR at 500kHz Input Frequency
Flexible Power/Throughput Rate Management
No Pipeline Delays
High Speed Parallel Interface
Sleep Mode: 500nA typ.
24-Pin SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



AD7470 is a 10 Bit part with DB0 to DB9 as outputs
AD7472 is a 12 Bit part with DB0 to DB11 as outputs

GENERAL DESCRIPTION

The AD7470/AD7472 are 10-bit /12-bit high speed, low power, successive-approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5MSPS for the 12-bit AD7472 and up to 1.75MSPS for the 10-bit AD7470. The parts contain a low-noise, wide bandwidth track/hold amplifier which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The BUSY goes high at the start of conversion and goes low 540ns later (AD7472 with a clock frequency of 26MHz) to indicate that the conversion is complete. There are no pipelined delays associated with the part. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7470/AD7472 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and 1.75MSPS throughput rate, the parts consume typically just 1mA. With 5V supplies and 1.75MSPS, the current consumption is typically 1.8mA. The part also offers flexible power/throughput rate management. Operating the part with 3V supplies and 500ksps throughput reduces the current consumption to 0.5mA. At 5V supplies and 500ksps, the part consumes 0.8mA.

It is also possible to operate the parts in an auto sleep mode, where the part wakes up to do a conversion and automatically enters sleep mode at the end of conversion. Using this method allows very low power dissipation numbers at lower throughput rates. In this mode, the AD7472 can be operated with 3V supplies at 100ksps, and consume an average current of just 119uA. At 5V supplies and 100ksps, the average current consumption is 216uA.

The analog input range for the part is 0 to REF IN. The +2.5V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption. The AD7470 offers 1.75MSPS throughput and the AD7472 offers 1.5MSPS throughput rates with 3mW power consumption.
2. Flexible Power/Throughput Rate Management
   The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an auto sleep mode to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay.
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

REV. PrE 03/99

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AD7470–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]		Units	Test Conditions/Comments
DYNAMIC PERFORMANCE	**5V**	**3V**		
Signal to Noise + Distortion (SINAD)	58	tbd	dB min	f_{IN} =500KHz Sine Wave, f_S = 1.75Msps
	tbd	tbd		f_{IN} =100KHz Sine Wave, f_s= 1.75Msps
Signal to Noise Ratio (SNR)	59	tbd	dB min	f_{IN} =500KHz Sine Wave, f_S = 1.75Msps
	tbd	tbd		f_{IN} =100KHz Sine Wave, f_s= 1.75Msps
Total Harmonic Distortion (THD)	–70	tbd	dB max	f_{IN} =500KHz Sine Wave, f_S = 1.75Msps
	tbd	tbd		f_{IN} =100KHz Sine Wave, f_s= 1.75Msps
Peak Harmonic or Spurious Noise (SFDR)	–70	tbd	dB max	f_{IN} =500KHz Sine Wave, f_S = 1.75Msps
	tbd	tbd		f_{IN} =100KHz Sine Wave, f_s= 1.75Msps
Intermodulation Distortion (IMD)				
Second Order Terms	–75	tbd	dB typ	
Third Order Terms	–75	tbd	dB typ	
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	20	tbd	MHz typ	
DC ACCURACY				
Resolution	10	tbd	Bits	
Integral Nonlinearity	±1	tbd	LSB max	
Differential Nonlinearity	±0.9	tbd	LSB max	Guaranteed No Missed Codes to 10 Bits.
Offset Error	±1	tbd	LSB max	
Gain Error	±1	tbd	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	*[4]	Volts	
dc Leakage Current	±1	*	µA max	
Input Capacitance	20	*	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	*	V	± -1% for Specified Performance
dc Leakage Current	±1	*	µA max	
Input Capacitance	20	*	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.8	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	*	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	*	V max	I_{SINK} =200uA
Floating-State Leakage Current	±10	*	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	*	pF max	
Output Coding	Straight(Natural) Binary			
CONVERSION RATE				
Conversion Time	12	*	CLK IN cycles	428ns with CLK IN at 28MHz
Track/Hold Acquisition Time	130	140	ns max	
Throughput Rate	1.75	1.5	MSPS max	Conversion Time + Acquisition Time. CLK IN at 28MHz

AD7470–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 28 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
I_{DD}[3]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	2.43	mA max	V_{DD} = 4.75V to 5.25V. f_S=1.75MSPS Typically 1.8mA.
Quiescent Current	0.85	mA	V_{DD} = 4.75V to 5.25V. f_S=1.75MSPS
Normal Mode	1.33	mA max	V_{DD} = 2.7V to 3.3V. f_S=1.75MSPS Typically 1mA.
Quiescent Current	tbd	mA	V_{DD} = 2.7V to 3.3V. f_S=1.75MSPS
Sleep Mode	1	µA max	CLK IN =0V or DV_{DD}
Power Dissipation[3]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	11	mW max	V_{DD} = 5V.
	4	mW max	V_{DD} = 3V
Sleep Mode	5	uW max	V_{DD} = 5V. CLK IN =0V or DV_{DD}
	3	µW max	V_{DD} = 3V. CLK IN =0V or DV_{DD}

NOTES
[1] Temperature ranges as follows: A Version: –40°C to +85°C.
[2] Sample tested @ +25°C to ensure compliance.
[3] See POWER VERSUS THROUGHPUT RATE section.
[4] Specifications for 3V and 5V are the same.

Specifications subject to change without notice.

AD7472–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 26 MHz @ 5V and 20 MHz @ 3V unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]		B Version[1]		Units	Test Conditions/Comments
DYNAMIC PERFORMANCE	**5V**	**3V**	**5V**	**3V**		fs=1.5Msps @ 5V, fs=1.2Msps @ 3V
Signal to Noise + Distortion (SINAD)	68	67	68	68	dB min	f_{IN} =500kHz Sine Wave
	69	68	69	68		f_{IN} =100KHz Sine Wave
Signal to Noise Ratio (SNR)	68	67	68	67	dB min	f_{IN} =500kHz Sine Wave
	69	68	69	68		f_{IN} =100KHz Sine Wave
Total Harmonic Distortion (THD)	–80	-75	-80	-75	dB max	f_{IN} =500kHz Sine Wave
	-80	-78	-80	-78		f_{IN} =100KHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–76	tbd	-76	tbd	dB max	f_{IN} =500kHz Sine Wave
						f_{IN} =100KHz Sine Wave
Intermodulation Distortion (IMD)						
Second Order Terms	–78	tbd	-78	tbd	dB typ	
Third Order Terms	–78	tbd	-78	tbd	dB typ	
Aperture Delay	5	5	5	5	ns typ	
Aperture Jitter	15	15	15	15	ps typ	
Full Power Bandwidth	20	tbd	20	tbd	MHz typ	
DC ACCURACY						fs=1.5Msps @ 5V, fs=1.2Msps @ 3V
Resolution	12	*[4]	12	*	Bits	
Integral Nonlinearity	±1.5	tbd	±1	tbd	LSB max	
Differential Nonlinearity	±0.9	tbd	±0.9	tbd	LSB max	Guaranteed No Missed Codes to 12 Bits.
Offset Error	±3	tbd	±3	tbd	LSB max	
Gain Error	±3	tbd	±3	tbd	LSB max	
ANALOG INPUT						
Input Voltage Ranges	0 to REF IN	*	0 to REF IN	*	Volts	
dc Leakage Current	±1	*	±1	*	µA max	
Input Capacitance	20	*	20	*	pF typ	
REFERENCE INPUT						
REF IN Input Voltage Range	2.5	*	2.5	*	V	± -1% for Specified Performance
dc Leakage Current	±1	*	±1	*	µA max	
Input Capacitance	20	*	20	*	pF typ	
LOGIC INPUTS					Volts	
Input High Voltage, V_{INH}	2.8	2.4	2.8	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[2]	10	10	10	10	pF max	
LOGIC OUTPUTS						
Output High Voltage, V_{OH}	V_{DRIVE} - 0.2	*	V_{DRIVE} - 0.2	*	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	*	0.4	*	V max	I_{SINK} =200uA
Floating-State Leakage Current	±10	*	±10	*	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	*	10	*	pF max	
Output Coding	Straight (Natural) Binary		Straight (Natural) Binary			
CONVERSION RATE						
Conversion Time	14	*	14	*	CLKIN cycles	540ns with CLK IN at 26MHz
Track/Hold Acquisition Time	130	140	130	140	ns max	
Throughput Rate	1.5	1.2	1.5	1.2	MSPS max	Conversion Time + Acquisition Time. CLK IN of 26MHz @ 5V and 20MHz @ 3V

AD7472–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 26 MHz @5V and 20 MHz @ 3V unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}[3]				Digital I/Ps = 0V or DV_{DD}
Normal Mode	2.43	2.43	mA max	V_{DD} = 4.75V to 5.25V. f_S=1.5MSPS Typically 1.8mA.
Quiescent Current	0.85	0.85	mA max	V_{DD} = 4.75V to 5.25V. f_S=1.5MSPS
Normal Mode	1.33	1.33	mA max	V_{DD} = 2.7V to 3.3V. f_S=1.2MSPS Typically 1mA.
Quiescent Current	tbd	tbd	mA	V_{DD} = 2.7V to 3.3V. f_S=1.2MSPS
Shutdown Mode	1	1	uA max	CLK IN =0V or DV_{DD}
Power Dissipation[3]				Digital I/Ps = 0V or DV_{DD}
Normal Mode	11	11	mW max	V_{DD} = 5V.
	4	4	mW max	V_{DD} = 3V
Shutdown Mode	5	5	uW max	V_{DD} = 5V. CLK IN =0V or DV_{DD}
	3	3	uW max	V_{DD} = 3V. CLK IN =0V or DV_{DD}

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2] Sample tested @ +25°C to ensure compliance.
[3] See POWER VERSUS THROUGHPUT RATE section.
[4] Specifications for 3V and 5V are the same.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7470	AD7472	Units	Description
f_{CLK}[2]	10	10	kHz min	
	28	26	MHz max	
$t_{CONVERT}$	12* t_{CLK}	14* t_{CLK}		t_{CLK}= 1/$f_{CLK\ IN}$
	428	540	ns max	
t_{WAKEUP}	1	1	us max	Wakeup Time
t_1	15	15	ns min	$\overline{CONVST}$ Pulse Width
t_2	10	10	ns min	$\overline{CONVST}$ to BUSY Delay
t_3	0	0	ns max	BUSY to $\overline{CS}$ Setup Time
t_4[3]	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	30	30	ns min	$\overline{RD}$ Pulse Width
t_6[3]	25	25	ns min	Data Access Time After Falling Edge of $\overline{RD}$
t_7[4]	5	5	ns min	Bus Relinquish Time After Rising Edge of $\overline{RD}$
t_8	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	130	130	ns min	Acquisition Time @ Vdd = 5V
	140	140	ns min	Acquisition Time @ Vdd = 3V
t_{10}	100	100	ns min	Quiet Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the CLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_7 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

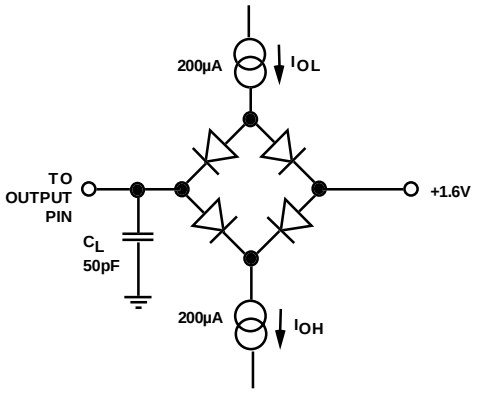


Figure 2. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS`1
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND/DGND ..... -0.3V to +7V
DV_{DD} to AGND/DGND ..... -0.3V to +7V
V_{DRIVE} to AGND/DGND ..... -0.3V to +7V
AV_{DD} to DV_{DD} ..... -0.3V to +0.3V
V_{DRIVE} to DV_{DD} ..... -0.3V to DVDD+0.3V
AGND TO DGND ..... -0.3V to +0.3V
Analog Input Voltage to AGND .. -0.3V to AVDD+0.3V
Digital Input Voltage to DGND .. -0.3V to DVDD+0.3V
REF IN to AGND ..... -0.3V to AVDD+0.3V
Input Current to Any Pin Except Supplies[2] ..... ±10mA
Operating Temperature Range
Commercial (A and B Version) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C

SOIC, TSSOP Package Dissipation ..... +450mW
θ_{JA} Thermal Impedance ..... 75°C/W (SOIC)
..... 115°C/W (TSSOP)
θ_{JC} Thermal Impedance ..... 25°C/W (SOIC)
..... 35°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Resolution (Bits)	Package Option[1]	Branding
AD7470ARU	-40°C to +85°C	10	RU-24	
AD7472AR	-40°C to +85°C	12	R-24	
AD7472BR	-40°C to +85°C	12	R-24	
AD7472ARU	-40°C to +85°C	12	RU-24	
EVAL-AD7470CB[2]	Evaluation Board			
EVAL-AD7472CB[2]	Evaluation Board			
EVAL-CONTROL BOARD[3]	Controller Board			

NOTES
[1]R = SOIC; RU = TSSOP.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/ demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the XX0000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Fig 3. AD7470 PIN CONFIGURATION

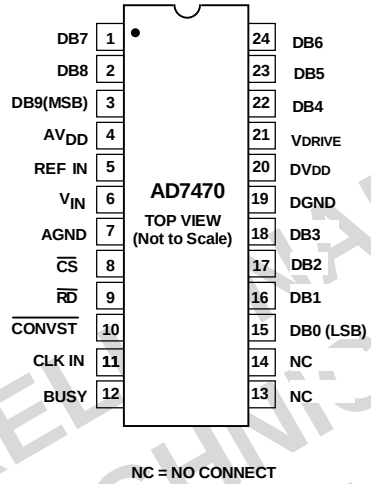
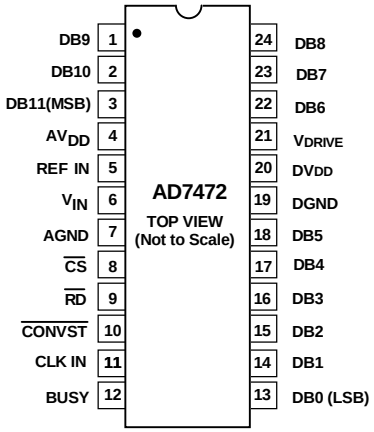


Fig 4. AD7472 PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ can be hardwired permanently low.
$\overline{RD}$	Read Input. Logic Input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to same AND gate on the input so the signals are interchangeable. $\overline{CS}$ and $\overline{RD}$ can be hardwired permanently low in which case, the data bus is always active and the result of the new conversion is clocked out subsequent to the BUSY line going low.
$\overline{CONVST}$	Conversion Start Input. Logic Input used to initiate conversion. The input track/hold amplifier goes from track mode to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initiated at this point. The conversion input can be as narrow as 15ns. If the $\overline{CONVST}$ input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter sleep mode. If the part enters this sleep mode, the next rising edge of $\overline{CONVST}$ wakes the part up. Wake-up time for the part is typically 1µs.
CLK IN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7472 takes 14 clock cycles while conversion time for the AD7470 takes 12 clock cycles. The frequency of this master clock input, therefore, determines the conversion time and achievable throughput rate. While the ADC is not converting the Clock-In pad is in three-state and thus no clock is going through the part.
BUSY	BUSY Output. Logic Output indicating the status of the conversion process. The BUSY signal goes high after the falling edge of $\overline{CONVST}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low. If the $\overline{CONVST}$ input is still low when BUSY goes low, the part automatically enters its sleep mode on the falling edge of BUSY.
REF IN	Reference Input. An external reference must be applied to this input. The voltage range for the external reference is 2.5V ±1% for specified performance.
AV_{DD}	Analog Supply Voltage, +2.7V to +5.25V. This is the only supply voltage for all analog circuitry on the AD7470/72. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to AGND.
DV_{DD}	Digital Supply Voltage, +2.7V to +5.25V. This is the supply voltage for all digital circuitry on the AD7470/72 apart from the output drivers. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to DGND.
AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7470/72. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis.
DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7470 and AD7472. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0V to REFIN. The analog input presents a high dc input impedance.
V_{DRIVE}	Supply Voltage for the Output Drivers, +2.7V to +5.25V. This voltage determines the output high voltage for the data output pins. It allows the AVDD and DVDD to operate at 5V (and maximize the dynamic performance of the ADC) while the digital outputs can interface to 3V logic.
DB0-DB9/11	Data Bit 0 to Data Bit 9 (AD7470) and DB11 (AD7472). Parallel digital outputs which provide the conversion result for the part. These are three-state outputs which are controlled by $\overline{CS}$ and $\overline{RD}$. The output high voltage level for these outputs is determined by the V_{DRIVE} input.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Gain Error
The last transition should occur at the analog value 1 1/2 LSB below the nominal full scale. The first transition is a 1/2 LSB above the low end of the scale (zero in the case of AD7470/74). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (f_S/2), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise + Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter is 62dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7470/72, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to f_S/2 and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7470/72 are tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
In a sample/hold, the time required after the hold command for the switch to open fully is the aperture delay. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter
Aperture jitter is the range of variation in the aperture delay. In other words, it is the uncertainty about when the sample is taken. Jitter is the result of noise which modulates the phase of the hold command. This specification establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution. This error will increase as the input dV/dt increases.

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7470/72 is a 10-bit/12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The AD7470/72 can convert analog input signals in the range 0V to Vref. Figure 5 shows a very simplified schematic of the ADC. The Control Logic, SAR and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor so as to bring the comparators back into a balanced condition.

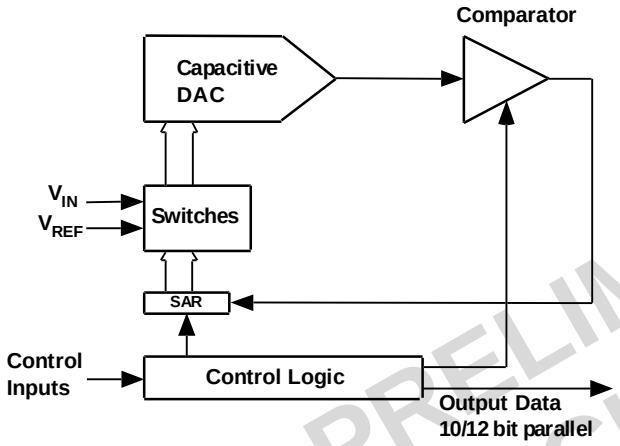


Figure 5. Simplified block diagram of AD7470/72

Figure 6 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on VIN.

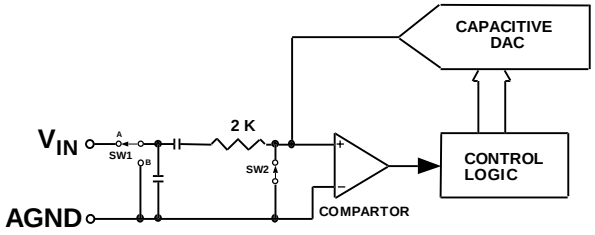


Figure 6. ADC Acquisition Phase

Figure 7 shows the ADC during conversion. When conversion starts SW2 will open and SW1 will move to position B, causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced the conversion result is available in the SAR register.

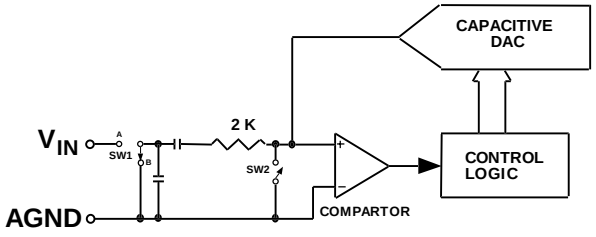


Fig. 7 ADC Conversion Phase

TYPICAL CONNECTION DIAGRAM

Figure 8 shows a typical connection diagram for the AD7470/72. Conversion is initiated by a falling edge on $\overline{\text{CONVST}}$. Once $\overline{\text{CONVST}}$ goes low the BUSY signal goes high, and at the end of conversion the falling edge of BUSY is used to activate an Interrupt Service Routine. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ lines are then activated in parallel to read the 10 or 12 data bits. The recommended REF IN voltage is 2.5V providing an analog input range of 0V to 2.5V, making the AD7470/72 an unipolar A/D. It is recommended to perform a dummy conversion after power-up as the first conversion result could be incorrect. The $\overline{\text{CONVST}}$ pin should not be floating when power is applied as a rising edge on $\overline{\text{CONVST}}$ might not wake up the part.

In Figure 8 the V_{DRIVE} pin is tied to DV_{DD} which results in logic output voltage values being either 0V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5V supply and V_{DRIVE} by a 3V supply then the logic output voltage levels would be either 0V or 3V. This feature allows the AD7470/72 to interface to 3V parts while still enabling the A/D to process signals at 5V supply.

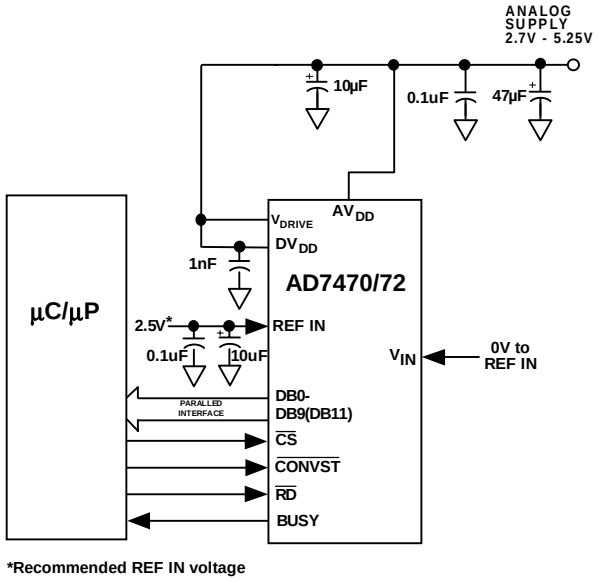


Figure 8. Typical Connection Diagram

ADC TRANSFER FUNCTION

The output coding of the AD7470/72 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, etc.). The LSB size is = (REF IN)/4096 for the AD7472 and (REF IN)/1024 for the AD7470. The ideal transfer characteristic for the AD7472 is shown in Fig. 9.

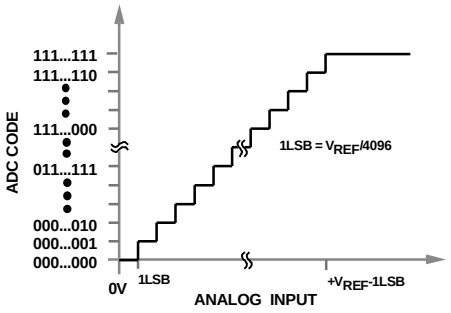


Figure 9. Transfer Characteristic for 12 Bits

AC ACQUISITION TIME

In ac applications it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of impedance at the VIN pin of the ADC will cause the THD to degrade at high input frequencies.

Input Buffers	AD7470/72 Dynamic Performance Specifications				Typ. Current Consumption
	SNR 100KHz	THD 100KHz	SNR 500KHz	THD 500KHz	
AD8047	tbd	tbd	tbd	tbd	5.8 mA
AD9631	tbd	tbd	tbd	tbd	17 mA
AD8051	tbd	tbd	tbd	tbd	4.4 mA
AD797	tbd	tbd	tbd	tbd	8.2 mA

Fig 10. Recommended Input Buffers

Reference Input

The following references are best suited for use with the AD7470/72.

ADR291

AD780

AD192

For optimum performance, a 2.5V reference is recommended. The part can function with a reference up to 3V and down to 2v, but the performance deteriorates.

DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends it on the falling edge of the $\overline{\text{CONVST}}$ signal. At the end of conversion there is a settling time associated with the sampling circuit. This settling time lasts approximately 140ns. The analog signal on V_{IN} is also being acquired during this settling time; therefore, the minimum acquisition time needed is approximately 140ns.

Figure 11 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R3 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal switch resistance, R2 is for bandwidth control and C1 is the sampling capacitor. C2 is back-plate capacitance and switch parasitic capacitance.

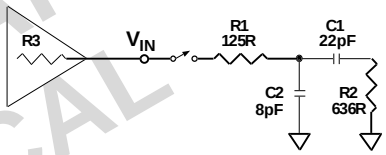


Fig. 11. Equivalent Sampling Circuit

During the acquisition phase the sampling capacitor must be charged to within a 1/2 LSB of its final value.

ANALOG INPUT

Figure 12 shows the equivalent circuit of the analog input structure of the AD7470/72. The two diodes, D1 and D2, provide ESD protection for the analog inputs. The capacitor C3 is typically about 4pF and can be primarily attributed to pin capacitance. The resistor R1 is an internal switch resistance. This resistor is typically about 125R. The capacitor C1 is the sampling capacitor while R2 is used for bandwidth control.

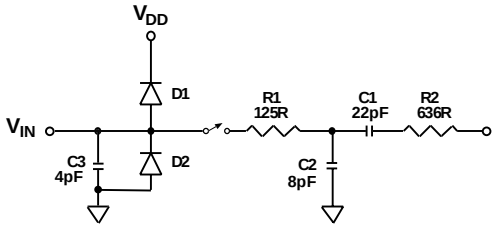


Fig. 12. Equivalent Analog Input Circuit

CLOCK SOURCES

The max CLK specification for the AD7470 is 28MHz and for the AD7472, it is 26MHz. These frequencies are not standard off the shelf oscillator frequencies. Many manufacturers produce oscillator modules close to these frequencies; a typical one being 25.175MHz from IQD Limited. AEL Crystals Limited produce a 25MHz oscillator module in various packages. Crystal oscillator manufacturers will produce 26MHz and 28MHz oscillators to order. Of course any clock source can be used, not just crystal oscillators.

PARALLEL INTERFACE

The parallel interface of the AD7470 and AD7472 is 10-bits and 12-bits wide respectively. The output data buffers are activated when both $\overline{CS}$ and $\overline{RD}$ are logic low. At this point the contents of the data register are placed onto the data bus. Figure 13 shows the timing diagram for the parallel port.

Figure 14 shows the timing diagram for the parallel port when CS and RD are tied permanently low. In this setup, once the BUSY line goes from high to low the conversion process is completed. The data is available on the output bus on the falling edge of BUSY.

It is important to point out that data bus cannot change state while the A/D is doing a conversion as this would have a detrimental effect on the conversion in progress. The data out lines will go three-state again when either the $\overline{RD}$ or $\overline{CS}$ line goes high. Thus the $\overline{CS}$ can be tied low permanently, leaving the $\overline{RD}$ line to control conversion result access. Please reference the V_{DRIVE} section for output voltage levels.

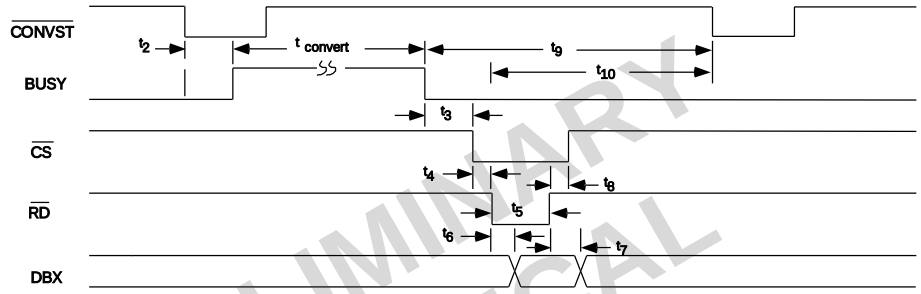


Figure 13. Parallel Port Timing

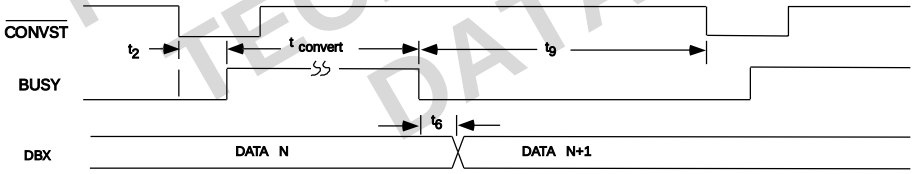


Figure 14. Parallel Port Timing With $\overline{CS}$ & $\overline{RD}$ Tied Low

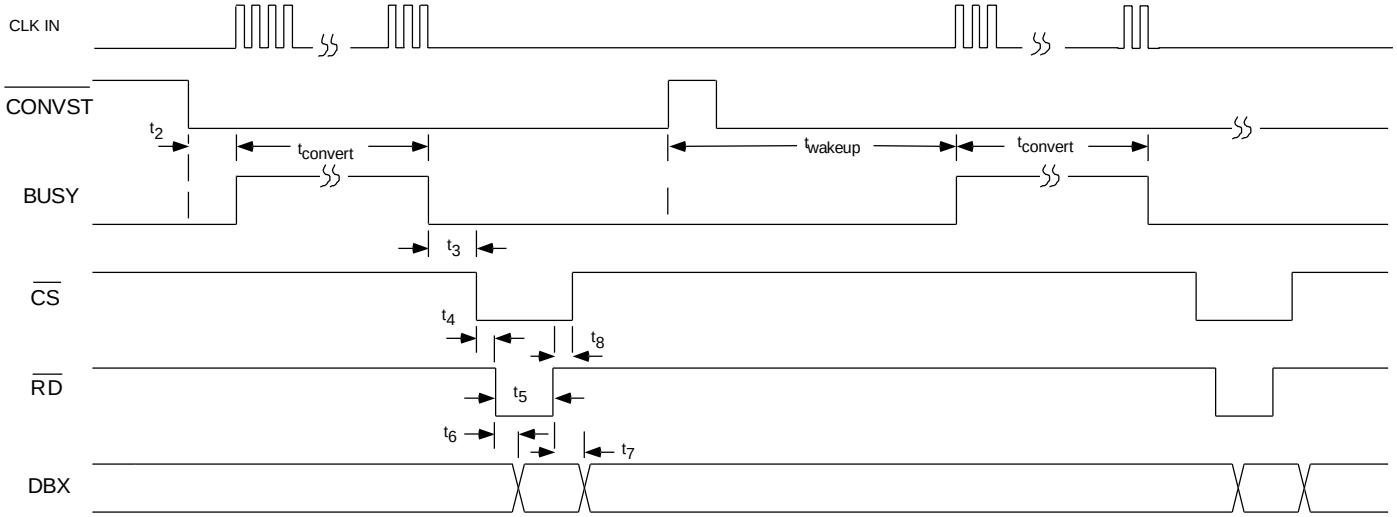


Figure 15. AD7470/AD7472 Wake-Up Timing Diagram (Burst Clock)

OPERATING MODES

The AD7470 and AD7472 have two possible modes of operation depending on the state of the $\overline{\text{CONVST}}$ pulse at the end of a conversion, Mode 1 and Mode 2. There is a continuous clock on the CLK IN pin.

Mode 1 (High Speed Sampling)

In this mode of operation the $\overline{\text{CONVST}}$ pulse is brought high before the end of conversion i.e. before the BUSY goes low, see Figure 13. If the $\overline{\text{CONVST}}$ pin is brought from high to low while BUSY is high then the conversion is restarted again. When operating in this mode a new conversion should not be initiated until 140ns after $\overline{\text{BUSY}}$ goes low. This acquisition time allows the track/hold circuit to accurately acquire the input signal. As mentioned earlier, a read should not be done during a conversion. This mode facilitates the fastest throughput times for the AD7470/72.

Mode 2 (Sleep Mode)

Figure 16 shows AD7470/72 in mode 2 operation where the ADC goes into sleep mode after conversion. The $\overline{\text{CONVST}}$ line is brought low to initiate a conversion and remains low until after the end of conversion. If $\overline{\text{CONVST}}$ goes high and low again while BUSY is high then the conversion is restarted again. Once the BUSY line goes from a high to a low, the $\overline{\text{CONVST}}$ line has its status checked and, if low, the part enters sleep-mode.

The device wakes up again on the rising edge of the $\overline{\text{CONVST}}$ signal. There is a wakeup time of typically 1us after the rising edge of $\overline{\text{CONVST}}$ before the BUSY line can go high to indicate start of conversion. BUSY will only go high once $\overline{\text{CONVST}}$ goes low. The $\overline{\text{CONVST}}$ line can go from a high to a low during this wakeup time and a conversion will still be initiated after 1us. Superior power performance can be achieved in this mode of operation by waking up the AD7470 and AD7472 only to carry out a conversion.

Burst mode

Burst mode on the AD7470/72 is a subsection of Mode 1 & 2, the clock is noncontinuous. Figure 15 shows how the ADC works in burst mode for Mode 2. The clock needs only to be switched on during conversion, min of 12 clock cycles for the AD7470 and 14 clock cycles for the AD7472. As the clock is off during non-converting intervals, system power is saved. The BUSY signal can be used to gate the CLK IN pulses. The ADC doesn't begin the conversion process until the first CLK IN rising edge after BUSY goes high. The clock needs to start less than 2 clock cycles away from the $\overline{\text{CONVST}}$ active edge otherwise INL deteriorates e.g. if the clock frequency is 28MHz then the clock must start within 71.4ns of $\overline{\text{CONVST}}$ going low. In Figure 15 the A-D converter section is put into sleep mode once conversion is completed and on the rising edge of $\overline{\text{CONVST}}$ it is woken up again; the user must be wary of the wakeup time as this will reduce the sampling rate of the ADC.

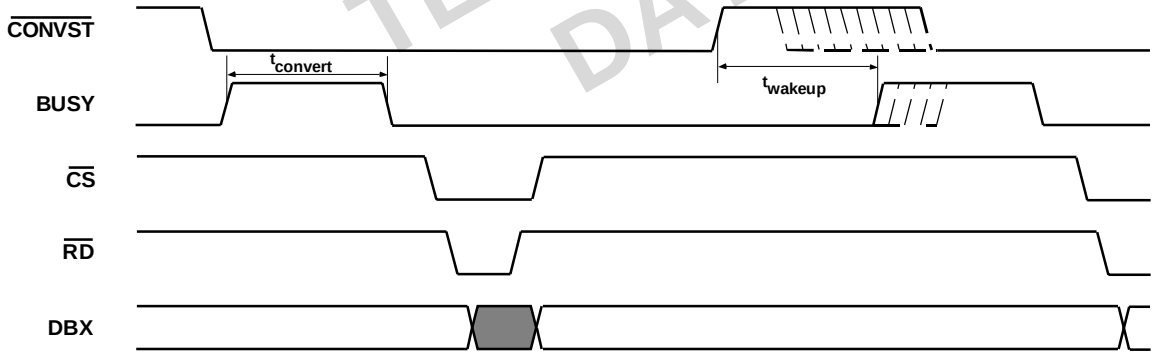


Fig. 16. Mode 2 Operation

VDRIVE

The V_{DRIVE} pin is used as the voltage supply to the output drivers and is a separate supply from AVDD and DVDD. The purpose to using a separate supply for the output drivers is that the user can vary the output high voltage, V_{OH}, from the VDD supply to the AD7470/72. For example, if AVDD and DVDD is using a 5V supply, the V_{DRIVE} pin can be powered off a 3V supply. The ADC has better dynamic performance at 5V than at 3V, so operating the part at 5V while still being able to interface to 3V parts, pushes the AD7470/72 to the top bracket of high performance 10/12 bit A/D's. Of course, the ADC can have its V_{DRIVE} and DVDD pins connected together and be powered from a 3V or 5V supply.

All outputs are powered off V_{DRIVE}. These are all the data out pins and the BUSY pin. The $\overline{\text{CONVST}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$ and CLK IN signals are related to the DVDD voltage.

POWER-UP

It is recommended that the user performs a dummy conversion after power up, as the first conversion result could be incorrect. The recommended power-up sequence is as follows:-

1> Gnd
2> Vdd
3> V_{DRIVE}
4> REF IN
5> Vin
6> Digital Inputs

Power V's throughput

The two modes of operation for the AD7470 and AD7472 will produce different power versus throughput performances, Mode 1 and Mode 2, see Operating Modes section of the data sheet for more detailed descriptions of these modes. Mode 2 is the Sleep Mode of the part and it achieves the optimum power performance.

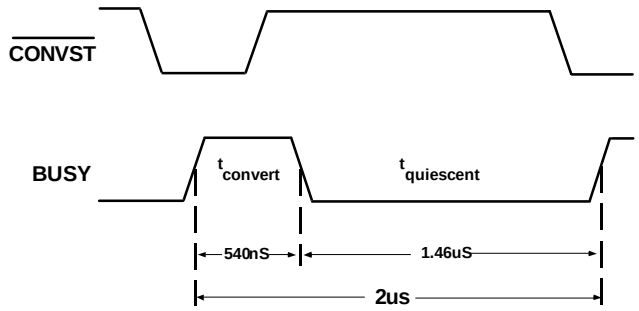


Fig. 17. Mode 1 Power Dissipation

Mode 1

Figure 17 above shows the AD7472 conversion sequence in Mode 1 using a throughput rate of 500Ksps and a clock frequency of 26MHz. At 5V supply the current consumption for the part when converting is 2.43mA and the quiescent current is 0.85mA. The conversion time of 540ns contributes 3.28mW to the overall power dissipation in the following way:-

(540ns/2us)x(5x2.43mA)=3.28mW

The contribution to the total power dissipated by the remaining 1.46us of the cycle is 3.1025mW.

(1.46us/2us)x(5x0.85mA)=3.1025mW

Thus the power dissipated during each cycle is 3.28mW+3.1025mW=6.3825mW

Mode 2

Figure 18 below shows the AD7472 conversion sequence in Mode 2 using a throughput rate of 500Ksps and a clock frequency of 26MHz. At 5V supply the current consumption for the part when converting is 2.43mA, while the sleep current is 1uA. The power dissipated during this power-down is negligible and is thus not worth considering in the total power figure. During the wakeup phase, the AD7472 will draw 0.85 mA. Overall power dissipated is:-

(540ns/2us)x(5x2.43mA)+(1us/2us)x(5x0.85mA)=5.4mW

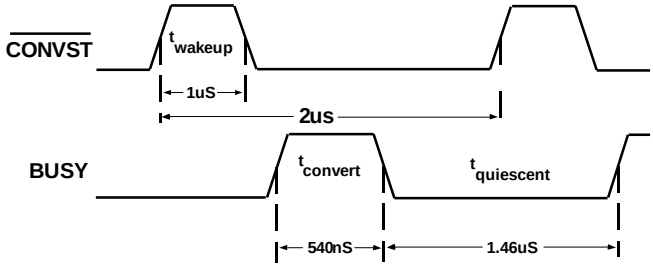


Fig. 18. Mode 2 Power Dissipation

Figure 19 to figure 22 show a graphical representation of power v's throughput for the AD7472 when in (a) 5V in Mode 1 and Mode 2 and (b) 3V in Mode 1 and Mode 2.

Fig. 19. Power vs Throughput (Mode 1 @ 5V)

Fig. 20. Power vs Throughput (Mode 2 @ 5V)

Fig. 21. Power vs Throughput (Mode 1 @ 3V)

Fig. 22. Power vs Throughput (Mode 1 @ 3V)

Fig. 25. SNR vs Temperature

Fig. 23. SNR vs Input Tone

Fig. 26. THD vs Temperature

Fig. 24. THD vs Input Tone

Fig. 27. Power vs CLK Frequency

GROUNDING AND LAYOUT

The analog and digital power supplies are independent and separately pinned out to minimize coupling between analog and digital sections within the device. To complement the excellent noise performance of the AD7470 & AD7472 it is imperative that care be given to the PCB layout. Fig. 28 shows a recommended connection diagram for the AD7470 & AD7472.

All of the AD7470/72 ground pins should be soldered directly to a ground plane to minimize series inductance. The AV_{DD}, DV_{DD} and V_{DRIVE} pins should be decoupled to both the analog and digital ground planes. The large value capacitors will decouple low frequency noise to analog ground, the small value capacitors will decouple high frequency noise to digital ground. All digital circuitry power pins should be decoupled to the digital ground plane. The use of ground planes can physically separate sensitive analog components from the noisy digital system. The two ground planes should **only** be joined in one place and should not overlap so as to minimize capacitive coupling between them. If the AD7470/72 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7470/72.

Noise can be minimized by applying some simple rules to the PCB layout :- analog signals should be kept away from digital signals; fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs; avoid running digital lines under the device as these will couple noise onto the die; the power supply lines to the AD7470/72 should use as large a trace as possible to provide a low impedance path and reduce the effects of glitches on the power supply line; avoid crossover of digital and analog signals and place traces that are on opposite sides of the board at right angles to each other.

Noise to the analog power line can be further reduced by use of multiple decoupling capacitors as shown in Fig. 28. Decoupling capacitors should be placed directly at the power inlet to the PCB and also as close as possible to the power pins of the AD7470/72. The same decoupling method should be used on other ICs on the PCB, with the capacitor leads as short as possible so as to minimize lead inductance.

POWER SUPPLIES

Separate power supplies for AV_{DD} and DV_{DD} are desirable but if necessary DV_{DD} may share its power connection to AV_{DD}. The digital supply(DV_{DD}) must not exceed the analog supply(AV_{DD}) by more than 0.3V in normal operation.

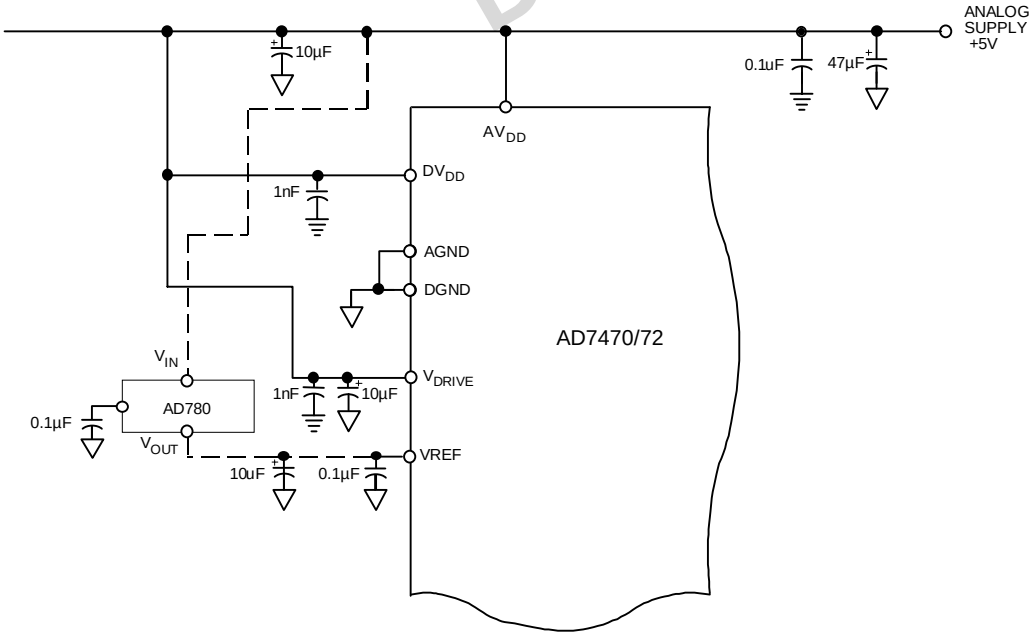


Fig. 28. AD7470/72 Decoupling Circuit

MICROPROCESSOR INTERFACING

AD7470/72 to ADSP-2185 Interface

Figure 29. shows a typical interface between the AD7470/72 and the ADSP-2185. The ADSP-2185 processor can be used in one of two memory modes, Full Memory Mode and Host Mode. The Mode C pin determines which mode the processor works in. The interface in Fig. 29 is set up to have the processor working in Full Memory Mode which allows full external addressing capabilities.

When the AD7470/72 has finished converting the BUSY line requests an interrupt through the $\overline{IRQ2}$ pin. The IRQ2 interrupt has to be set up in the interrupt control register as edge-sensitive. The DMS (Data Memory Select) pin latches in the address of the A/D into the address decoder. The read operation is thus started.

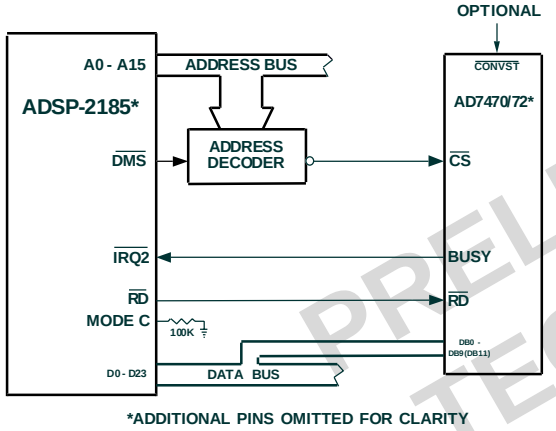


Figure 29. Interfacing to the ADSP-2185

AD7470/72 to ADSP-21065 Interface

Figure 30. shows a typical interface between the AD7470/72 and the ADSP-21065L SHARC processor. This interface is an example of one of three DMA handshake modes. The $\overline{MS}_{\overline{X}}$ control line is actually three memory select lines. Internal $ADDR_{25-24}$ are decoded into $\overline{MS}_{3-0}$, these lines are then asserted as chip selects. The $\overline{DMAR}_1$ (DMA Request 1) is used in this setup as the interrupt to signal end of conversion. The rest of the interface is standard handshaking operation.

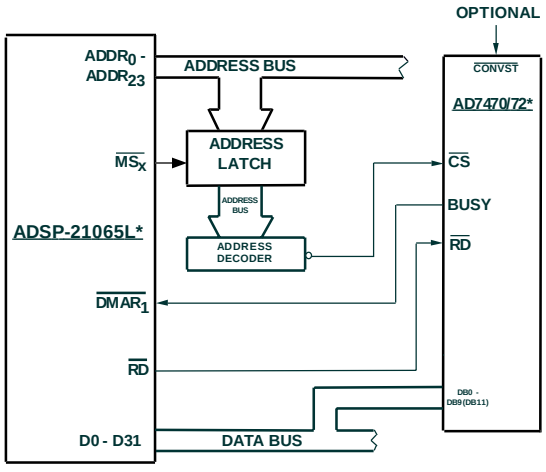


Figure 30. Interfacing to ADSP-21065L

AD7470/72 to TMS320C25 Interface

Figure 31 shows an interface between the AD7470/72 and the TMS320C25. The $\overline{CONVST}$ signal can be applied from the TMS320C25 or from an external source. The BUSY line interrupts the digital signal processor when conversion is completed. The TMS320C25 does not have a separate $\overline{RD}$ output to drive the AD7470/72 $\overline{RD}$ input directly. This has to be generated from the processor STRB and R/$\overline{W}$ outputs with the addition of some glue logic. The $\overline{RD}$ signal is OR-gated with the $\overline{MSC}$ signal to provide the WAIT state required in the read cycle for correct interface timing. The following instruction is used to read the conversion from the AD7470/72:

IN D,ADC

where D is Data Memory address and the ADC is the AD7470/72 address. The read operation must not be attempted during conversion.

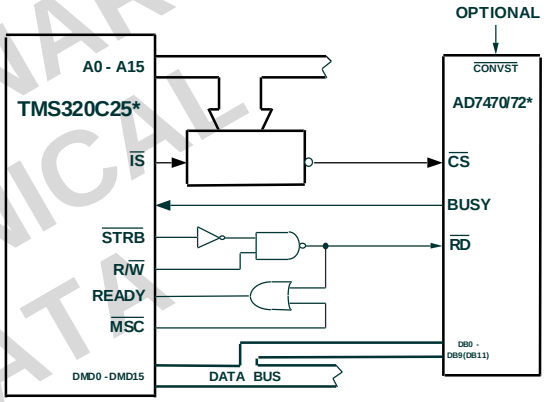


Figure 31. Interfacing to the TMS320C25

AD7470/72 to PIC17C4X Interface

Figure 32 shows a typical parallel interface between the AD7470/72 and PIC17C42/43/44. The microcontroller sees the A/D as another memory device with its own specific memory address on the memory map. The $\overline{CONVST}$ signal can either be controlled by the microcontroller or an external source. The BUSY signal provides an interrupt request to the microcontroller when a conversion ends. The INT pin on the PIC17C42/43/44 must be configured to be active on the negative edge. PORTC & PORTD of the microcontroller are bidirectional and are used to address the AD7470/72 and also to read in the 10 bit (AD7470) or 12 bit (AD7472) data. The OE pin on the PIC can be used to enable the output buffers on the AD7470/72 and preform a read operation.

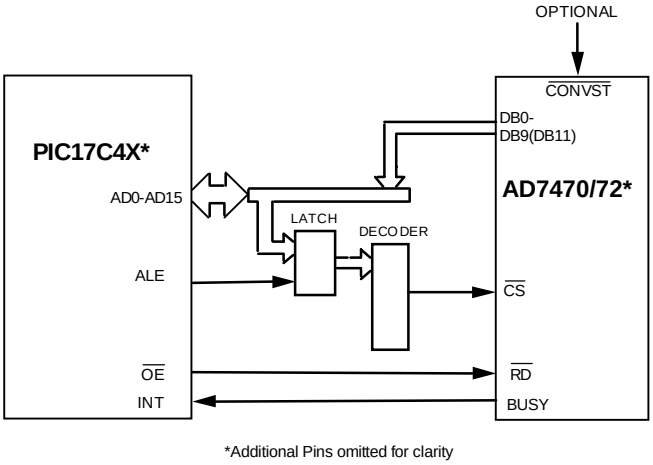


Figure 32. Interfacing to the PIC17C4X

AD7470/72 to 80C186 Interface

Figure 33 shows the AD7470/72 interfaced to the 80C186 microprocessor. The 80C186 DMA controller provides two independent high-speed DMA channel where data transfer can occur between memory and I/O spaces (the AD7470/72 occupies one of these I/O spaces). Each data transfer consumes 2 bus cycles, one cycle to fetch data and the other to store data.

After the AD7470/72 has finished conversion, the BUSY line generates a DMA request to Channel 1 (DRQ1). As a result of the interrupt, the processor performs a DMA READ operation which also resets the interrupt latch. Sufficient priority must be assigned to the DMA channel to ensure that the DMA request will be serviced before the completion of the next conversion. This configuration can be used with 6MHz and 8MHz 80C186 processors.

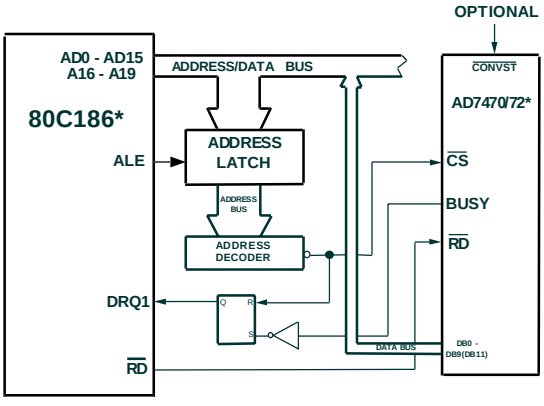


Figure 33. Interfacing to the 80C186

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Fig 34. 24-LEAD SOIC (R-24)

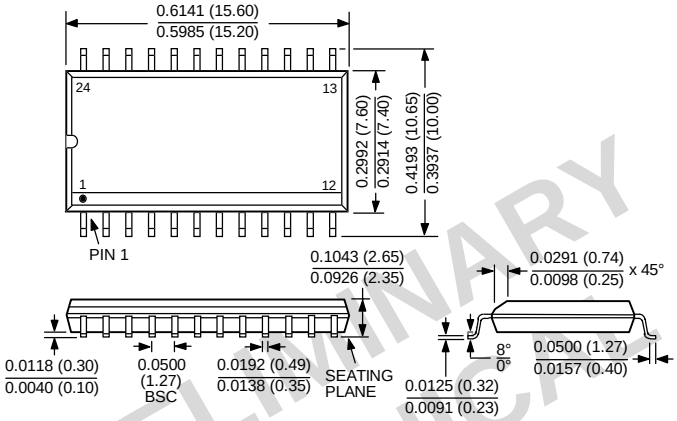


Fig 35. 24-LEAD TSSOP (RU-24)