ANALOG DEVICES

1 MSPS, 12-/10-Bit ADCs in 6-Lead SOT-23

AD7476/AD7477

FEATURES
Fast Throughput Rate: 1 MSPS
Specified for V_{DD} of 2.35 V to 5.25 V
Low Power:
    3.6 mW Typ at 1 MSPS with 3 V Supplies
    15 mW Typ at 1 MSPS with 5 V Supplies
Wide Input Bandwidth:
    70 dB SNR at 100 kHz Input Frequency
Flexible Power/Serial Clock Speed Management
No Pipeline Delays
High-Speed Serial Interface
    SPI™/QSPI™/MICROWIRE™/DSP Compatible
Standby Mode: 1 μA Max
6-Lead SOT-23 Package

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD7476/AD7477 are, respectively, 12-bit and 10-bit, high speed, low-power, successive-approximation ADCs. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low-noise, wide bandwidth track/hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and the conversion is also initiated at this point. There are no pipelined delays associated with the part.

The AD7476/AD7477 use advanced design techniques to achieve very low-power dissipation at high throughput rates.
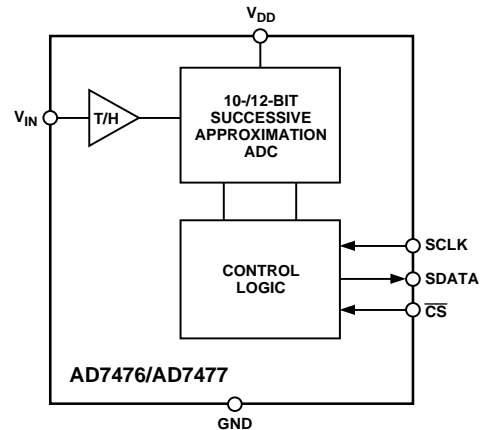
The reference for the part is taken internally from V_{DD}. This allows the widest dynamic input range to the ADC. Thus the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. First 12-/10-bit ADCs in an SOT-23 package.

2. High Throughput with Low Power Consumption.

3. Flexible Power/Serial Clock Speed Management.
   The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Power consumption is 1 μA max when in shutdown.

4. Reference derived from the power supply.

5. No Pipeline Delay.
   The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

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MICROWIRE is a trademark of National Semiconductor Corporation.

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AD7476–SPECIFICATIONS[1]

(A Version: V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS unless otherwise noted; B Version: V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 12 MHz, f_{SAMPLE} = 600 kSPS unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE				f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[2]	69	70	dB min	
	70		dB min	T_A = 25°C
Signal-to-Noise Ratio (SNR)[2]	70	71	dB min	
Total Harmonic Distortion (THD)[2]	–80	–78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[2]	–82	–80	dB typ	
Intermodulation Distortion (IMD)[2]				
Second Order Terms	–78	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third Order Terms	–78	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	10	ns max	
Aperture Jitter	30	30	ps typ	
Full Power Bandwidth	6.5	6.5	MHz typ	@ 3 dB
DC ACCURACY				B Version, V_{DD} = (2.35 V to 3.6 V)[3]; A Version, V_{DD} = (2.7 V to 3.6 V)
Resolution	12	12	Bits	
Integral Nonlinearity[2]		±1.5	LSB max	
	±1	±0.6	LSB typ	
Differential Nonlinearity[2]		–0.9/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.75	±0.75	LSB typ	
Offset Error[2]		±2	LSB max	
	±0.5		LSB typ	
Gain Error[2]		±2	LSB max	
	±0.5		LSB typ	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	30	30	pF typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
	2.35	2.35	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.4	0.4	V max	V_{DD} = 3 V
	0.8	0.8	V max	V_{DD} = 5 V
Input Current, I_{IN}, SCLK Pin	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	±1	µA typ	
Input Capacitance, C_{IN}[2, 4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DD} – 0.2	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[2, 4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	0.8	1.33	µs max	Sixteen SCLK Cycles
Track/Hold Acquisition Time	500	500	ns max	Full-Scale Step Input
	350	400	ns max	Sine Wave Input ≤100 kHz
Throughput Rate	1000	600	kSPS max	See Serial Interface Section
POWER REQUIREMENTS				
V_{DD}	2.35/5.25	2.35/5.25	V min/max	
I_{DD}				Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	2	mA typ	V_{DD} = 4.75 V to 5.25 V. SCLK On or Off
	1	1	mA typ	V_{DD} = 2.35 V to 3.6 V. SCLK On or Off
Normal Mode (Operational)	3.5	3	mA max	V_{DD} = 4.75 V to 5.25 V. f_{SAMPLE} = f_{SAMPLE}MAX[5]
	1.6	1.4	mA max	V_{DD} = 2.35 V to 3.6 V. f_{SAMPLE} = f_{SAMPLE}MAX[5]
Full Power-Down Mode	1	1	µA max	SCLK Off
	80	80	µA max	SCLK On
Power Dissipation[6]				
Normal Mode (Operational)	17.5	15	mW max	V_{DD} = 5 V. f_{SAMPLE} = f_{SAMPLE}MAX[5]
	4.8	4.2	mW max	V_{DD} = 3 V. f_{SAMPLE} = f_{SAMPLE}MAX[5]
Full Power-Down	5	5	µW max	V_{DD} = 5 V. SCLK Off
	3	3	µW max	V_{DD} = 3 V. SCLK Off

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]See Terminology.
[3]Maximum B Version specs apply as typical figures when V_{DD} = 5.25 V.
[4]Sample tested at 25°C to ensure compliance.
[5]A Version: f_{SAMPLE}MAX = 1 MSPS; B Version: f_{SAMPLE}MAX = 600 kSPS.
[6]See Power Versus Throughput Rate section.

Specifications subject to change without notice.

AD7477–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	AD7477[1, 2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz Sine Wave, f_{SAMPLE} = 1 MSPS
Signal-to-Noise + Distortion (SINAD)	61	dB min	
Total Harmonic Distortion (THD)	–73	dB max	
Peak Harmonic or Spurious Noise (SFDR)	–74	dB max	
Intermodulation Distortion (IMD)			
Second Order Terms	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Third Order Terms	–78	dB typ	fa = 103.5 kHz, fb = 113.5 kHz
Aperture Delay	10	ns max	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	6.5	MHz typ	@ 3 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±1	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±1	LSB max	
Gain Error	±1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{DD}	V	
DC Leakage Current	±1	µA max	
Input Capacitance	30	pF typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±1	µA typ	
Input Capacitance, C_{IN}[3, 4]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	µA max	
Floating-State Output Capacitance[3, 4]	10	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	800	ns max	Sixteen SCLK Cycles with SCLK at 20 MHz
Track/Hold Acquisition Time	400	ns max	
Throughput Rate	1	MSPS max	See Serial Interface Section
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2	mA typ	V_{DD} = 4.75 V to 5.25 V. SCLK On or Off
	1	mA typ	V_{DD} = 2.7 V to 3.6 V. SCLK On or Off
Normal Mode (Operational)	3.5	mA max	V_{DD} = 4.75 V to 5.25 V. f_{SAMPLE} = 1 MSPS
	1.6	mA max	V_{DD} = 2.7 V to 3.6 V. f_{SAMPLE} = 1 MSPS
Full Power-Down Mode	1	µA max	SCLK Off
	80	µA max	SCLK On
Power Dissipation[5]			
Normal Mode (Operational)	17.5	mW max	V_{DD} = 5 V. f_{SAMPLE} = 1 MSPS
	4.8	mW max	V_{DD} = 3 V. f_{SAMPLE} = 1 MSPS
Full Power-Down	5	µW max	V_{DD} = 5 V. SCLK Off

NOTES
[1]Temperature ranges as follows: A Version: –40°C to +85°C.
[2]Operational from V_{DD} = 2.35 V.
[3]See Terminology.
[4]Sample tested at 25°C to ensure compliance.
[5]See Power Versus Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = 2.35 V to 5.25 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7476/AD7477		Unit	Description
	3 V[2]	5 V[2]		
f_{SCLK}[3]	10	10	kHz min	
	20	20	MHz max	A Version
	12	12	MHz max	B Version
$t_{CONVERT}$	$16 \times t_{SCLK}$	$16 \times t_{SCLK}$		
t_{QUIET}	50	50	ns min	Minimum Quiet Time Required Between Bus Relinquish and Start of Next Conversion
t_1	10	10	ns min	Minimum $\overline{CS}$ Pulsewidth
t_2	10	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[4]	20	20	ns max	Delay from $\overline{CS}$ Until SDATA Three-State Disabled
t_4[4]	40	20	ns max	Data Access Time After SCLK Falling Edge. A Version
	70	20	ns max	Data Access Time After SCLK Falling Edge. B Version
t_5	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulsewidth
t_6	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulsewidth
t_7	10	10	ns min	SCLK to Data Valid Hold Time
t_8[5]	10	10	ns min	SCLK Falling Edge to SDATA High Impedance
	25	25	ns max	SCLK Falling Edge to SDATA High Impedance
$t_{POWER-UP}$[6]	1	1	μs typ	Power-Up Time from Full Power-Down

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2]3 V specifications apply from V_{DD} = 2.7 V to 3.6 V for A Version; 3 V specifications apply from V_{DD} = 2.35 V to 3.6 V for B Version; 5 V specifications apply from V_{DD} = 4.75 V to 5.25 V.

[3]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[5]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[6]See Power-up Time section.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . –0.3 V to +7 V
Analog Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND . . . . –0.3 V to +7 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] . . . . ±10 mA
Operating Temperature Range
 Commercial (A, B Version) . . . . –40°C to +85°C
 Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . 150°C
SOT-23 Package, Power Dissipation . . . . 450 mW
 θ_{JA} Thermal Impedance . . . . 230°C/W
 θ_{JC} Thermal Impedance . . . . 92°C/W
Lead Temperature, Soldering
 Vapor Phase (60 secs) . . . . 215°C
 Infrared (15 secs) . . . . 220°C
ESD . . . . 3.5 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

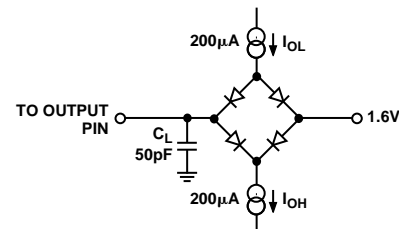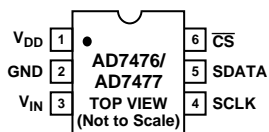[2]Transient currents of up to 100 mA will not cause SCR latch-up.

Figure 1. Load Circuit for Digital Output Timing Specifications

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7476/AD7477 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WARNING!

ESD SENSITIVE DEVICE

REV. 0

PIN CONFIGURATION


```
        ┌──────⌣──────┐
VDD  1 ─┤●            ├─ 6  CS
        │  AD7476/    │
GND  2 ─┤  AD7477     ├─ 5  SDATA
        │  TOP VIEW   │
VIN  3 ─┤ (Not to Scale)├─ 4  SCLK
        └─────────────┘
```

PIN FUNCTION DESCRIPTIONS

Pin No.	Pin Mnemonic	Function
1	V_{DD}	Power Supply Input. The V_{DD} range for the AD7476/AD7477 is from 2.35 V to 5.25 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the AD7476/AD7477. All analog input signals should be referred to this GND voltage.
3	V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 to V_{DD}.
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476/AD7477's conversion process.
5	SDATA	Data Out. Logic output. The conversion result from the AD7476/AD7477 is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476 consists of four leading zeros followed by the 12 bits of conversion data which is provided MSB first, and the data stream from the AD7477 consists of four leading zeros followed by the 10 bits of conversion data, followed by two trailing zeroes, which is also provided MSB first.
6	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476/AD7477 and framing the serial data transfer.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding Information
AD7476ART	–40°C to +85°C	±1 typ	RT-6	CEA
AD7476BRT	–40°C to +85°C	±1.5 max	RT-6	CEB
AD7477ART	–40°C to +85°C	±1 max	RT-6	CFA
EVAL-AD7476CB[3]				
EVAL-AD7476CB[3]				
EVAL-CONTROL BOARD[4]				

NOTES
[1]Linearity Error here refers to integral linearity error.
[2]RT = SOT-23.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

AD7476/AD7477

TERMINOLOGY

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 0.5 LSB.

Gain Error

This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1.5 LSB) after the offset error has been adjusted out.

Track/Hold Acquisition Time

The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See Serial Interface Timing section for more detail.

Signal-to-(Noise + Distortion) Ratio

This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter it is 62 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7476/AD7477 it is defined as:

$$THD\ (dB) = 20\ \log \frac{\sqrt{(V_2{}^2 + V_3{}^2 + V_4{}^2 + V_5{}^2 + V_6{}^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7476/AD7477 are tested using the CCIF standard where two input frequencies are used, fa = 103.5 kHz and fb = 113.5 kHz. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PERFORMANCE CURVES

Figure 2 shows a typical FFT plot for the AD7476 at 1 MHz sample rate and 100 kHz input frequency.
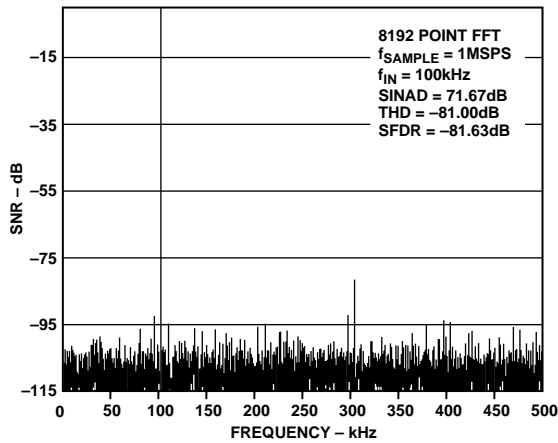

Figure 2. AD7476 Dynamic Performance at 1 MSPS

Figure 3 shows a typical FFT plot for the AD7476 at 600 kHz sample rate and 100 kHz input frequency.
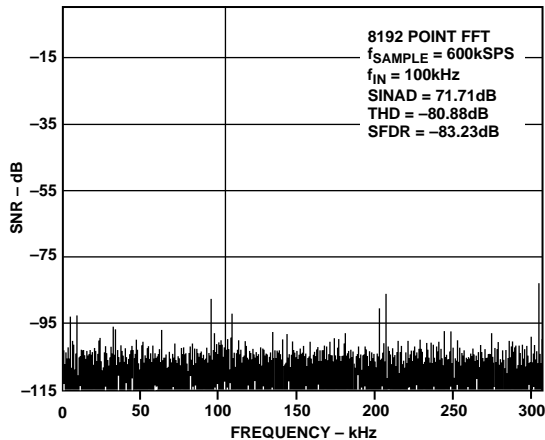

Figure 3. AD7476 Dynamic Performance at 600 kSPS

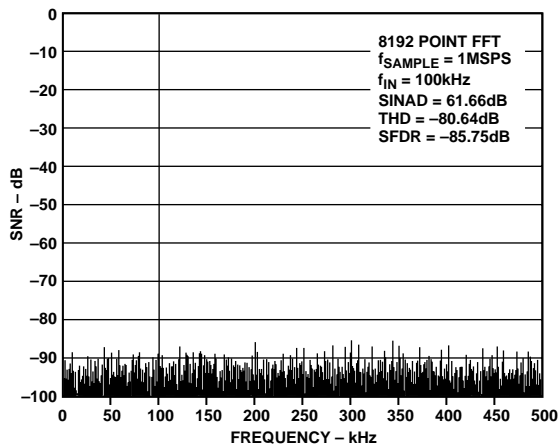Figure 4 shows a typical FFT plot for the AD7477 at 1 MHz sample rate and 100 kHz input frequency.

Figure 4. AD7477 Dynamic Performance at 1 MSPS

Figure 5 shows the signal-to-(noise + distortion) ratio performance versus input frequency for various supply voltages while sampling at 993 kSPS with an SCLK frequency of 20 MHz.

Figure 5. AD7476 SINAD vs. Input Frequency at 993 kSPS

Figure 6 shows the signal-to-(noise + distortion) ratio performance versus input frequency for various supply voltages while sampling at 605 kSPS with a SCLK frequency of 12 MHz.

Figure 6. AD7476 SINAD vs. Input Frequency at 605 kSPS

CIRCUIT INFORMATION

The AD7476/AD7477 are, respectively, fast, micropower, 12-bit and 10-bit, single supply, A/D converters. The parts can be operated from a 2.35 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7476/AD7477 are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7476/AD7477 provide the user with an on-chip track/hold, A/D converter, and a serial interface housed in a tiny 6-lead SOT-23 package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part and also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 to V_{DD}. An external reference is not required for the ADC, nor is there a reference on-chip. The reference for the AD7476/AD7477 is derived from the power supply and thus gives the widest dynamic input range.

AD7476/AD7477

The AD7476/AD7477 also feature a power-down option to save power between conversions. The power-down feature is implemented across the standard serial interface as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7476/AD7477 is a successive-approximation analog-to-digital converter based around a charge redistribution DAC. Figures 7 and 8 show simplified schematics of the ADC. Figure 7 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

Figure 7. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 8), SW2 will open and SW1 will move to Position B causing the comparator to become unbalanced. The Control Logic and the Charge Redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The Control Logic generates the ADC output code. Figure 9 shows the ADC transfer function.

Figure 8. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476/AD7477 is straight binary. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, etc.). The LSB size for the AD7476 is = $V_{DD}/4096$ and the LSB size for the AD7477 is = $V_{DD}/1024$. The ideal transfer characteristic for the AD7476/AD7477 is shown in Figure 9.
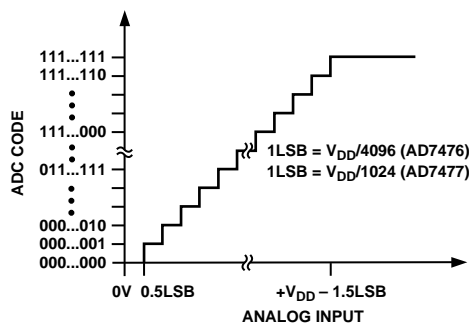

Figure 9. Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 10 shows a typical connection diagram for the AD7476/AD7477. V_{REF} is taken internally from V_{DD} and as such V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit or 10-bit result. The 10-bit result from the AD7477 will be followed by two trailing zeros.

Alternatively, because the supply current required by the AD7476/AD7477 is so low, a precision reference can be used as the supply source to the AD7476/AD7477. A REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 10). This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (e.g., 15 V). The REF19x will output a steady voltage to the AD7476/AD7477. If the low dropout REF193 is used, the current it typically needs to supply to the AD7476/AD7477 is 1 mA. When the ADC is converting at a rate of 1 MSPS, the REF193 will need to supply a maximum of 1.6 mA to the AD7476/AD7477. The load regulation of the REF193 is typically 10 ppm/mA (REF193, V_S = 5 V), which results in an error of 16 ppm (80 µV) for the 1.6 mA drawn from it. This corresponds to a 0.11 LSB error for the AD7476 with V_{DD} = 3 V from the REF193, and a 0.03 LSB error for the AD7477. For applications where power consumption is of concern, the power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See Modes of Operation section.
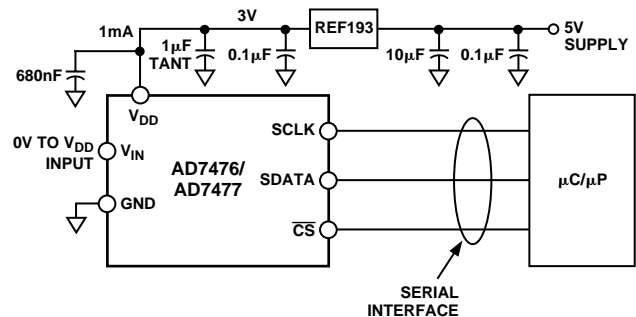

Figure 10. REF193 as Power Supply to AD7476/AD7477

Table I provides some typical performance data with various references used as a V_{DD} source with a low frequency analog input. Under the same setup conditions the references were compared and the AD780 proved the optimum reference.

Table I.

Reference Tied to V_{DD}	AD7476 SNR Performance 1 kHz Input
AD780 @ 3 V	71.17 dB
REF193	70.4 dB
AD780 @ 2.5 V	71.35 dB
REF192	70.93 dB
AD1852	70.05 dB

Analog Input

Figure 11 shows an equivalent circuit of the analog input structure of the AD7476/AD7477. The two diodes D1 and D2 provide

ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 200 mV. This will cause these diodes to become forward-biased and start conducting current into the substrate. 20 mA is the maximum current these diodes can conduct without causing irreversible damage to the part. The capacitor C1 in Figure 11 is typically about 4 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 30 pF. For ac applications, removing high-frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.
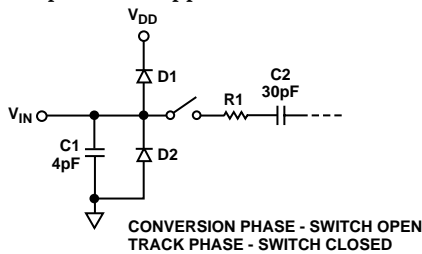

Figure 11. Equivalent Analog Input Circuit

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and performance will degrade. Figure 12 shows a graph of the total harmonic distortion versus source impedance for different analog input frequencies when using a supply voltage of 2.7 V and sampling at a rate of 605 kSPS. Figures 13 and 14 each show a graph of the total harmonic distortion versus analog input signal frequency for various supply voltages while sampling at 993 kSPS with an SCLK frequency of 20 MHz and 605 kSPS with a SCLK frequency of 12 MHz respectively.
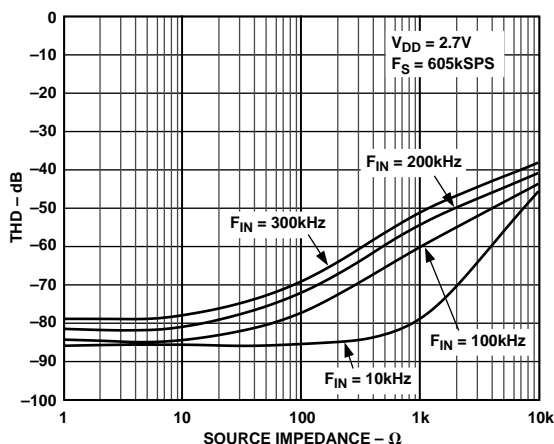

Figure 12. THD vs. Analog Input Frequency for Various Source Impedance
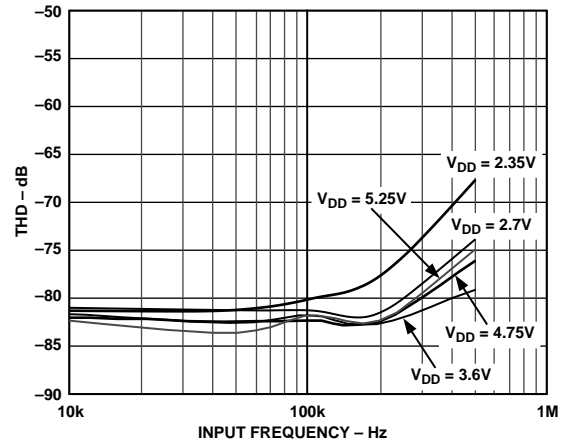

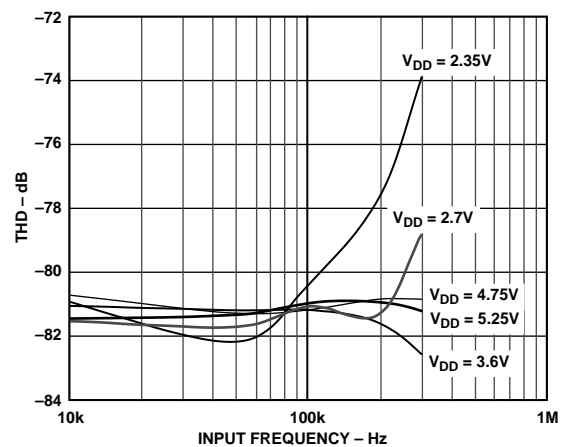Figure 13. THD vs. Analog Input Frequency, f_S = 993 kSPS

Figure 14. THD vs. Analog Input Frequency, f_S = 605 kSPS

Digital Inputs

The digital inputs applied to the AD7476/AD7477 are not limited by the maximum ratings which limit the analog inputs. Instead, the digitals inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog inputs. For example, if the AD7476/AD7477 were operated with a V_{DD} of 3 V, then 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK are applied before V_{DD} then there is no risk of latch-up as there would be on the analog inputs if a signal greater than 0.3 V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7476/AD7477 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation, Normal Mode and Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether or not the AD7476/AD7477 will enter power-down mode. Similarly, if already in power-down, $\overline{CS}$ can control whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

AD7476/AD7477

Normal Mode

This mode is intended for fastest throughput rate performance, as the user does not have to worry about any power-up times with the AD7476/AD7477 remaining fully powered all the time. Figure 15 shows the general diagram of the operation of the AD7476/AD7477 in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge, but before the 16th SCLK falling edge, the part will remain powered up but the conversion will be terminated and SDATA will go back into three-state. Sixteen serial clock cycles are required to complete the conversion and access the complete conversion result. $\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion, (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by again bringing $\overline{CS}$ low.

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7476/AD7477 is in power-down, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK as shown in Figure 16. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power-down and the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated and SDATA will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power-down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7476/AD7477 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up once 16 SCLKs have elapsed and, as shown in Figure 17, valid data will result from the next conversion. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, the AD7476/AD7477 will again go back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will again power down on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

Power-Up Time

The power-up time of the AD7476/AD7477 is typically 1 μs, which means that with any frequency of SCLK up to 20 MHz, one dummy cycle will always be sufficient to allow the device to power-up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly.
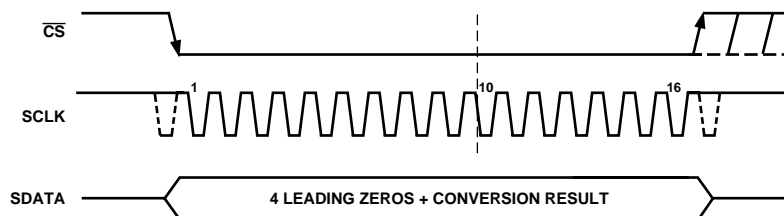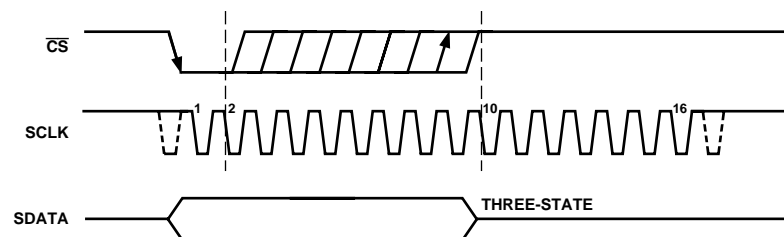

Figure 15. Normal Mode Operation

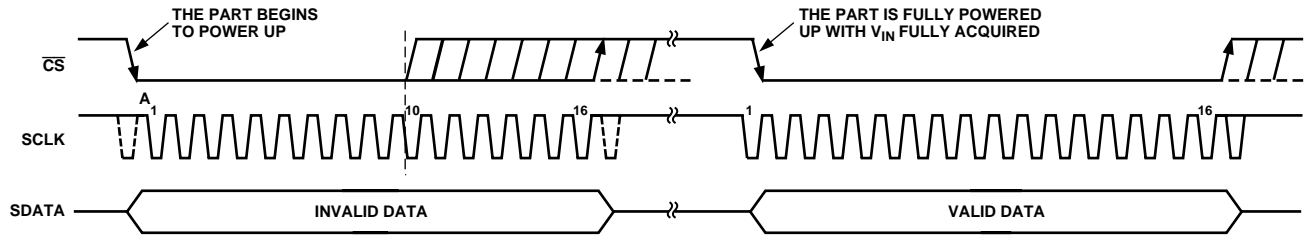*Figure 16. Entering Power-Down Mode*

Figure 17. Exiting Power-Down Mode

The quiet time t_{QUIET} must still be allowed from the point at which the bus goes back into three-state after the dummy conversion, to the next falling edge of $\overline{CS}$. When running at 1 MSPS throughput rate, the AD7476/AD7477 will power up and acquire a signal within ±0.5 LSB in one dummy cycle, i.e., 1 μs.

When powering up from the power-down mode with a dummy cycle, as in Figure 17, the track and hold that was in hold mode while the part was powered down, returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 17. Although at any SCLK frequency one dummy cycle is sufficient to power up the device and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and fully acquire V_{IN}; 1 μs will be sufficient to power up the device and acquire the input signal. If, for example, a 5 MHz SCLK frequency were applied to the ADC, the cycle time would be 3.2 μs. In one dummy cycle, 3.2 μs, the part would be powered up and V_{IN} fully acquired. However after 1 μs with a 5 MHz SCLK only five SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. So, in this case, the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time t_{QUIET} to initiate the conversion.

When power supplies are first applied to the AD7476/AD7477, the ADC may power up in either power-down mode or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the power-down mode while not in use and the user wishes the part to power up in power-down mode, the dummy cycle may be used to ensure the device is in power-down by executing a cycle such as that shown in Figure 16. Once supplies are applied to the AD7476/AD7477, the power-up time is the same as that when powering up from the power-down mode. It takes approximately 1 μs to fully power up if the part powers up in normal mode. It is not necessary to wait 1 μs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is then performed directly after the dummy conversion, care must be taken to ensure that adequate acquisition time has been allowed. As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track and hold will already be in track. This means that if the ADC powers up in the desired mode of operation, and a dummy cycle is not required to change mode, a dummy cycle is not required to place the track and hold into track.

POWER VERSUS THROUGHPUT RATE

By using the power-down mode on the AD7476/AD7477 when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 18 shows how as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

For example if the AD7476/AD7477 is operated in a continuous sampling mode with a throughput rate of 100 kSPS and a SCLK of 20 MHz (V_{DD} = 5 V), and the device is placed in the power-down mode between conversions, then the power consumption is calculated as follows. The power dissipation during normal operation is 17.5 mW (V_{DD} = 5 V). If the power-up time is one dummy cycle, i.e., 1 μs, and the remaining conversion time is another cycle, i.e., 1 μs, then the AD7476/AD7477 can be said to dissipate 17.5 mW for 2 μs during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 μs and the average power dissipated during each cycle is $(2/10) \times (17.5 \text{ mW})$ = 3.5 mW. If V_{DD} = 3 V, SCLK = 20 MHz and the device is again in power-down mode between conversions, the power dissipation during normal operation is 4.8 mW. The AD7476/AD7477 can now be said to dissipate 4.8 mW for 2 μs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is $(2/10) \times (4.8 \text{ mW})$ = 0.96 mW. Figure 18 shows the power versus throughput rate when using the power-down mode between conversions with both 5 V and 3 V supplies.
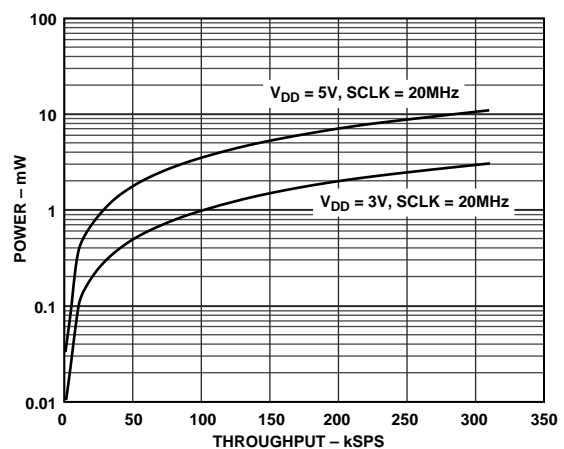

Figure 18. Power vs. Throughput AD7476/AD7477

The power-down mode is intended for use with throughput rates of approximately 333 kSPS and under as at higher sampling rates power is not saved by using the power-down mode.

AD7476/AD7477

SERIAL INTERFACE

Figure 19 and Figure 20 show the detailed timing diagram for serial interfacing to the AD7476 and the AD7477 respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7476/AD7477 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of three-state and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track and hold will go back into track on the next SCLK rising edge as shown in Figures 19 and 20 at Point B. On the 16th SCLK falling edge the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated

and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the 16th SCLK falling edge as shown in Figures 19 and Figure 20. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476/AD7477. $\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero. Thus the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e., the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the first leading zero provided and the 15th rising SCLK edge would have DB0 provided.
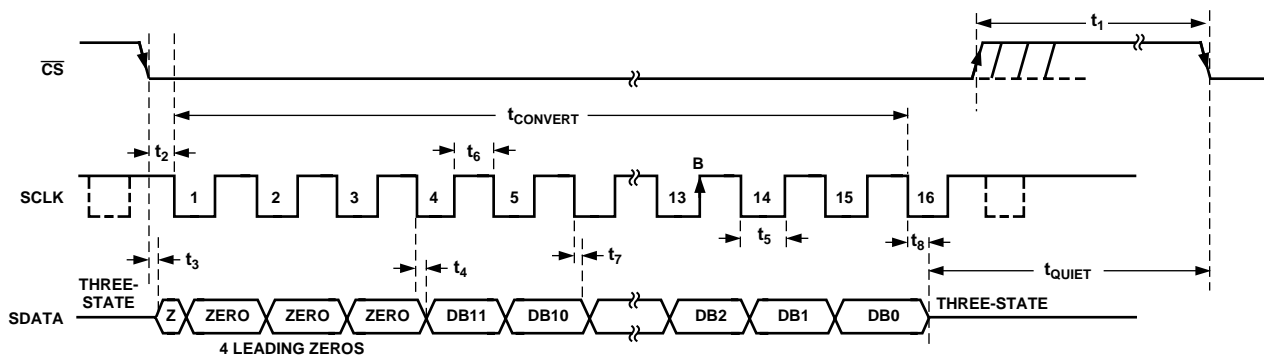

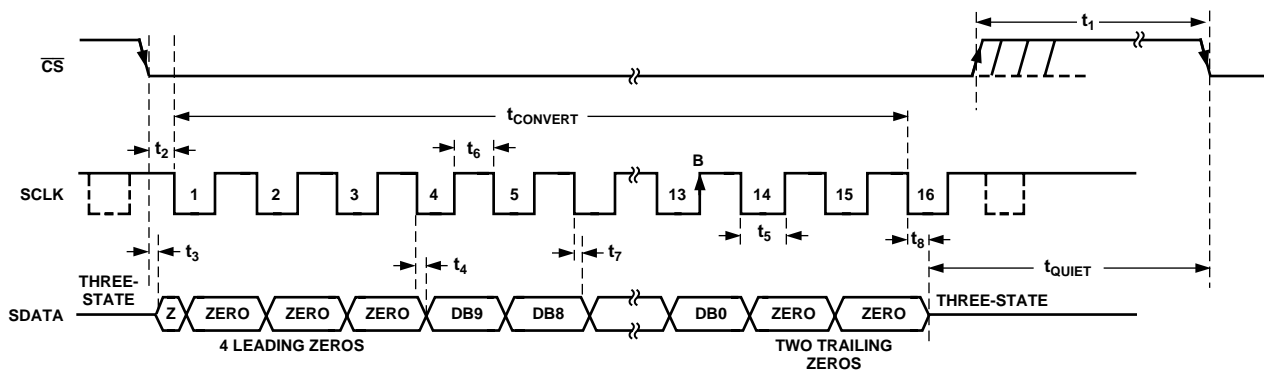Figure 19. AD7476 Serial Interface Timing Diagram

Figure 20. AD7477 Serial Interface Timing Diagram

–12–

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MICROPROCESSOR INTERFACING

The serial interface on the AD7476/AD7477 allows the part to be directly connected to a range of many different microprocessors. This section explains how to interface the AD7476/AD7477 with some of the more common microcontroller and DSP serial interface protocols.

AD7476/AD7477 to TMS320C5x/C54x Interface

The serial interface on the TMS320C5x uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices like the AD7476/AD7477. The $\overline{CS}$ input allows easy interfacing between the TMS320C5x/C54x and the AD7476/AD7477 without any glue logic required. The serial port of the TMS320C5x/C54x is set up to operate in burst mode with internal CLKX (Tx serial clock) and FSX (Tx frame sync). The serial port control register (SPC) must have the following setup: FO = 0, FSM = 1, MCM = 1 and TXM = 1. The format bit, FO, may be set to 1 to set the word length to eight bits, in order to implement the power-down mode on the AD7476/AD7477. The connection diagram is shown in Figure 21. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C5x/C54x will provide equidistant sampling.
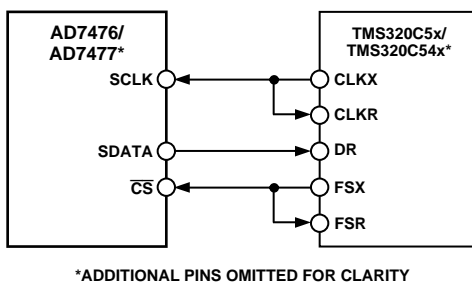

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 21. Interfacing to the TMS320C5x/C54x

AD7476/AD7477 to ADSP-21xx Interface

The ADSP21xx family of DSPs are interfaced directly to the AD7476/AD7477 without any glue logic required. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
SLEN = 1111, 16-Bit Data Words
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0
ITFS = 1

To implement the power-down mode SLEN should be set to 1001 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 22. The ADSP-21xx has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in Alternate Framing Mode and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$ and as with all signal processing applications equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers etc., are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and hence the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given (i.e., AX0 = TX0), the state of the SCLK is checked. The DSP will wait until the SCLK has gone High, Low, and High before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, a SCLK of 2 MHz is obtained, and eight master clock periods will elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling will be implemented by the DSP.
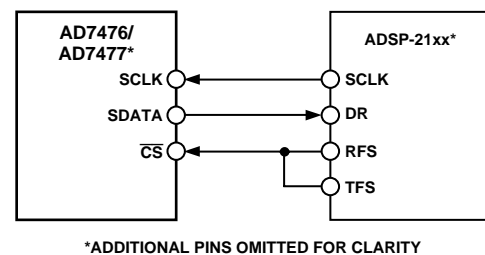

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 22. Interfacing to the ADSP-21xx

AD7476/AD7477 to DSP56xxx Interface

The connection diagram in Figure 23 shows how the AD7476/AD7477 can be connected to the SSI (Synchronous Serial Interface) of the DSP56xxx family of DSPs from Motorola. The SSI is operated in Synchronous Mode (SYN bit in CRB =1) with internally generated 1-bit clock period frame sync for both Tx and Rx (Bits FSL1 = 1 and FSL0 = 0 in CRB). Set the word length to 16 by setting bits WL1 = 1 and WL0 = 0 in CRA. To implement the power-down mode on the AD7476/AD7477, the word length can be changed to eight bits by setting bits WL1 = 0 and WL0 = 0 in CRA. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP56xxx will provide equidistant sampling.
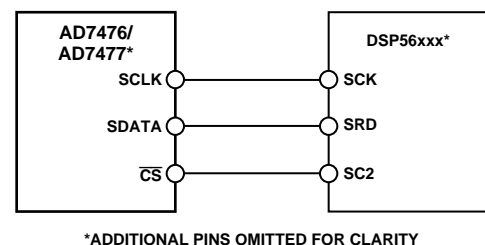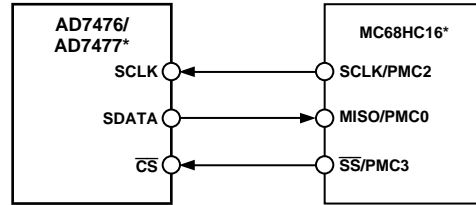

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 23. Interfacing to the DSP56xxx

AD7476/AD7477

AD7476/AD7477 to MC68HC16 Interface

The Serial Peripheral Interface (SPI) on the MC68HC16 is configured for Master Mode (MSTR = 1), Clock Polarity Bit (CPOL) = 1 and the Clock Phase Bit (CPHA) = 0. The SPI is configured by writing to the SPI Control Register (SPCR)—see *68HC16 User Manual.* The serial transfer will take place as a 16-bit operation when the SIZE bit in the SPCR register is set to SIZE = 1. To implement the power-down mode with an 8-bit transfer set SIZE = 0. A connection diagram is shown in Figure 24.
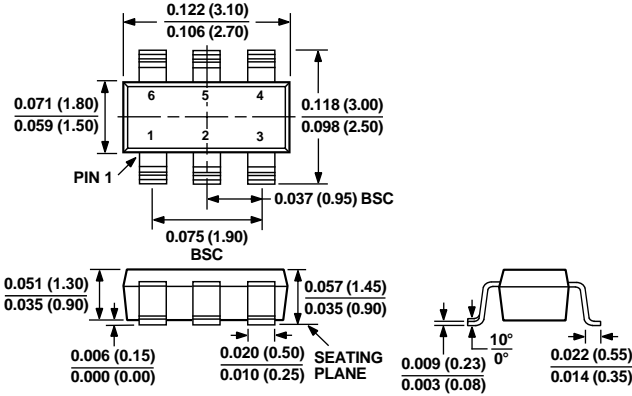

*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 24. Interfacing to the MC68HC16

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OUTLINE DIMENSIONS
(Dimensions shown in inches and (mm).)

6-Lead SOT-23
(RT-6)