

Preliminary Technical Data

AD8018

FEATURES

Line drive amplifiers provide 8Vpp differential output drive. Ideal xDSL line driver for USB, PCMCIA or PCI based Customer Premise Equipment (CPE).

High Output Voltage and Current Drive

350mA Minimum Output Drive Current
8Vp-p Differential Output Voltage, $R_L = 11\Omega$

Low Distortion

-95dBc SFDR @ 100kHz into 11Ω , 6Vpp Differential

4nV/ $\sqrt{\text{Hz}}$ Voltage noise density, 100kHz

Out of Band MTPR = -87dBc, 144kHz to 500kHz,

$Z_{\text{line}} = 11\Omega$, $P_{\text{line}} = 13\text{dBm}$

Low Power Operation

+5V to +8V Power Supply Range

2-bit logic controlled Stand-by, Shutdown

Low supply current of 9mA/amplifier (typ)

Current Feedback Amplifiers

High Speed

135MHz Bandwidth (-3dB)

370V/ μs Slew Rate

APPLICATIONS

xDSL USB, PCI, PCMCIA Cards

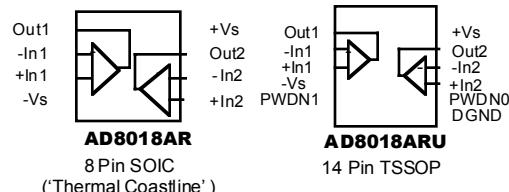
Consumer DSL Modems

Twisted Pair Line Driver

PRODUCT DESCRIPTION

The AD8018 is a dual, high speed, low cost amplifier capable of driving low distortion signals to within 0.5V of the supply rail. It is intended for use in single supply xDSL systems where low distortion and low cost is essential, and maximum reach on the line must be attained with the minimum of supply voltages. Each amplifier drives minimum 350mA of output current and while maintaining -95dBc of SFDR at 100kHz, outstanding performance for any xDSL CPE application. The AD8018 is available with flexible standby and shutdown modes. Two bit control (1.5V threshold referenced to DGND) will put the AD8018 into a full power, standby (outputs low Z) and shutdown (outputs high Z).

Fabricated in ADI's high speed XFCB process, the high bandwidth and fast slew rate of the AD8018 keep distortion to a minimum, while dissipating a minimum of power. The quiescent current of the AD8018 is low 8.7mA/amplifier max. Low distortion, high output voltage drive, and high output current drive in small packages make the AD8018 ideal for use in low cost USB, PCMCIA and PCI Customer Premise



8 Pin SOIC
('Thermal Coastline')

14 Pin TSSOP

Figure 1. Distortion verses Rload.

Equipment for ADSL, SDSL, VDSL and proprietary xDSL systems.

The AD8018 drive capability comes in compact 8 Lead SOIC, and 14 lead TSSOP, 'Thermal Coastline' packages. Both models will operate over the Temperature range -40°C to +85°C.

SPECIFICATIONS (@25°C, Vs=+5V, RL=100Ω, RF=RG=900Ω unless otherwise noted)

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|--|-----|------|-----------------|------------|
| DYNAMIC PERFORMANCE | | | | | |
| -3dB Bandwidth | G= +1, V _{OUT} <0.4V p-p | TBD | 135 | | MHz |
| | G= +2, V _{OUT} <0.4V p-p | TBD | 110 | | MHz |
| 0.1dB Bandwidth | V _{OUT} < 0.4V p-p | | 70 | | MHz |
| Large Signal Bandwidth | V _{OUT} = 4V p-p | | 50 | | MHz |
| Slew Rate | Non-Inverting, V _{OUT} =4Vp-p | | 370 | | V/ μ s |
| Rise & Fall Time | Non-Inverting, V _{OUT} =2Vp-p | | 5.5 | | ns |
| Settling Time | 0.1%, V _{OUT} = 2Vp-p | | 20 | | ns |
| NOISE / HARMONIC PERFORMANCE | | | | | |
| Distortion, | V _{OUT} = 6Vp-p (differential) | | | | |
| 2 nd Harmonic | 100kHz, R _L =11 Ω | | -97 | | dBc |
| | 500kHz, R _L =11 Ω | | -82 | | dBc |
| 3 rd Harmonic | 100kHz, R _L =11 Ω | | -95 | | dBc |
| | 500kHz, R _L =11 Ω | | -85 | | dBc |
| MTPR (Out of band) | 144kHz to 500kHz, R _l =11Ω | | -87 | | dBc |
| Input Noise Voltage | f=100kHz | 4 | TBD | nV/ \sqrt{Hz} | |
| Input Noise Current | f=100kHz (+ Inputs) | 1 | | pA/ \sqrt{Hz} | |
| Input Noise Current | f=100kHz (- Inputs) | 10 | | pA/ \sqrt{Hz} | |
| Crosstalk | f = 1MHz, G=+2 | TBD | | dB | |
| DC PERFORMANCE | | | | | |
| Input Offset Voltage | T _{min} -T _{max} | 1 | 5.5 | mV | |
| Input Offset Voltage Match | | 2 | 10 | mV | |
| Transimpedance | V _{OUT} = 2Vp-p, R _l = 11 Ohms | TBD | 15 | mV | |
| | T _{min} -T _{max} | TBD | | MΩ | |
| | | | | MΩ | |
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | +Input | | 10 | | MΩ |
| | -Input | | 125 | | Ω |
| Input Capacitance | +Input | | 0.5 | | pF |
| Input Bias Current (-) | T _{MIN} to T _{MAX} | | 0.25 | TBD | μA |
| Input Bias Current (-) Match | T _{MIN} to T _{MAX} | | TBD | TBD | μA |
| Input Bias Current (+) | T _{MIN} to T _{MAX} | | 1 | TBD | μA |
| Input Bias Current (+) Match | T _{MIN} to T _{MAX} | | TBD | TBD | μA |
| CMRR | V _{in} 2V to 4V | | 58 | | dB |
| Input CM Voltage Range | Conditions TBD | 2 | 4 | | V |
| OUTPUT CHARACTERISTICS | | | | | |
| Cap Load | 30% overshoot | TBD | | | |
| Output Resistance | Frequency = 100kHz, PWDN1, PWDN0 = "1" | 0.2 | | | |
| Output Voltage Swing | | 2 | 4 | | |
| Output Voltage Swing | | TBD | TBD | | |
| Linear Output Current | RI = 5.5Ω | 350 | 400 | | V |
| Short-Circuit Current | SFDR < -TBD dBc, f=100kHz, R _l =11 Ω | | 1000 | | V |
| | | | | mA | |
| | | | | mA | |
| POWER SUPPLY | | | | | |
| Supply Current/Amp | PWDN1= "1", PWDN0 = "1" | | 9 | TBD | m |
| | T _{min} - T _{max} | | TBD | | A |
| STBY Supply Current/Amp | PWDN1= "0", PWDN0 = "1" | | TBD | TBD | mA |
| SHUTDOWN Supply Current/Amp | PWDN1= "0", PWDN0 = "0" | | TBD | TBD | mA |
| Operating Range | Single Supply | +4 | +8 | | V |
| Power Supply Rejection Ratio | ΔVs = ± 1V | 56 | TBD | | dB |

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacturing unless otherwise agreed to in writing. Patents pending. Rev 2
PrC 1/21/00

SPECIFICATIONS (@25°C, Vs=+5V, RL=100Ω, RF=RG=900Ω unless otherwise noted)

Logic Inputs (PWDN [1,0])

Logic “1” Voltage
Logic “0” Voltage
Logic Input Bias Current
Standby Recovery Time

RL=11Ω, CL=?pF, G=?, IS = 90% of Typical

2.0
TBD
5

0.8

V
V
μA
μs

Preliminary
Technical
Data

Pr C 1/21/00

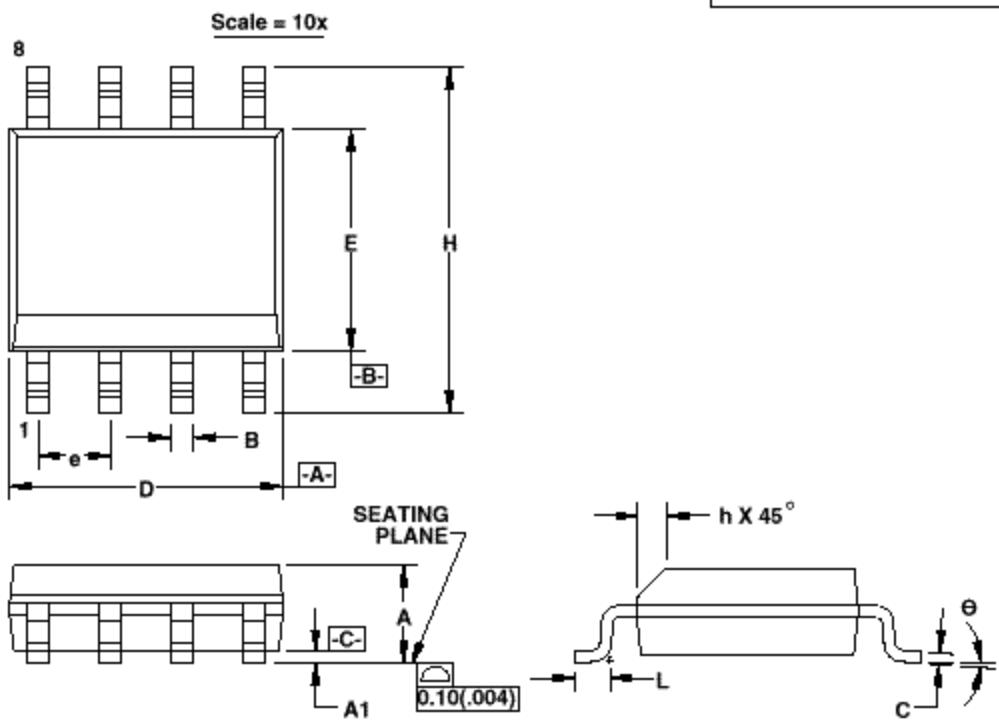
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Rev

3

PrC 1/21/00

Analog Devices Confidential Information



| MILLIMETERS | | |
|-------------|-----------|------|
| Dimension | Min. | Max |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC. | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| Θ | 0° | 8° |

| INCHES | | |
|-----------|-----------|-------|
| Dimension | Min. | Max |
| A | .0532 | .0688 |
| A1 | .0040 | .0098 |
| B | .013 | .020 |
| C | .0075 | .0098 |
| D | .1890 | .1968 |
| E | .1497 | .1574 |
| e | .050 BSC. | |
| H | .2284 | .2440 |
| h | .0099 | .0196 |
| L | .016 | .050 |
| Θ | 0° | 8° |

**Title: 8L SOIC 150 mil
Package Outline
CUSTOMER**

NOTES:

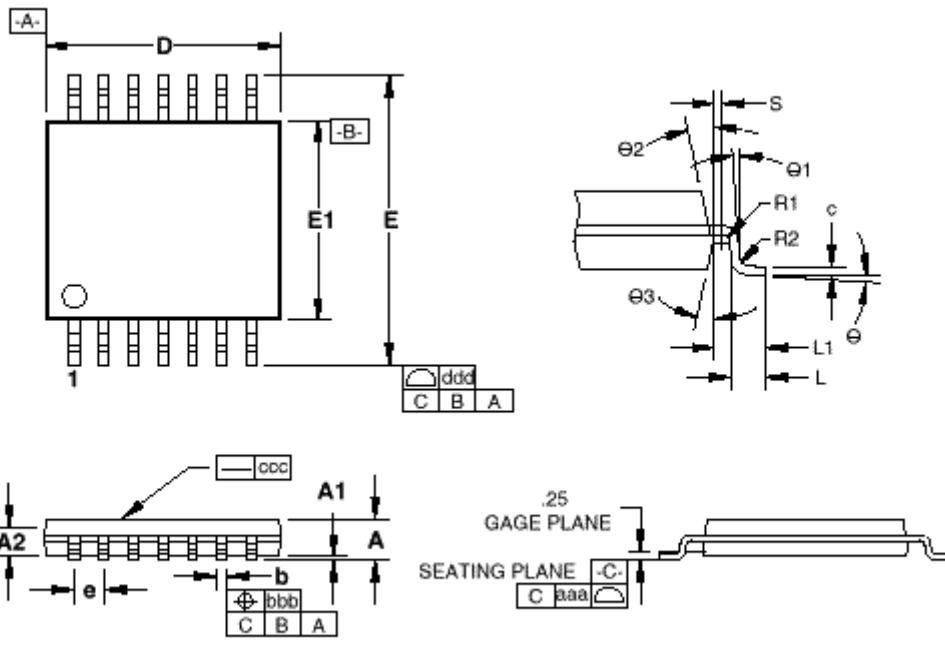
1. Controlling Dimensions are in mm.
2. All Dimensions per JEDEC Standards MS-012 AA

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| Dim | Min. | Nom. | Max |
|-----|------|----------|------|
| A | | | 1.2 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.80 | 1.00 | 1.05 |
| D | 4.90 | 5.00 | 5.10 |
| E | | 6.40 BSC | |
| E1 | 4.30 | 4.40 | 4.50 |
| b | 0.19 | | 0.30 |
| c | 0.09 | | 0.20 |
| e | | 0.65 BSC | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | | 1.00 REF | |
| R1 | 0.09 | | |
| R2 | 0.09 | | |
| S | 0.20 | | |
| θ1 | 0° | | 8° |
| θ2 | | 12° REF | |
| θ3 | | 12° REF | |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.05 | |
| ddd | | 0.20 | |

NOTES:

1. Controlling Dimensions are in mm.
2. All Dimensions per JEDEC Standards MO-153-AB-1

**Title: 14L TSSOP 4.40mm
Package Outline
Customer**



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