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+5V CATV Line Driver
Coarse Step

Preliminary Technical Data — AD8322

FEATURES

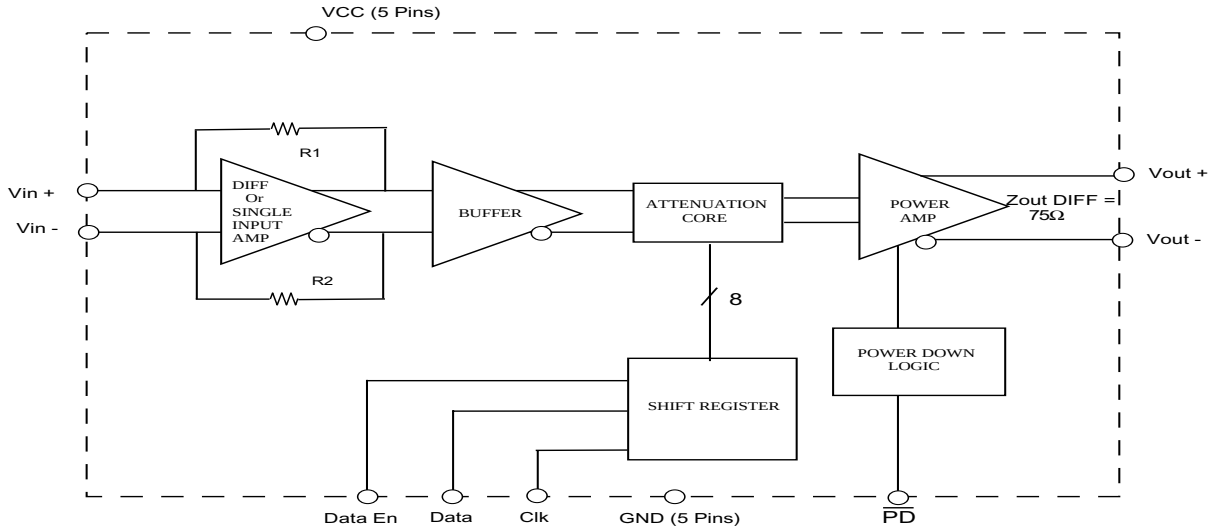
Supports DOCSIS standard for reverse path transmission
Gain Programmable in 6 dB steps over a 42dB Range
Low Distortion at 11dBm output:
  -56 dBc SFDR at 42MHz
  -52 dBc SFDR at 65MHz
11 nV/√Hz Output Noise Level
Low Power-up/Power-down Glitch
Maintains 75Ω Output Impedance
  Power up and Power down Condition
Upper Bandwidth: 180 MHz (Min Gain)
+5V Supply Operation
Supports SPI and Parallel Control Interfaces
  TTL / CMOS Logic Levels

APPLICATIONS

Gain Programmable Line Driver
  DOCSIS Compliant Cable Data Modems
  Interactive Set-top Boxes
  PC Plug-in Modems
General Purpose Digitally Controlled Variable Gain Block

ORDERING GUIDE

Model	Temperature Range	Package
AD8322ARU	-40°C to +85°C	28-Pin TSSOP



Block Diagram

DESCRIPTION

The AD8322 is a low cost digitally controlled variable gain amplifier optimized for coaxial line driving applications such as cable modems that are designed to the MCNS-DOCSIS upstream standard. A 8-bit serial word determines the desired output gain over a 42 dB range resulting in gain changes of 6 dB/LSB.

The AD8322 comprises a digitally controlled variable attenuator of +28 dB to -14 dB which is preceded by a low noise, fixed gain buffer and is followed by a low distortion high power amplifier. When used in a DOCSIS modem application the AD8322 works with the attenuator available on some demodulators to support the 50dB range required by DOCSIS. The AD8322 accepts a differential or single-ended input signal. The output is specified for driving a 75Ω load, such as coaxial cable, although the AD8322 is capable of driving other loads.

Distortion performance of -56 dBc is achieved with an output level up to 11dBm at 42 Mhz bandwidth. The very low distortion of the AD8322 results from the ability to maintain a constant 75Ω output impedance during power-up and power-down conditions, eliminating the need for external 75Ω termination resulting in twice the effective output voltage when compared to a standard operational amplifiers. The differential output of the AD8322 results in low glitch output during power-down and power-up transitions, eliminating the need for an external switch.

The AD8322 is packaged in a low cost 28-pin TSSOP, operates from a single +5V supply and has an operational temperature range of -40°C to +85°C.

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AD8322 Specifications (at V_{CC} = +5V, 75Ω source and load, Z =75Ω through a 1:1 transformer, T_A = 25C, V_{IN} = 110mV_{pp}, (All Gain Codes)

Parameter	Conditions	Specifications Min	Typ	Max	Unit
Input Characteristics					
AC Voltage Range	Output = 11dBm, Max Gain		110		mV_{PP}
Input Noise Spectral Density	Max Gain, f = 10MHz		1.6		nV/√Hz
Noise figure	Max Gain, f= 10MHz		9.1		dB
Input Resistance	Single-ended Differential input		210		Ω
Gain Control Interface					
Gain Range			42		dB
Maximum Gain			28		dB
Minimum Gain			-14		dB
Gain Scaling Factor			6		dB/Step
Gain Accuracy	0C≤ T≤70C		±0.2		dB
Output Characteristics					
Bandwidth (-3dB)	All Gain Codes		180		MHz
Bandwidth Rolloff	f= 65MHz		0.5		dB
Output Noise Spectral Density	Max Gain, f = 10MHz		40		nV/√Hz
	Min Gain, f = 10MHz		11		nV/√Hz
	Power-down		1.4		nV/√Hz
1dB compression Point	@ 10MHz		TBD		dBm
Output Impedance	Power Up and Power Down		75		Ω
Maximum Load Capacitance			TBD		pF
Powerdown Pedestal Offset	Min Gain, V_{IN} = 0		±3		mV
Overall Performance					
Worst Harmonic Distortion	f = 21MHz, POUT =11.25 dBm (60dBmV)		-58		dB
	f = 42MHz, POUT = 11.25dBm (60dBmV)		-56		dBc
	f = 65MHz, POUT = 11.25dBm (60dBmV)		-52		dBc
Output Settling to 1mV					
Gain change @ TDATEN =1	Min to Max, V_{IN} = 0V		TBD		ns
Input Change	Max Gain, V_{IN} = 140m Step		TBD		ns
Power Control					
Powerdown Settling time to 1mV	Max Gain, V_{IN} = 0		TBD		ns
Powerup Settling time to 1mV	Max Gain, V_{IN} = 0		TBD		ns
Power Supply					
Specified Operating Range		4.75	5.0	5.25	V
Quiescent Current	Power Up, V_{CC} = 5V		110	122	mA
Quiescent Current	Power Down, V_{CC} = 5V		54	66	mA

LOGIC INPUTS (TTL/CMOS Logic)

(DATEN, CLK, SDATA, V_{CC} = +5 V; Full Temperature Range)

Parameter	Min	Typ	Max	Units
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, DATEN	0		20	n A
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, DATEN	–600		–100	n A
Logic "1" Current (V_{INH} = 5 V) PD	50		190	µ A
Logic "0" Current (V_{INL} = 0 V) PD	–250		–30	µ A

TIMING REQUIREMENTS

(Full Temperature Range, V_{CC} = +5 V, T_R = T_F = 4 ns, f_{CLK} = 8 MHz unless otherwise noted)

Parameter	Min	Typ	Max	Units
Clock Pulsewidth (T_{WH})	16.0			n s
Clock Period (T_C)	32.0			n s
Setup Time SDATA vs. Clock (T_{DS})	5.0			n s
Setup Time DATEN vs. Clock (T_{ES})	15.0			n s
Hold Time SDATA vs. Clock (T_{DH})	5.0			n s
Hold Time DATEN vs. Clock (T_{EH})	3.0			n s
Input Rise and Fall Times, SDATA, DATEN, Clock (T_R, T_F)			10	n s

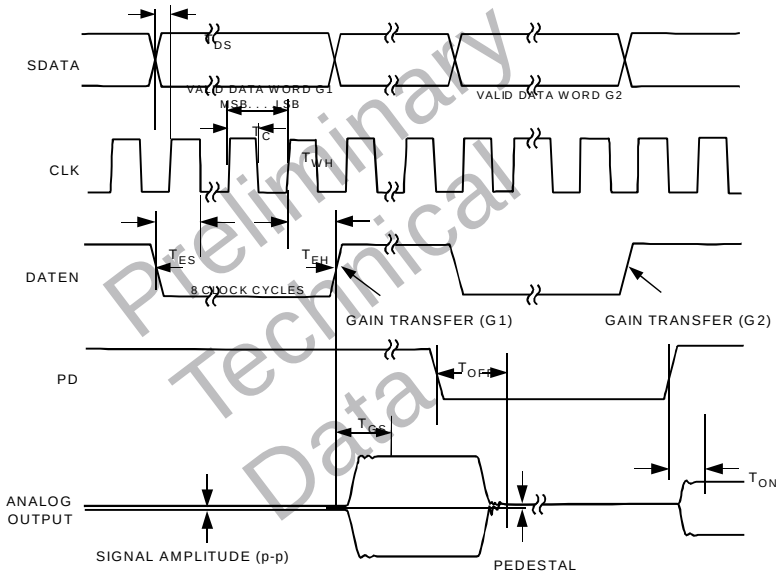


Figure 2. Serial Interface Timing

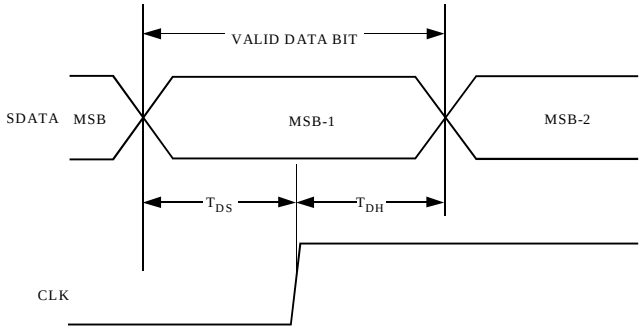
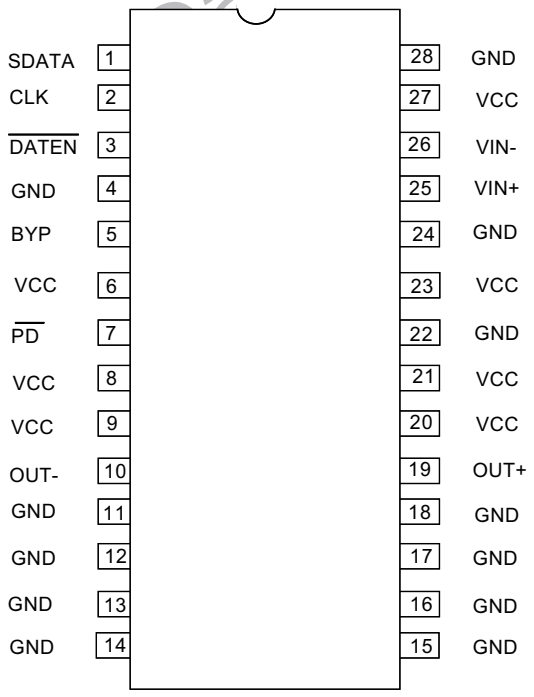


Figure 3. SDATA Timing

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
2	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
3	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhib-its serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
4, 11, 12, 13, 14, 15, 16, 17, 18, 22, 24,28	GND	Common External Ground Reference
5	BYP	Internal Bypass. This pin must be externally ac-decoupled (p.1µF cap).
6, 8, 9, 20, 21, 23, 27	VCC	Common Positive External Supply Voltage. A 0.1uF capacitor must decouple each pin. The 8/9 (and 20/21) pair may share one 0.1uF capacitor.
7	$\overline{\text{PD}}$	Logic “0” powers the part down. Logic “1” powers the part up to its normal operating mimimum code.
10	OUT-	Negative Output Signal.
19	OUT+	Positive Output Signal.
25	VIN+	Noninverting Input. DC-biased to approximately $V_{CC}/2$. For single-ended inverting operation, use 0.1µF decoupling capacitor between VIN- and ground.
26	VIN-	Inverting Input. DC-biased to approximate;ly $V_{CC}/2$. For single-ended inverting operation, use 0.1µF decoupling capacitor between VIN+ and ground.



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm.)

28-Pin TSSOP