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+5V CATV Line Driver
Fine Step

Preliminary Technical Data — AD8323

FEATURES

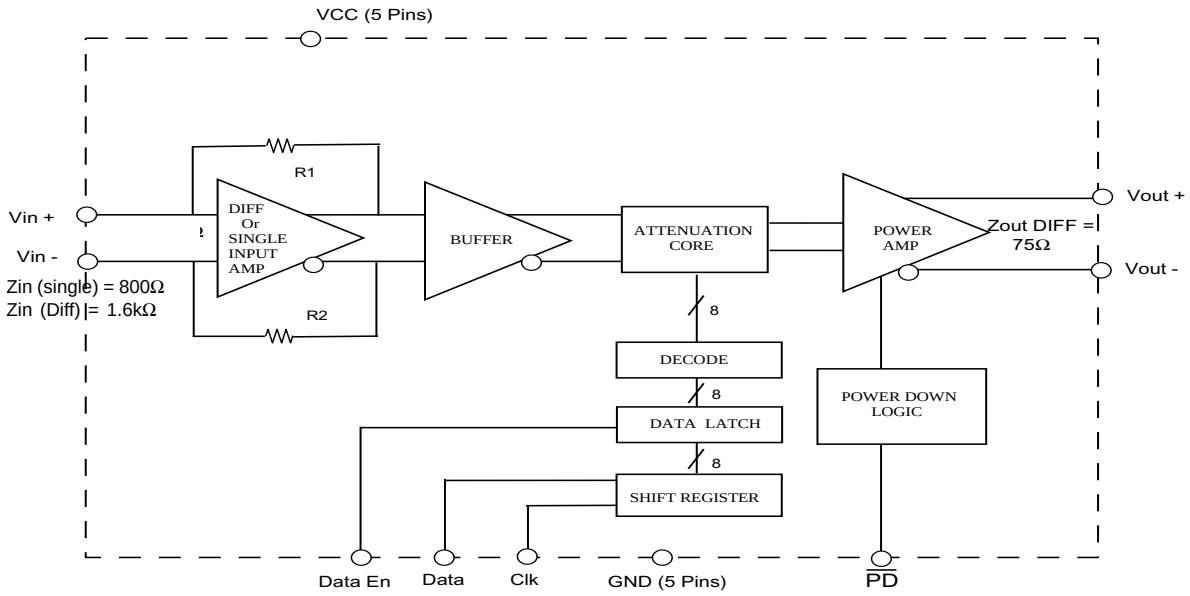
Supports DOCSIS standard for reverse path transmission
Gain Programmable in .75 dB steps over a 53.5 dB Range
Low Distortion at 11dBm output:
  -54 dBc SFDR at 42MHz
  -52 dBc SFDR at 65MHz
12nV/√Hz Output Noise Level
Low Power-up/Power-down Glitch
Maintains 75Ω Output Impedance
  Power up and Power down Condition
Upper Bandwidth: 130 MHz (Full Gain Range)
+5V Supply Operation
Supports SPI and Parallel Control Interfaces
  TTL / CMOS Logic Levels

APPLICATIONS

Gain Programmable Line Driver
  HFC High-speed Data Modems
  Interactive Set-top Boxes
  PC Plug-in Modems
General Purpose Digitally Controlled Variable Gain Block

ORDERING GUIDE

Model	Temperature Range	Package
AD8323ARU	-40°C to +85°C	28-Pin TSSOP



Block Diagram

DESCRIPTION

The AD8323 is a low cost digitally controlled variable gain amplifier optimized for coaxial line driving applications such as cable modems that are designed to the MCNS-DOCSIS upstream standard. A 8-bit serial word determines the desired output gain over a 54 dB range resulting in gain changes of .75 dB/LSB

The AD8323 comprises a digitally controlled variable attenuator of 0 dB to -54 dB which is preceded by a low noise, fixed gain buffer and is followed by a low distortion high power amplifier. The AD8323 accepts a differential or single-ended input signal. The output is specified for driving a 75Ω load, such as coaxial cable, although the AD8323 is capable of driving other loads.

Distortion performance of -56 dBc is achieved with an output level up to 11dBm at 42 Mhz bandwidth. The very low distortion of the AD8323 results from the ability to maintain a constant 75Ω output impedance during power-up and power-down conditions, eliminating the need for external 75Ω termination resulting in twice the effective output voltage when compared to a standard operational amplifiers. The differential output of the AD8323 results in low glitch output during power-down and power-up transitions, eliminating the need for an external switch.

The AD8323 is packaged in a low cost 28 TSSOP, operates from a single +5V supply and has an operational temperature range of -40°C to +85°C.

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AD8323 Specifications (at V_{CC} = +5V, 75Ω source and load, Z =75Ω through a 1:1 transformer, T_A = 25C, V_{IN} = 110mV_{pp}, (All Gain Codes))

Parameter	Conditions	Specifications Min	Typ	Max	Unit
Input Characteristics					
AC Voltage Range	Output = 11dBm, Max Gain		110		mV_{PP}
Input Noise Spectral Density	Max Gain, f = 10MHz		2.8		nV/√Hz
Noise figure	Max Gain, f= 10MHz		13.8		dB
Input Resistance	Single input		800		Ω
	Differential input		1600		Ω
Gain Control Interface					
Gain Range 1.			53.50		dB
Maximum Gain 1.			27.5		dB
Minimum Gain 1.			-26.0		dB
Gain Scaling Factor			0.75		dB/LSB
Gain Accuracy	0C≤ T≤70C		±0.2		dB
Output Characteristics					
Bandwidth (-3dB)	All Gain Codes		115		MHz
Bandwidth Rolloff	f= 65MHz		1.0		dB
Bandwidth Peaking	f= 65MHz		0		dB
Differential Pedestal Offset	Min Gain		±3		mV
Output Noise Spectral Density	Max Gain, f = 10MHz		69		nV/√Hz
	Min Gain, f = 10MHz		12		nV/√Hz
	Power-down		1.4		nV/√Hz
1dB compression Point			TBD		dBm
Differential Output Impedance	Power Up and Power Down	60	75	90	Ω
Maximum Load Capacitance			TBD		pF
Powerdown Pedestal Offset	Min Gain, V_{IN} = 0		±3		mV
Overall Performance					
Worst Harmonic Distortion	f=21MHz, POUT =11dBm		-56		dB
	f = 42MHz, POUT = 11dBm		-54		dBc
	f = 65MHz, POUT = 11dBm		-52		dBc
Output Settling to 1mV					
Gain change @ TDATEN =1	Min to Max, V_{IN} = 0V		TBD		ns
Input Change	Max Gain, V_{IN} = 140m Step		TBD		ns
Power Control					
Powerdown Settling time to 1mV	Max Gain, V_{IN} = 0		TBD		ns
Powerup Settling time to 1mV	Max Gain, V_{IN} = 0		TBD		ns
Power Supply					
Specified Operating Range		4.75	5.0	5.25	V
Quiescent Current	Power Up, V_{CC} = 5V		132	145	mA
	Power-Down		36.2	43.4	mA
	Sleep		4.0	5.3	mA

Note 1. Measured at transformer output, where transformer results in 0.5dB of loss

LOGIC INPUTS (TTL/CMOS Logic) (DATEN, CLK, SDATA, V_{CC} = +5 V: Full Temperature Range)

Parameter	Min	Typ	Max	Units
Logic "1" Voltage	2.1		5.0	V
Logic "0" Voltage	0		0.8	V
Logic "1" Current (V_{INH} = 5 V) CLK, SDATA, DATEN	0		20	n A
Logic "0" Current (V_{INL} = 0 V) CLK, SDATA, DATEN	–600		–100	n A
Logic "1" Current (V_{INH} = 5 V) PD	50		190	µ A
Logic "0" Current (V_{INL} = 0 V) PD	–250		–30	µ A

TIMING REQUIREMENTS (Full Temperature Range, V_{CC} = +5 V, T_R = T_F = 4 ns, f_{CLK} = 8 MHz unless otherwise noted)

Parameter	Min	Typ	Max	Units
Clock Pulsewidth (T_{WH})	16.0			n s
Clock Period (T_C)	32.0			n s
Setup Time SDATA vs. Clock (T_{DS})	5.0			n s
Setup Time DATEN vs. Clock (T_{ES})	15.0			n s
Hold Time SDATA vs. Clock (T_{DH})	5.0			n s
Hold Time DATEN vs. Clock (T_{EH})	3.0			n s
Input Rise and Fall Times, SDATA, DATEN, Clock (T_R, T_F)			10	n s

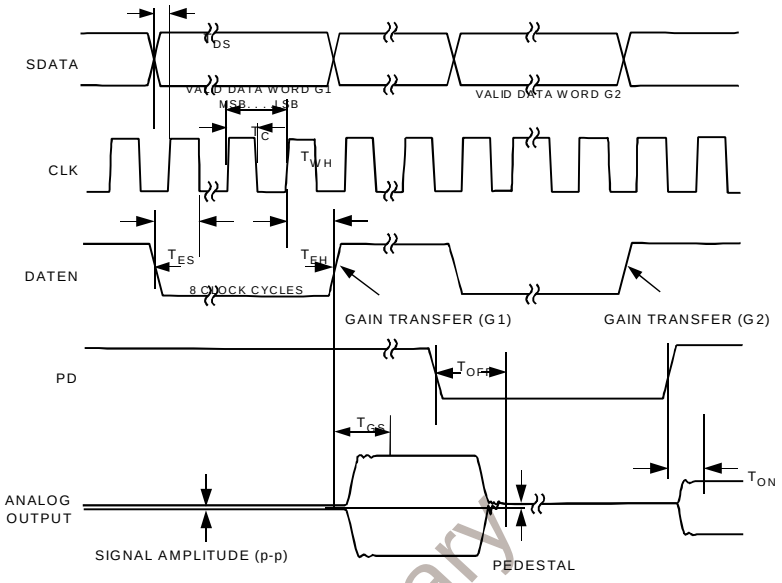


Figure 2. Serial Interface Timing

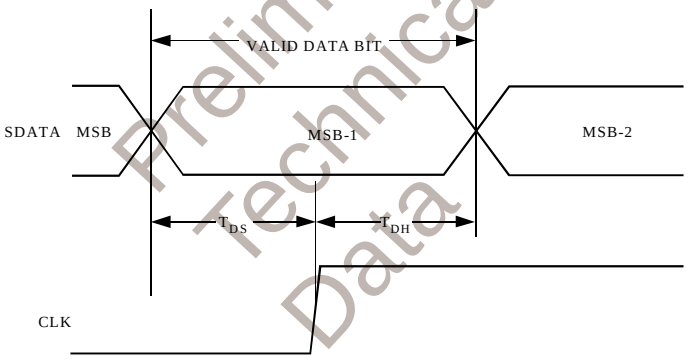
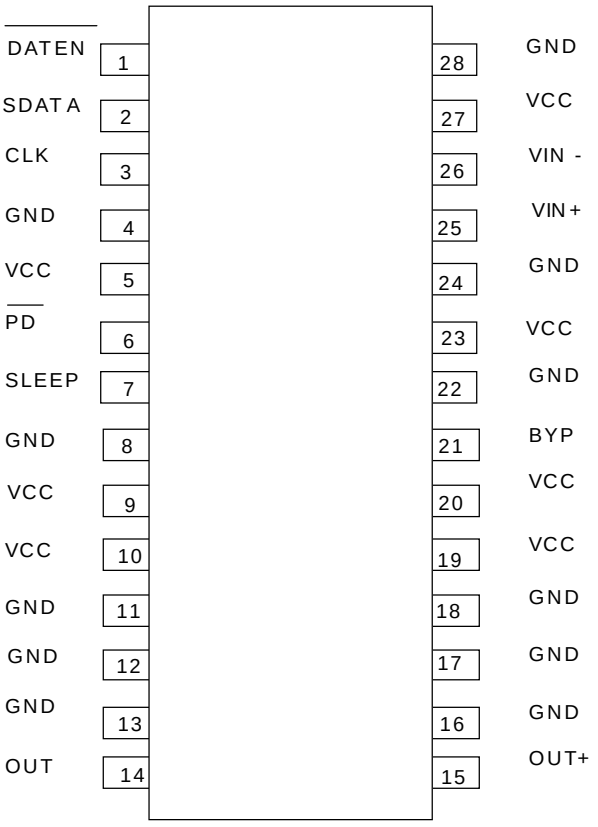


Figure 3. SDATA Timing

PIN FUNCTION DESCRIPTION (Subject to Change)

Pin	Function	Description
1	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A 1-to-0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
2	SDATA	Serial Data Input. This digital input allows for an 8-bit serial (gain) word to be loaded into the internal register with the MSB (most significant bit) first.
3	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-1 transition latches the data bit and a 1-to-0 transfers the data bit to the slave. This requires the input serial data word to be valid at or before this clock transition.
4, 8, 11,12, 13, 16, 17, 18, 22, 24, 28	GND	Common External Ground Reference
5, 9, 10, 19, 20, 23, 27	VCC	Common Positive External Supply Voltage. A 0.1uF capacitor must decouple each pin. The 9/10 (and 19/20) pair may share one 0.1uF capacitor.
6	$\overline{\text{PD}}$	Logic “0” powers the part down. Logic “1” powers the part up.
7	SLEEP	Low power sleep mode. In the Sleep mode, the AD8323’s supply current is reduced to 4.4mA. A Logic “0” powers the part down and a Logic “1” powers the part up.
14	OUT-	Negative Output Signal.
15	OUT+	Positive Output Signal.
21	BYP	Internal Bypass. This pin must be externally ac-coupled (0.1µF cap).
25	VIN+	Noninverting Input. DC-biased to approximately $V_{CC}/2$. For single-ended inverting operation, use a 01.uF decoupling capacitor between VIN+ and ground.
26	VIN-	Inverting Input. DC-biased to approximate;ly $V_{CC}/2$. Should be ac-coupled with a 0.1µF capacitor.



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm.)

28-Pin TSSOP