2.5 GHz True Power Detector

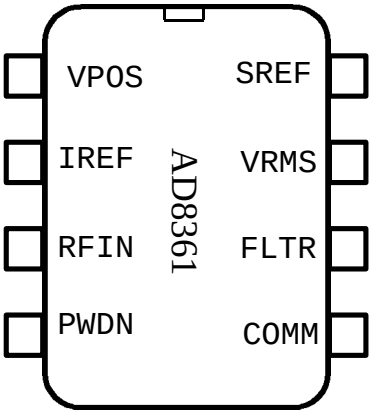
Preliminary Technical Data AD8361

FEATURES

True Power Detection™ IC
RMS-to-DC Conversion
Modulation Independent Response
Excellent Temperature Stability
Greater Than 23 dB Input Range
Linear Response from DC to 2.5GHz
2.7 - 5.5 V Supply Voltage
Rapid Power-down to less than 1 uA
Single-ended Input, 200Ω//1pF

APPLICATIONS

Measurement of CDMA (IS-95) or Other Complex Waveforms
Cellular Base Stations, Power Amplifiers, Radio Links
Transmitter Power Measurement
RSSI



8 Pin Micro-SO Package

PRODUCT DESCRIPTION

The AD8361 is a low power RMS-responding *True Power Detection™* IC for use in high frequency receiver and transmitter signal chains. The device directly measures the RMS or True Power level of signals up to 2.5GHz, covering the required frequency range for cellular telephony, CATV, Wireless LAN and many other applications. It is very easy to apply, requiring only a single supply between 2.7 V and 5.5V, power supply decoupling capacitor and an input coupling capacitor for many applications. The output is linear responding DC output producing a conversion gain of 7.4 V/V_{RMS}. The averaging time constant can be modified by adding an external filter capacitor.

The AD8361 is intended for True Power measurement of simple and complex waveforms. The device is particular useful for measuring high crest factor (high peak-to-average ratio) signals, such as CDMA and W-CDMA. It is also accurate for measurement of most other complex modulation waveforms.

The AD8361 has three output reference modes to accommodate a variety of analog-to-digital converter requirements: 1) ground referenced, 2) internally referenced, offsetting the output 360 mV above ground , and 3) Vpos referenced, offsetting the output to Vpos divided by 7.4.

The AD8361 is specified for operation from -30°C to +85°C and is available in an 8 pin micro-SO package. It is fabricated on an Analog Devices' proprietary high fT silicon bipolar process.

AD8361-SPECIFICATIONS

(Unless otherwise noted, Vs=+3V; T_A=25°C; f_{RF}=900MHz, Ground reference output mode)

Parameter	Condition	Min	Typ	Max	Units
SIGNAL INPUT INTERFACE	(Input RFIN)				
Frequency Range		0.1		2.5	GHz
Maximum Input	Vs=+3V		390		mV_{RMS}
	Equivalent dBM re 50Ω		4.9		dBm
	Vs =+5V		660		mV_{RMS}
Input Impedance			200//1		Ω//pF
RMS Conversion	(Input RFIN to Output VRMS)				
Conversion Gain			7.4		V/V_{RMS}
±0.25dB Error Dynamic Range	CW input		14		dB
±1dB Error Dynamic Range	CW input		23		dB
±2dB Error Dynamic Range	CW input		26		dB
	CW input , Vs=+5V		30		dB
Reference Mode Range reduction	Internal Reference Mode		1		dB
	Supply Reference Mode, Vs=3.0V		1		
	Supply Reference Mode, Vs=5.0V		1.5		
Deviation from CW response	5.5dB Peak to Average Ratio (IS95 reverse link)		0.2		dB
	12dB Pk to Ave Ratio (WCDMA 4 channels)		1.0		dB
	18dB Pk to Ave Ratio (WCDMA 15 channels)		TBD		dB
Large Signal Response Time	No added capacitor on FLTR pin		1		usec
Output Reference	Calculated by a linear regression in linear output range				
Ground Reference Mode (GRM)	0V at SREF, Vs at IREF		0		V
Internal Reference Mode (IRM)	0V at SREF, IREF open		345		mV
Supply Reference Mode (SRM)	0V at SREF and IREF		400		mV
	0V at SREF and IREF, Vs		Vs/7.5		V
ENABLE INTERFACE					
ENBL HI Threshold	+2.7≤Vs≤+5.5V, -40C<T<+85C	Vs-0.5			V
ENBL LO Threshold	+2.7≤Vs≤+5.5V, -40C<T<+85C			0.1	V
Power-up Response Time	2pF at FLTR pin, 227 mV_{RMS} at RFIN		5		uS
	100nF at FLTR pin, 227 mV_{RMS} at RFIN		320		uS
ENBL bias current			<1		uA
POWER SUPPLIES					
Operating Range	-40C<T<-85C	+2.7		+5.5	V
Quiescent Current	200 mV_{RMS} at RFIN, ENBLE input HI		2		mA
	GRM, 0 mV_{RMS} at RFIN, ENBLE input LO		<1		uA
	IRM, 0 mV_{RMS} at RFIN, ENBLE input LO		<1		uA
	SRM, 0 mV_{RMS} at RFIN, ENBLE input LO		9.8*Vs		uA

Absolute Max. Ratings			
Supply Voltage		5.5	V
RF Input Power		TBD	dBm
Operating Temperature	-30	85	Deg. C
Storage Temperature	-65	150	Deg. C

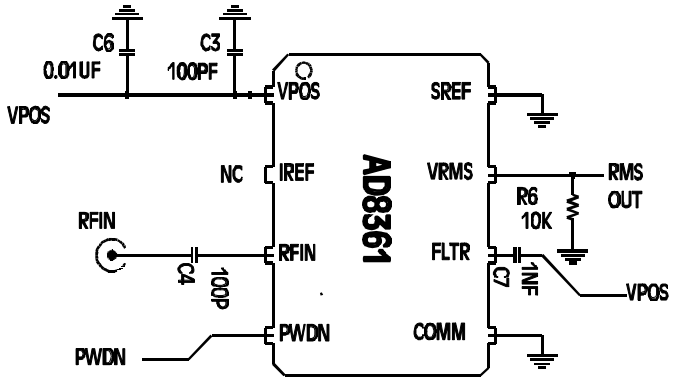
AD8361 Pin Descriptions

PIN	NAME	DESCRIPTION	EQUIVALENT CIRCUIT
1	VPOS	Supply voltage pin operational range 2.7 to 5.5 volts.	
2	IREF	One of the output reference mode enable pin. For internal reference mode this pin is left open. For the other two modes this pin should be tied to VPOS.	
3	RFIN	This is the signal input pin. It must be driven from an AC couples source. The low frequency real input impedance is 200 ohms.	
4	PWDN	This is the power-down mode pin. For the device to operate as a detector it needs a logical low input (less than 100mV). When a logic high (greater than VPOS-0.5volts) is applied the device is turned off and the supply current goes to nearly zero (ground and internal reference mode less than 5uA, supply reference mode Vpos divided by 100K).	
5	COMM	This is the device ground pin.	
6	FLTR	By placing a capacitor between this pin and VPOS, the corner frequency on the modulation filter is lowered. The on-chip filter is formed with 30pF//500 Ohms.	
7	VRMS	This is the output. It is a near-rail-to-rail voltage output with limited current drive capabilities. Expected load 10Kohms or greater.	
8	SREF	The other output reference mode control pin. For supply reference mode this pin must be connected to VPOS. For the other to mode it must be connected to COMM (ground).	

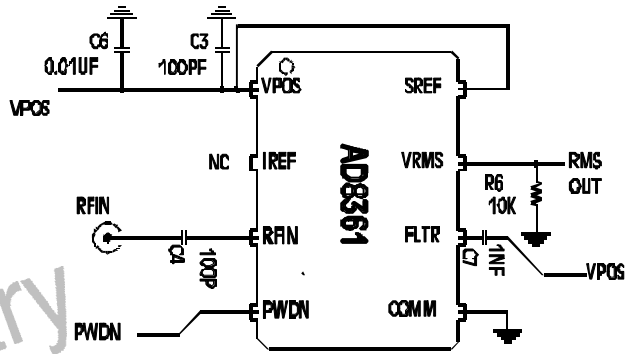
Theory of Application

Although the general operation of the AD8361 is simple, it should be kept in mind it is a linear responding device. The output to input relationship is a conversion gain in volts out per volts RMS in. The resolution decrease and error increase as the signal level decreases as with any linear responding device.

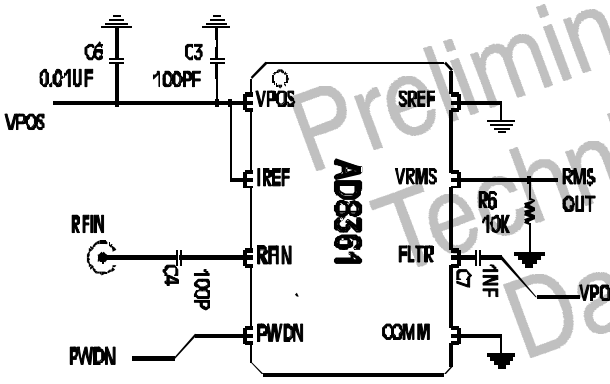
Reference Mode	Control Conditions	
	IREF	SREF
Ground Reference	Vpos	Comm
Internal Reference	Open	Comm
Supply Reference	Vpos	Vpos



Internal Reference Mode



Supply Reference Mode



Ground Reference Mode