10–Bit, 208 MSPS A/D Converter

Preliminary Technical Data 2/25/00 AD9410

The AD9410 is an 10-bit monolithic sampling analog–to–digital converter with an on–chip track–and–hold circuit and is optimized for high speed conversion and ease of use. The product operates at a 208 Msps conversion rate with outstanding dynamic performance over its full operating range.

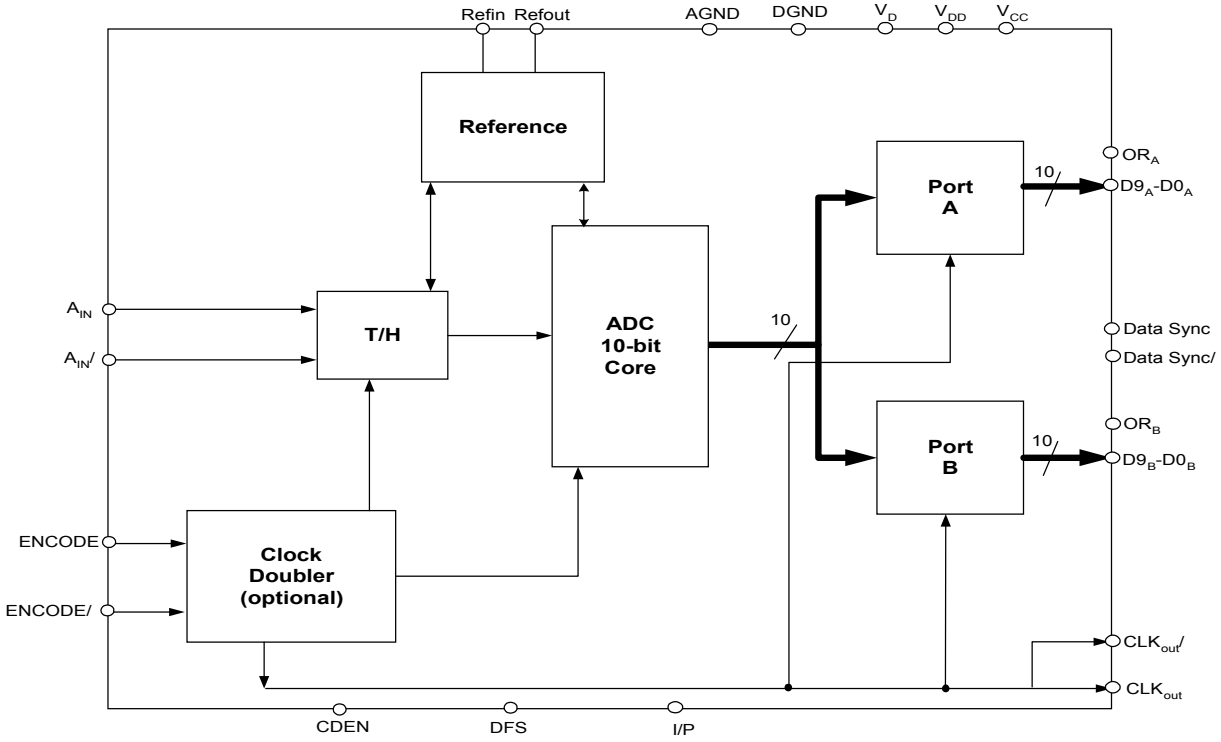
The ADC requires a single 5.0V and 3.3V power supply and up to a 208MHz differential clock input for full–performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3V logic.

The clock input is differential and TTL/CMOS compatible. The 10-bit digital outputs can be operated from +3.3V (2.5V to 3.6V) supplies. An on-chip clock doubler allows up to 208 Msps conversion rates with a 104MHz input clock. Two output buses support demultiplexed data up to 104 Msps rates.

Fabricated on an advanced BiCMOS process, the AD9410 is available in a 80 pin surface mount plastic package (80 Power2 Quad) specified over the industrial temperature range (–40°C to +85°C).

FEATURES
10–Bit, 208Msps ADC
On–Chip Reference and Track/Hold
Selectable on-chip clock doubler
500 MHz Analog Bandwidth
SNR = 54dB with 99MHz analog input
1.5 Vp–p Analog Input Range
+5.0V and +3.3V Supply Operation
+3.3V CMOS/TTL outputs
Power: 1.8 W Typical at 208 Msps
Demultiplexed outputs each at 104 Msps
Output data format option
Data Sync input and Data Clock output provided
Interleaved or parallel data output option.

APPLICATIONS
Communications and Radar
Basestations and 'Zero-IF' subsystems
Wireless Local Loop (WLL)
Local Multipoint Distribution Service (LMDS)
High-End Imaging Systems and projectors



REV. PrB

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AD9410—TARGET SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1] (V_{DD} = 3.0V, V_{CC} = 5.0V; external reference; Clock input = 208 Msps, unless otherwise noted)

Parameter	Temp	Test Level	AD9410BSQ Min	Typical	Max	Units
RESOLUTION				10		bits
DC ACCURACY						
Differential Nonlinearity	+25°C	I		±1.0		LSB
	Full	VI				LSB
Integral Nonlinearity	+25°C	I		±1.0		LSB
	Full	VI				LSB
Gain Error	+25°C	I		±2		% FS
	Full	VI				% FS
Gain Tempco	Full	V		100		ppm/°C
ANALOG INPUT						
Input Voltage Range (with respect to AIN\)	Full	V		±768		mV p–p
Common Mode Voltage	Full	V		3.0		V
Input Offset Voltage	+25°C	I				mV
	Full	I				mV
Reference Voltage	+25°C	I	2.4	2.5	2.6	V
Input Resistance	+25°C	I	700	850	1100	Ω
	Full	I	700	850	1100	Ω
Input Capacitance	+25°C	V		3		pF
Input Bias Current	+25°C	I				µA
	Full	I				µA
Analog Bandwidth, Full Power	+25°C	V		500		MHz
SWITCHING PERFORMANCE						
Maximum Conversion Rate	Full	VI	200			Msps
Minimum Conversion Rate	Full	IV			100	Msps
Encode Pulse Width High (t_{EH})	+25°C	IV				ns
Encode Pulse Width Low (t_{EL})	+25°C	IV				ns
Aperture Delay (t_A)	+25°C	V		0.85		ns
Aperture Uncertainty (Jitter)	+25°C	V		1.0		ps rms
Output Valid Time (t_V)	Full	VI	4.0			ns
Output Propagation Delay (t_{PD})	Full	VI			7.0	ns
Output Rise Time (t_R)	Full	VI		1.8		ns
Output Fall Time (t_F)	Full	VI		1.4		ns
DIGITAL INPUTS						
Logic "1" Voltage	Full	IV				V
Logic "0" Voltage	Full	IV				V
Logic "1" Current	Full	VI			±10	µA
Logic "0" Current	Full	VI			±10	µA
Input Capacitance	+25°C	V		3		pF
DIGITAL OUTPUTS						
Logic "1" Voltage (V_{DD} = +3.3V)	Full	VI	V_{DD}-0.5			V
Logic "0" Voltage (V_{DD} = +3.3V)	Full	VI			0.05	V
Output Coding			Binary or Two's Compliment			
POWER SUPPLY						
Power Dissipation	Full	VI		1.8		W
Power Supply Rejection Ratio (PSRR)	+25°C	I				mV/V

Parameter	Temp	Test Level	AD9410BSQ Min	Typical	Max	Units
DYNAMIC PERFORMANCE						
Transient Response	+25°C	V		tbf		ns
Overvoltage Recovery Time	+25°C	V		tbf		ns
Signal–to–Noise Ratio (SNR) (Without Harmonics)						
f_{IN} = 41 MHz	+25°C	I		55		dB
f_{IN} = 100 MHz	+25°C	I		54		dB
Signal–to–Noise Ratio (SINAD) (With Harmonics)						
f_{IN} = 41 MHz	+25°C	I		54		dB
f_{IN} = 100 MHz	+25°C	I		53		dB
Effective Number of Bits						
f_{IN} = 41 MHz	+25°C	I		8.6		bits
f_{IN} = 100 MHz	+25°C	I		8.5		bits
2nd Harmonic Distortion						
f_{IN} = 41 MHz	+25°C	I		65		dBc
f_{IN} = 100 MHz	+25°C	I		65		dBc
3rd Harmonic Distortion						
f_{IN} = 41 MHz	+25°C	I		65		dBc
f_{IN} = 100 MHz	+25°C	I		65		dBc
Two–Tone Intermod Distortion (IMD)						
f_{IN} = 41 MHz	+25°C	V		58		dBc
f_{IN} = 100 MHz	+25°C	V		58		dBc

NOTES
1. Target Specifications only for product development purposes.
2. On-chip clock doubler supports encode rates from 190Msps to 208Msps, which translates into 95MHz to 104MHz clock input.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9410BSQ	–40°C to +85°C	
AD9410-EVAL	+25°C	Evaluation Board

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EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range.

ABSOLUTE MAXIMUM RATINGS*

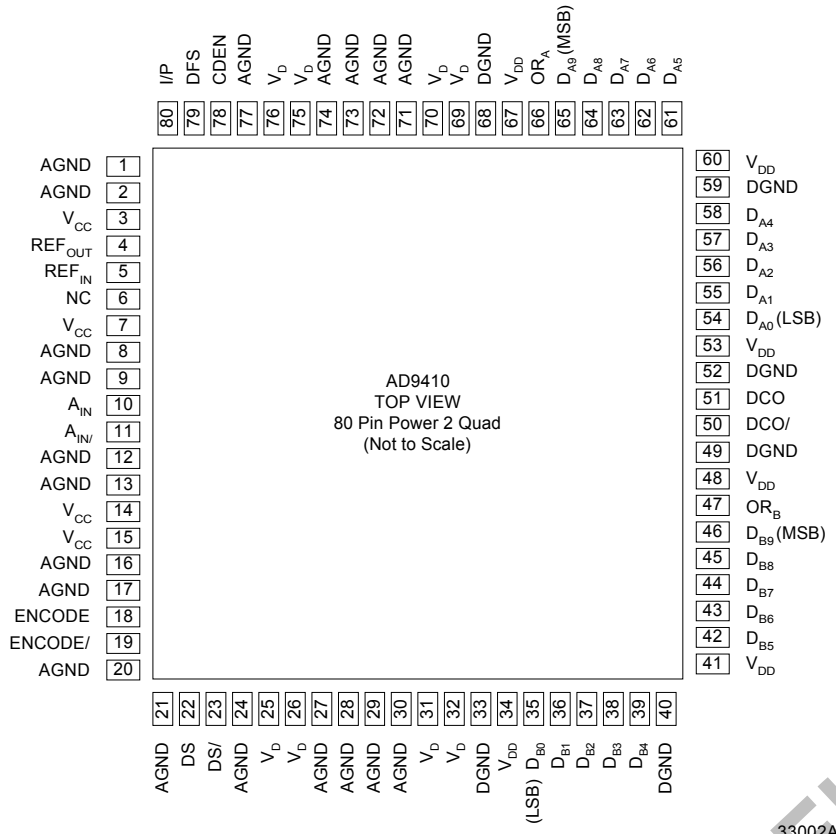
V_D .....+4 V
V_{cc} .....+6 V
V_{DD} .....+4 V
Analog Inputs ..... 0V to V_{CC} + 0.5 V
Digital Inputs ..... 0V to V_{DD} + 0.5 V
VREF IN ..... 0V to V_D + 0.5 V
Digital Output Current ..... 20 mA
Operating Temperature ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin Number	Name	Function
1,2,8,9,12,13,16,17,20,21,24, 27,28,29,30,71,72,73,74,77	AGND	Analog ground.
4	REF_{OUT}	Internal Reference output.
5	REF_{IN}	Internal Reference input.
6	NC	Do not connect.
3,7,14,15	V_{CC}	5V supply. (regulated to within +/- 10%)
10	A_{IN}	Analog input – true.
11	$A_{IN/}$	Analog input – compliment.
18	ENCODE	Clock input – true.
19	ENCODE/	Clock input – compliment.
22	DS	Data sync (input) – true. Aligns output channels so that data from channel B represents a sample that is prior from data in channel A, taking into account the pipeline delay. (See timing diagram). Tie LOW if not used.
23	DS/	Data sync (input) – compliment. Tie HIGH if not used.
25,26,31,32,69,70,75,76	V_D	3.3V analog supply. (regulated to within +/- 5%)
33,40,49,52,59,68	DGND	Digital ground.
34,41,48,53,60,67	V_{DD}	3.3V digital output supply.
35-39	$D_{B0} – D_{B4}$	Digital data output for channel B. (LSB=DB_0)
42-46	$D_{B5} – D_{B9}$	Digital data output for channel B (MSB=DB_9).
47	OR_B	Data over range for channel B.
50	DCO/	Clock output – compliment.
51	DCO	Clock output – true.
54-58	$D_{A0} – D_{A4}$	Digital data output for channel A. (LSB = DA_0)
61-65	$D_{A5} – D_{A9}$	Digital data output for channel A. (MSB=DA_9).
66	OR_A	Data over range for channel A.
78	CDEN	Clock doubler enable. HIGH = Enable, samples at 2X rate when ENCODE = 100Msps +/-5%. LOW = Not enabled
79	DFS	Data format select. HIGH = Two's compliment, LOW = Binary.
80	I/P	Interlaced or parallel output mode. HIGH = data arrives in channel A at falling edge of clock and data arrives in channel B at rising edge of clock (It is recommended to place a 6k ohm resistor between the pin and the HIGH 5V supply.), LOW = data arrives in channels A and B at rising edge of clock.

PIN CONFIGURATION



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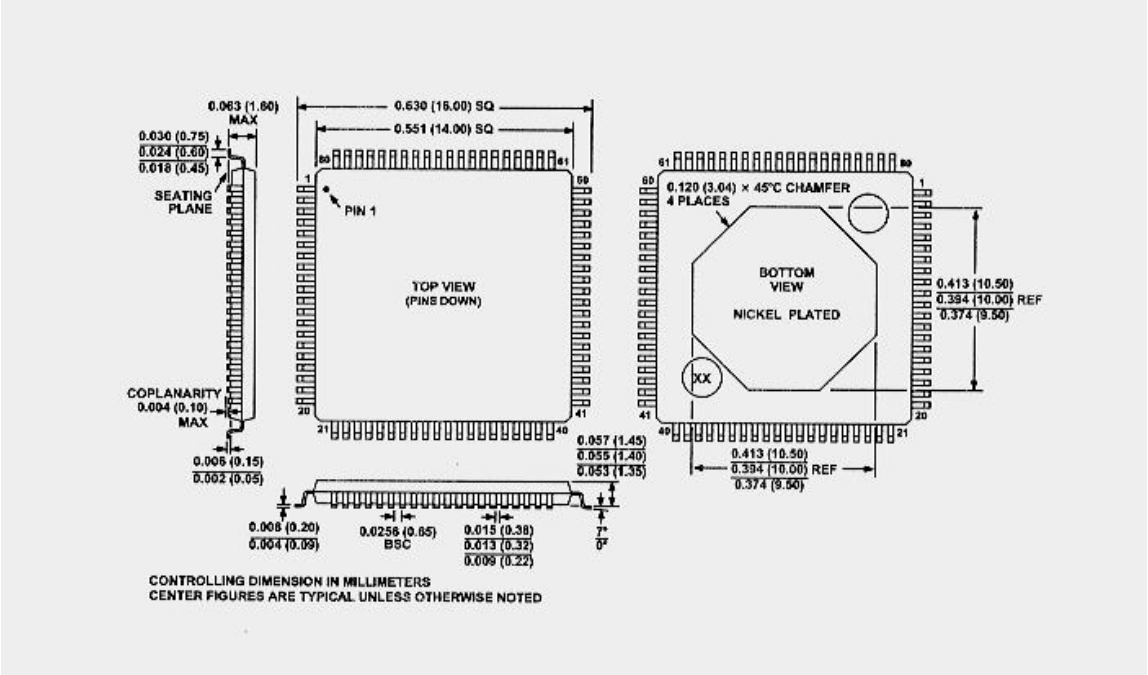
PACKAGE DRAWING - 80 Pin Power2 Quad



Note: It is recommended not to place trace lines underneith for future migration to a lower cost package

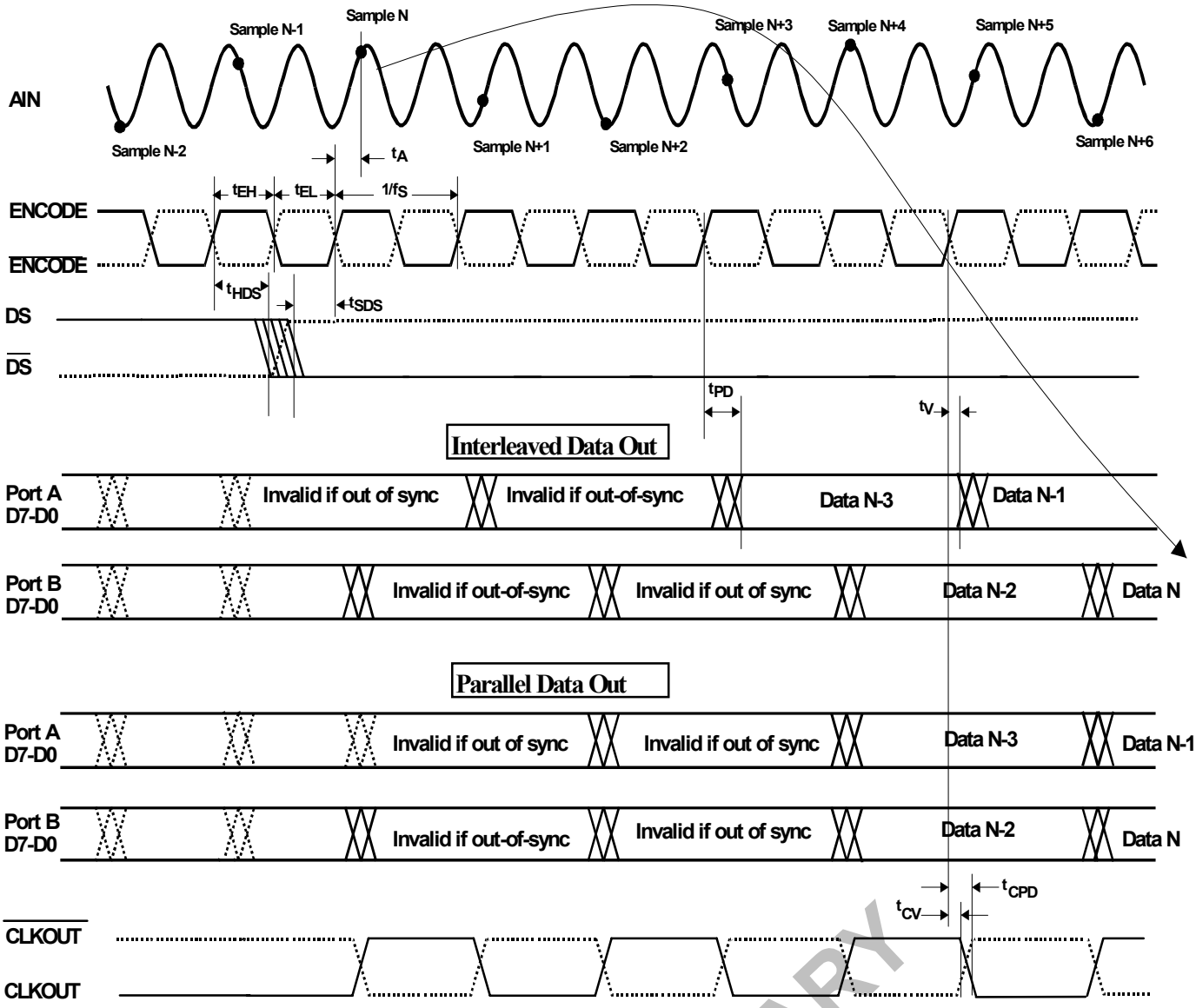


Figure 1. Timing Diagram – Dual Channel Mode with Clock Doubler Disabled.

Erratta

Date	Revision	Changes to Datasheet
2/18/99	R0.3	Removed Pinout and pin desicription. They have changed due to heat dissipation concerns. To be finalized.
4/12/99	R0.4	Added pin out, pin description, pin configuration and package drawing. Updated ordering part number and target AC specifications.
4/30/99	R0.5	Updated package drawing, front page copy and block diagram, page 2 specs, absolute max's, polarity definitions of DFS and I/P switched.
9/16/99	R0.6	Eval board part number, updated package drawing.
2/15/00	R0.7	Changed Pin 6 to do not connect.
2/25/00	R0.8	Updated speed to 208Msps. Noted clock doubler operation window. Changed data sync definition. Inserted timing diagram