CMOS 175 MHz DDS/DAC Synthesizer

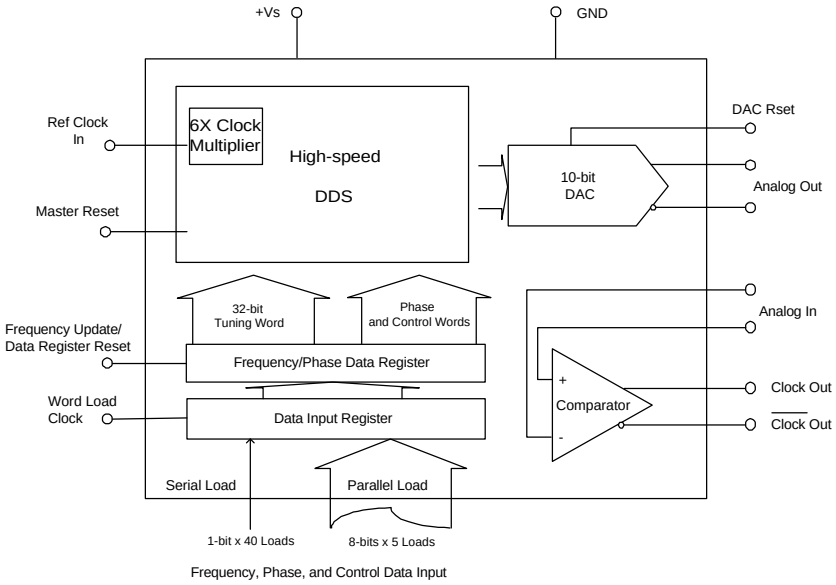
PRELIMINARY TECHNICAL DATA AD9851

FEATURES

175 MHz Clock Rate
6X Internal Reference Clock Multiplier
On-chip High-performance 10-bit DAC & High-speed Comparator
SFDR >48 dB@70 MHz Aout
32-bit Frequency Tuning Word
Simplified Control Interface: Parallel or Serial Loading Format
Phase Modulation Capability
Comparator Jitter <10pS RMS @ 20MHz
+5V or +3.0V Single Supply Operation
Low Power: 400 mW @ 175 MHz
Power-down Function
Ultra-Small 28-pin SSOP Packaging

APPLICATIONS

Frequency/phase-Agile Sinewave Synthesis
Clock Recovery and Locking Circuitry for Digital Communications
Digitally-controlled ADC Encode Generator
Agile L.O. applications in communications
Quadrature oscillator
AM, FM, FSK, MSK mode transmitter



AD9851 FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD9851 is a highly integrated device that uses advanced DDS technology, coupled with an internal high-speed, high performance D/A converter, and comparator, to form a digitally-programmable frequency synthesizer and clock generator function. When referenced to an accurate clock source, the AD9851 generates a stable frequency and phase-programmable digitized analog output sinewave. This sinewave can be used directly as a frequency source, or internally converted to a square wave for agile-clock generator applications. The AD9851's innovative high-speed DDS core provides a 32-bit frequency tuning word, which results in an output tuning resolution of 40 milli-Hertz, for a 175 MHz reference clock. The AD9851 contains a unique X6 reference clock multiplier circuit that obviates the need for a high-speed reference oscillator. The 6X PLL multiplier has minimal impact on SFDR and phase noise characteristics. The device provides 5-bits of digitally-controlled phase modulation which enables phase shifting of its output in increments of 180°, 90°, 45°, 22.5°, 11.25°, and any combination thereof.

The AD9851 contains an improved internal high-speed comparator which can be configured to accept the (externally) filtered output of the DAC to generate a low-jitter output pulse.

The frequency tuning, control, and phase modulation words are loaded into the AD9851 via parallel or serial loading format. The parallel load format consists of five iterative loads of an 8-bit control word (byte). The first 8-bit byte controls output phase, power-down enable, and loading format; bytes 2-5 comprise the 32-bit frequency tuning word. Serial loading is accomplished via a 40-bit serial data stream on a single pin. The AD9851 uses advanced CMOS technology to provide this breakthrough level of functionality on just 550 mW of power dissipation (+5 V supply), at the maximum clock rate of 175 MHz.

The AD9851 is available in a space-saving 28-pin SSOP, surface mount package that is pin-for-pin compatible with the popular AD9850 125 MHz DDS. It is specified to operate over the extended industrial temperature range of -40∞ to +85∞C.

6/12/98

ABSOLUTE MAXIMUM RATINGS[1]

Maximum Junction Temp. .....+165° C
Vs ..... +6 V
Digital Inputs ..... -0.7 V to +Vs
Digital Output Current ..... 5 mA
Storage Temperature ..... -65°C to +150°C
Operating Temp. ..... -40° C to +85° C
Lead Temp. (10 sec. soldering) ..... +300° C

AD9851 ELECTRICAL CHARACTERISTICS (Vs=+5 V ±5 % or +3.0 V ±5 % except as noted, Rset=3.9 kΩ)

Parameter	Temp	Test Level	AD9851BRS Min	AD9851BRS Typ	AD9851BRS Max	Units
CLOCK INPUT CHARACTERISTICS						
Frequency Range						
+5 V Supply	FULL	VI	10		175	MHz
+3.0 V Supply	FULL	VI	10		125	MHz
Duty Cycle	+25°C	I		50		%
Input Capacitance	+25°C	IV		3		pF
Input Impedance	+25°C	IV		100		MΩ
Input Threshhold Voltage						
+5 V Supply	+25°C	IV		TBD		
+3.0 V Supply	+25°C	IV		TBD		
DAC OUTPUT CHARACTERISTICS						
Full Scale Output Current	+25°C	V		10	20	mA
Gain error	+25°C	I	-10		10	%FS
Output Offset	+25°C	I			10	uA
Differential Non-linearity	+25°C	I		.5		lsb
Integral Non-linearity	+25°C	I		.5		lsb
Output Slew Rate	+25°C	IV		400		V/nS
Residual Phase Noise						
PLL On	+25°C	IV		TBD		
PLL Off	+25°C	IV		TBD		
Output Impedance	+25°C	I		120		kΩ
Voltage Compliance Range	+25°C	I			1.5	V
Spurious-free Dynamic Range (SFDR):						
1 MHz Analog Out	+25°C	V		72		dBC
20 MHz Analog Out		V		58		dBC
40 MHz Analog Out		V		54		dBC
70 MHz Analog Out	+25°C	V		48		dBC
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	+25°C	V		3		pF
Input Resistance	+25°C	IV		200		kΩ
Input Bias Current	+25°C	I		25		nA
Input Voltage Range	+25°C	IV	0		3	V
Input Bandwidth	+25°C	IV		TBD		MHz
Input Sensitivity	+25°C	IV		TBD		mV
COMPARATOR OUTPUT CHARACTERISITICS						
Logic "1" voltage +5V supply	FULL	VI	+4.8			V
Logic "1" voltage +3.0V supply	FULL	VI	+3.1			V
Logic "0" voltage	FULL	VI			+0.4	V
Short Circuit Output Current	+25°C	IV		TBD		
Maximum Safe Steady-State Output Current (Voh=)	+25°C	IV		TBD		
Minimum Hysteresis	+25°C	IV	10			mV
Propagation Delay	+25°C	IV,		7		ns
Maximum Toggle Frequency	+25°C	IV		200		MHz
Rise/Fall Time	+25°C	IV		3		ns
Output Jitter (p-p)	+25°C	IV		80		ps

AD9851 ELECTRICAL CHARACTERISTICS (Vs=+5 V ± 5% or +3.0 V ± 5% except as noted, Rset=3.9 kΩ)

Parameter	Temp	Test Level	AD9851BRS Min	Typ	Max	Units
CLOCK OUTPUT CHARACTERISTICS						
Clock Output Duty Cycle	FULL	VI		50±10		%
TIMING CHARACTERISTICS						
t_{wh}, t_{wl} (W_CLK min. pulse width high/low)	+25°C	IV	3.5			ns
t_{ds}, t_{dh} (Data to W_CLK setup and hold times)	+25°C	IV	3.5			ns
t_{fs}, t_{fh} (FQ_UD to REF CLK setup and hold times)	+25°C	IV	3.5			ns
t_{fh}, t_{fl} (FQ_UD min. pulse width high/low)	+25°C	IV	7			ns
t_{rs} (RESET minimum pulse width)	+25°C	IV	5			ns
t_{sr} (RESET to REF CLK setup time)	+25°C	IV	3.5			ns
t_{fd} (FQ_UD min. delay after W_CLK)	+25°C	IV	7			ns
CMOS LOGIC INPUTS						
Logic "1" Voltage, +5V Supply	+25°C	I	3.5			V
Logic "1" Voltage, +3.0V Supply	+25°C	I	3.0			V
Logic "0" Voltage	+25°C	I			0.4	V
Logic "1" Current	+25°C	IV			12	uA
Logic "0" Current	+25°C	IV			12	uA
Minimum Rise/Fall Time	+25°C	IV				
Input Capacitance	+25°C	V		3		pF
POWER SUPPLY						
+Vs Current @:						
62.5MHz Clock, +3.0V Supply	+25°C	I		55		mA
125MHz Clock, +3.0V Supply	+25°C	I		85		mA
175 MHz Clock, 3.0 V Supply	+25°C	I		90		mA
62.5MHz Clock, +5V Supply	+25°C	I		56		mA
125MHz Clock, +5V Supply	+25°C	I		80		mA
175 MHz Clock, +5 V Supply	+25°C	I		100		mA
$P_{DISS@:}$						
62.5MHz Clock, +5V Supply	+25°C	I		280		mW
62.5MHz Clock, +3.0V Supply	+25°C	I		180		mW
125MHz Clock, +5V Supply	+25°C	I		400		mW
125MHz Clock, +3.0V Supply	+25°C	I		280		mW
175 MHz Clock, 3.0 V Supply	+25°C	I		300		mW
175 MHz Clock, +5 V Supply	+25°C	I		500		mW
P_{DISS} Relative to CLK Frequency	+25°C	V		1.6		mW/MHz
P_{DISS} Power-down Mode	+25°C	I		30		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I - 100% Production Tested.

III - Sample Tested Only.

IV - Parameter is guaranteed by design and characterization testing.

V - Parameter is a typical value only.

VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

Table I. AD9851 PIN-FUNCTION DESCRIPTIONS

REFCLK (Pin 9)	Reference clock input. This may be a continuous TTL-level pulse train or sine input biased at +2.5V. The rising edge of this clock initiates operation.
Rset (Pin 12)	This is the DAC's external Rset connection. This resistor value sets the DAC fullscale output current. For normal applications (FS Iout =10mA), the value for Rset is 3.9kΩ connected to ground.
AGND (Pins 10, 19)	Analog Ground. These pins are the ground return for the analog circuitry (DAC and comparator).
DGND (Pins 5, 24)	Digital Ground. These are the ground return pins for the digital circuitry.
VDD (Pins 6, 23)	Supply voltage pins for digital circuitry.
AVCC (Pins 11, 18)	Supply voltage for the analog circuitry (DAC and comparator).
W_CLK (Pin 7)	Word load clock. This clock is used to load the parallel or serial frequency/phase/control words
FQ_UD (Pin 8)	Frequency Update. When this pin is set high, the DDS will update to the frequency (or phase) loaded in the data input register, it then resets the data register.
D0-D7 (Pins 1-4, 25-28)	8-bit Data Input. This is the 8-bit data port for iteratively loading the 32-bit frequency & and 8-bit phase/ control word. D7=MSB; D0=LSB. D7 (Pin 25) also serves as the input pin for the 40-bit serial data word.
RESET (Pin 22)	Reset. This is the master reset pin; when set high it clears all registers and the DAC output will go to Cosine 0 (after additional clock cycles).
IOUT (Pin 21)	The true output of the differential DAC.
IOUTB (Pin 20)	The complementary output of the differential DAC.
DACBP (Pin 17)	DAC Bypass. This is the DAC baseline reference; this pin is internally bypassed and should normally be considered a "no connect" for optimum performance.
VINP (Pin 16)	Voltage input positive. This is the comparator's positive input pin.
VINN (Pin 15)	Voltage input negative. This is the comparator's negative input pin.
VOUTP (Pin 14)	Voltage output positive. This is the comparator's positive output pin.
VOUTN (Pin 13)	Voltage output negative. This is the comparator’s negative output pin.

Figure 1. Pin Function Assignments

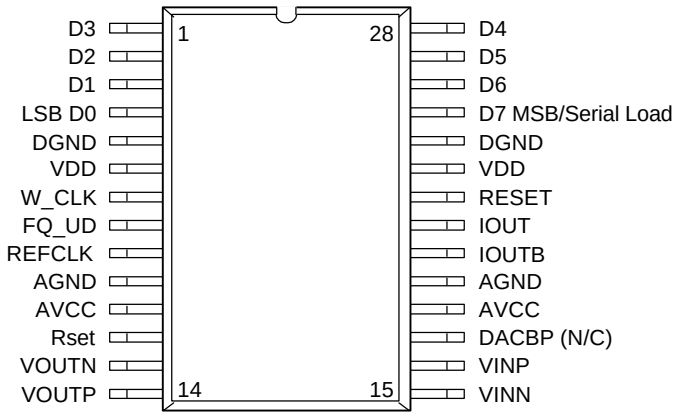


Table II. 8-bit Parallel Control Word Functional Assignment

	data[7]	data[6]	data[5]	data[4]	data[3]	data[2]	data[1]	data[0]
W0	Phase-b0 (MSB)	Phase-b1	Phase-b2	Phase-b3	Phase-b4 (LSB)	Power-down	Logic 0 for factory use only	6X REF CLK enable
W1	Freq -b0 (MSB)	Freq -b1	Freq -b2	Freq -b3	Freq -b4	Freq -b5	Freq -b6	Freq -b7
W2	Freq -b8	Freq -b9	Freq -b10	Freq -b11	Freq -b12	Freq -b13	Freq -b14	Freq -b15
W3	Freq -b16	Freq -b17	Freq -b18	Freq -b19	Freq -b20	Freq -b21	Freq -b22	Freq -b23
W4	Freq -b24	Freq -b25	Freq -b26	Freq -b27	Freq -b28	Freq -b29	Freq -b30	Freq -b31 (LSB)

Table III. 40-bit Serial-load Word Functional Assignment:

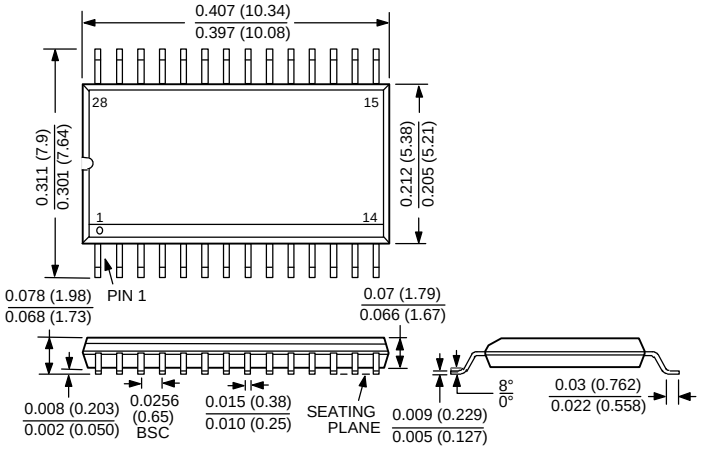
W0	Freq-b31 (LSB)
W1	Freq-b30
W2	Freq-b29
W3	Freq-b28
W4	Freq-b27
W5	Freq-b26
W6	Freq-b25
W7	Freq-b24
W8	Freq-b23
W9	Freq-b22
W10	Freq-b21
W11	Freq-b20
W12	Freq-b19
W13	Freq-b18
W14	Freq-b17

W15	Freq-b16
W16	Freq-b15
W17	Freq-b14
W18	Freq-b13
W19	Freq-b12
W20	Freq-b11
W21	Freq-b10
W22	Freq-b9
W23	Freq-b8
W24	Freq-b7
W25	Freq-b6
W26	Freq-b5
W27	Freq-b4
W28	Freq-b3
W29	Freq-b2

W30	Freq-b1
W31	Freq-b0 (MSB)
W32	6X REFCLK enable
W33	Always logic 0
W34	Power-down
W35	Phase-b0 (LSB)
W36	Phase-b1
W37	Phase-b2
W38	Phase-b3
W39	Phase-b4 (MSB)

Logic High = true
Logic Low = false

Figure 2. Mechanical Diagram
28-pin Shrink Small Outline Package



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