a

CMOS 300 MHz Complete-DDS

PRELIMINARY TECHNICAL DATA

AD9852

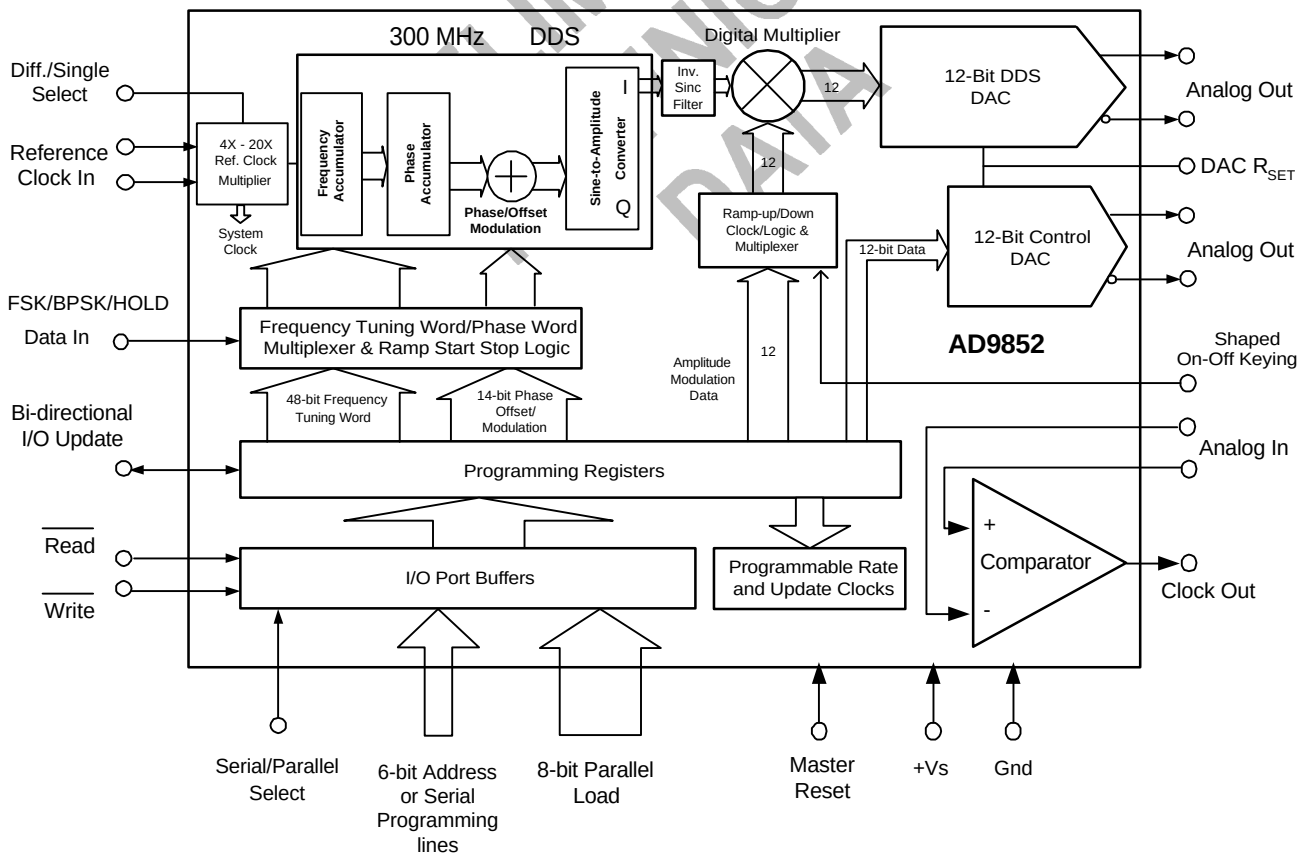
FEATURES

300 MHz Internal Clock Rate
12-bit Sine Wave Output DAC
12-bit Auxiliary or Control DAC
Ultra High-speed, 3ps RMS Jitter Comparator
Excellent Dynamic Performance:
80 dB SFDR @ 100 MHz (±1 MHz) Aout
4× - 20× Programmable Reference Clock Multiplier
Dual 48-bit Programmable Frequency Registers
Dual 14-bit Programmable Phase Offset Registers
12-bit Amplitude Modulation and Programmable Shaped On-Off Keying Function
Single pin FSK and PSK data interface
Linear or Non-Linear FM Chirp Functions with Single Pin Frequency "Hold" Function
Frequency-Ramped FSK
Automatic Bi-directional Frequency Sweep
SIN (X)/X Correction
Simplified Control Interface:
10 MHz Serial, 2 or 3-wire SPI compatible or
100 MHz Parallel 8-Bit Byte Programming
+3.3 V Single Supply
Multiple Power-Down Functions
Single-Ended or Differential Input Reference Clock
Small 80 -pin LQFP Packaging

APPLICATIONS

Agile, L.O. Frequency Synthesis
Programmable Clock Generator
FM Chirp Source for Radar and Scanning Systems
Test and Measurement Equipment
Commercial & Amateur RF exciter

AD9852 Block Diagram

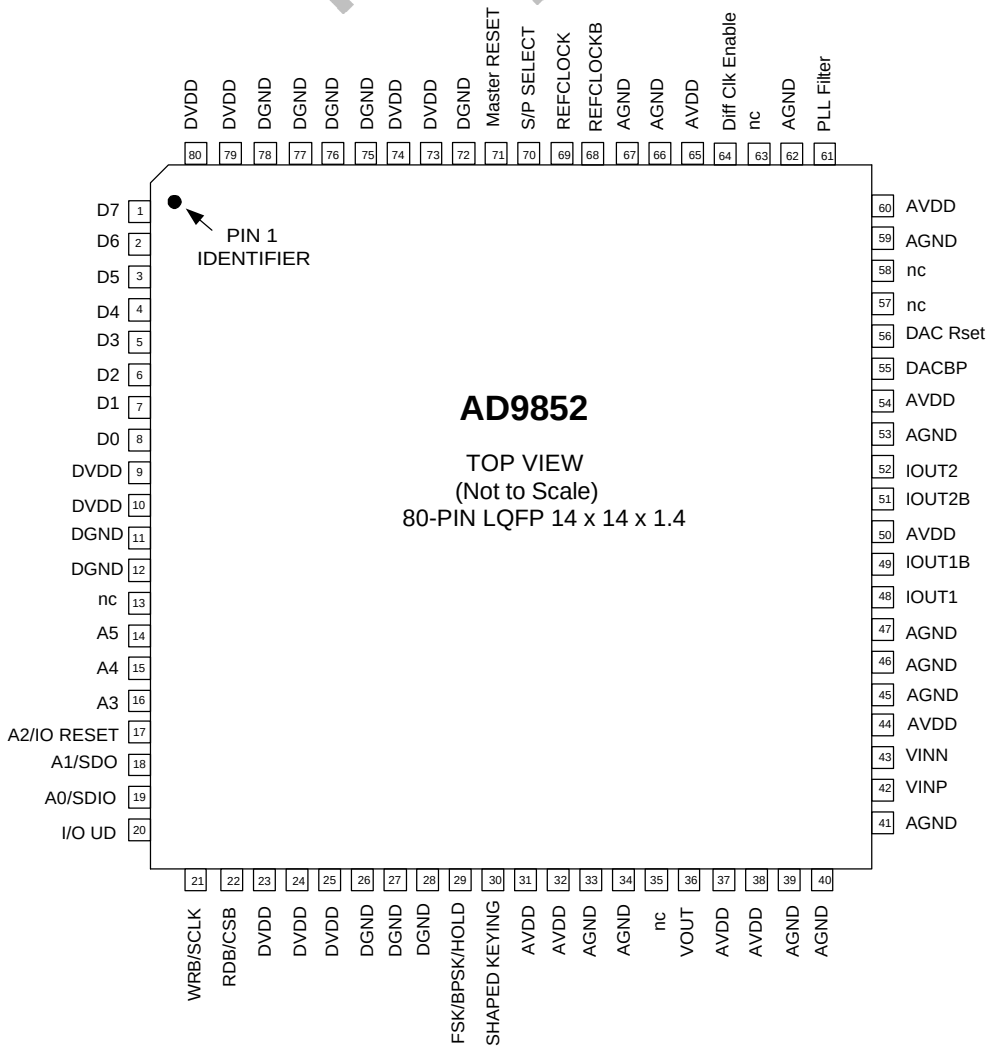


GENERAL DESCRIPTION

The AD9852 digital synthesizer is a highly integrated CMOS device that uses advanced DDS technology, coupled with (2) internal high-speed, high performance D/A converters and comparator to form a digitally-programmable single-tone frequency synthesizer. When referenced to an accurate clock source, the AD9852 generates a highly stable, frequency, phase and amplitude programmable sinewave output that can be used as an agile L.O. in communications, radar, and many other applications. The AD9852's innovative high-speed DDS core provides 48-bit frequency resolution (1 microHertz tuning steps). Phase truncation to 17-bits assures excellent digital SFDR performance. The AD9852's circuit architecture allows the generation of a single-tone output at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The (externally filtered) sine wave output can be converted to a square wave using the internal comparator for agile clock generator applications. The device provides 14-bits of digitally-controlled phase modulation and single-pin PSK. The 12-bit DAC, coupled with the innovative DDS architecture, provide excellent wideband and narrowband analog output SFDR. The 12-bit auxiliary DAC is user-programmable and can accept input data at a 100 MSPS (maximum) rate. When configured with the on-board comparator, the 12-bit control DAC facilitates pulse-width modulation (PWM) and static duty cycle control, in the high-speed clock generator application. A 12-bit digital multiplier permits programmable amplitude modulation of the sine wave output, shaped on-off keying and precise amplitude control. The AD9852's programmable 4× - 20× REFCLK Multiplier circuit generates the 300 MHz (maximum) clock internally from a lower frequency external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz clock source. Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of "ramped" FSK are provided. The AD9852 uses advanced .35 micron CMOS technology to provide this high level of functionality on a single +3.3 V supply.

The AD9852 is available in a space-saving 80-pin LQFP surface mount package. It is pin-for-pin compatible with the AD9854 Quadrature DDS. It is specified to operate over the extended industrial temperature range of -40° to +85°C.

Preliminary Pin Assignments



ABSOLUTE MAXIMUM RATINGS[1]

Maximum Junction Temp. .....+150° C
Vs ..... +4 V
Digital Inputs ..... -0.7 V to +Vs
Digital Output Current ..... 5 mA
Storage Temperature ..... -65° C to +165° C
Operating Temp. ..... -40° C to +85° C
Lead Temp. (10 sec. soldering) ..... +300° C
Maximum Clock Frequency…… TBD MHz

AD9852 PRELIMINARY ELECTRICAL SPECIFICATIONS (V_S=+3.3 V ±5%, R_{SET}=3.9 kΩ, External reference clock frequency = 30 MHz with REFCLK Multiplier enabled at 10×) unless otherwise noted.

Parameter	Temp	Test Level	AD9852 Min	AD9852 Typ	AD9852 Max	Units
REF CLOCK INPUT CHARACTERISTICS[2]						
Internal Clock Frequency Range	FULL	VI	5		300	MHz
External REF Clock Frequency Range:						
REFCLK Multiplier Enabled	FULL	VI	5		75	MHz
REFCLK Multiplier Disabled	FULL	VI	5		300	MHz
Duty Cycle	+25°C	V		50		%
Input Capacitance	+25°C	IV		3		pF
Input Impedance	+25°C	IV		100		MΩ
Common-mode Voltage Range (Differential Mode)	+25°C			TBD		V
V_{IH} (Single-ended Mode)	+25°C			TBD		V
V_{IL} (Single-ended Mode)	+25°C			TBD		V
DAC STATIC OUTPUT CHARACTERISTICS (apply to both DDS and Auxiliary DAC's)						
Output Update Speed	FULL	I			300	MSPS
Resolution	+25°C	IV		12		Bits
Full-Scale Output Current	+25°C	IV	5	10	20	mA
Gain error	+25°C	I	-10		+10	%FS
Output Offset	+25°C	I			10	uA
Differential Non-linearity	+25°C	I		.5		lsb
Integral Non-linearity	+25°C	I		1		lsb
Output Impedance	+25°C	I		100		kΩ
Voltage Compliance Range	+25°C	I	-0.5		+1.0	V
DDS DAC DYNAMIC OUTPUT CHARACTERISTICS						
Wideband SFDR:						
1 to 20 MHz Aout	+25°C	V	TBD	70		dBC
20 to 40 MHz Aout	+25°C	V	TBD	65		dBC
40 to 60 MHz Aout	+25°C	V	TBD	60		dBC
60 to 80 MHz Aout	+25°C	V	TBD	55		dBC
80 to 100 MHz Aout	+25°C	V	TBD	55		dBC
100 to 120 MHz Aout	+25°C	V	TBD	55		dBC
Narrowband SFDR:						
10 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
10 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
10 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
10 MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC
30 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
30 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
30 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
30 MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC
50 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
50 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
50 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
50 MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
70 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC

AD9852 PRELIMINARY ELECTRICAL SPECIFICATIONS (V_S=+3.3 V ±5%, R_{SET}=3.9 kΩ, External reference clock frequency = 30 MHz with REFCLK Multiplier enabled at 10×) unless otherwise noted.

Parameter	Temp	Test Level	AD9852 Min	AD9852 Typ	AD9852 Max	Units
DAC Narrowband SFDR continued:						
90 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
90 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
90 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
90 MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC
110 MHz Aout (± 1 MHz)	+25°C	V	TBD	TBD		dBC
110 MHz Aout (± 250 kHz)	+25°C	V	TBD	TBD		dBC
110 MHz Aout (± 50 kHz)	+25°C	V	TBD	TBD		dBC
11 0MHz Aout (± 10 kHz)	+25°C	V	TBD	TBD		dBC
DDS DAC SIGNAL-TO-NOISE RATIO (calculated)	+25°C			TBD		dB
DDS DAC Residual Phase Noise (Freq TBD)						
1 kHz Offset	+25°C			TBD		dBc/Hz
10 kHz Offset	+25°C			TBD		dBc/Hz
100 kHz Offset	+25°C			TBD		dBc/Hz
Pipeline Delays						
TBD	+25°C			TBD		SysClk Cycles
Phase Accumulator & DSP Algorithm	+25°C			TBD		SysClk Cycles
Inverse Sinc Filter	+25°C			TBD		SysClk Cycles
Digital Multiplier	+25°C			TBD		SysClk Cycles
MASTER RESET DURATION	+25°C		10			SysClk Cycles
DIGITAL (AM) MULTIPLIER DYNAMIC RANGE	+25°C			TBD		dB
COMPARATOR INPUT CHARACTERISTICS						
Input Capacitance	+25°C	V		3		pF
Input Resistance	+25°C	IV		500		kΩ
Input Current	+25°C	I		±12		µA
Hysteresis	+25°C	IV	10			mV
Input Voltage Range	+25°C	IV	0		V_{DD}	V
COMPARATOR OUTPUT CHARACTERISTICS						
Logic "1" voltage, high Z load	FULL	VI	+2.7			V
Logic "0" voltage, high Z load	FULL	VI			+0.4	V
Output Power, 50-ohm load, 100 MHz toggle rate	+25°C	IV		10		dBm
Propagation Delay	+25°C	IV		3		ns
Output Duty Cycle Error[3]	+25°C	IV		±5		%
Rise/Fall Time	+25°C	IV		1		ns
Toggle Rate, high Z load	+25°C	IV		300		MHz
Toggle Rate, 50-ohm load	+25°C	IV		400		MHz
Output Jitter[4]	+25°C	IV		3		ps RMS
COMPARATOR NARROWBAND SFDR[5]						
10 MHz (± 1 MHz)	+25°C	V	TBD	TBD		dBC
10 MHz (± 250 kHz)	+25°C	V	TBD	TBD		dBC
10 MHz (± 50 kHz)	+25°C	V	TBD	TBD		dBC
10 MHz (± 10 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz (± 1 MHz)	+25°C	V	TBD	TBD		dBC
70 MHz (± 250 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz (± 50 kHz)	+25°C	V	TBD	TBD		dBC
70 MHz (± 10 kHz)	+25°C	V	TBD	TBD		dBC
110 MHz (± 1 MHz)	+25°C	V	TBD	TBD		dBC
110 MHz (± 250 kHz)	+25°C	V	TBD	TBD		dBC
110 MHz (± 50 kHz)	+25°C	V	TBD	TBD		dBC
110MHz (± 10 kHz)	+25°C	V	TBD	TBD		dBC
"CLOCK GENERATOR" OUTPUT JITTER[5] @						
5 MHz	+25°C	IV		20		ps RMS

AD9852 PRELIMINARY ELECTRICAL SPECIFICATIONS (V_S=+3.3 V ±5%, R_{SET}=3.9 kΩ, External reference clock frequency = 30 MHz with REFCLK Multiplier enabled at 10×) unless otherwise noted.

10 MHz	+25°C	IV		20	ps RMS
40 MHz	+25°C	IV		20	ps RMS
80 MHz	+25°C	IV		20	ps RMS
120 MHz	+25°C	IV		20	ps RMS
CMOS LOGIC INPUTS					
Logic "1" Voltage	+25°C	I	2.7		V
Logic "0" Voltage	+25°C	I		0.4	V
Logic "1" Current	+25°C	IV		±12	uA
Logic "0" Current	+25°C	IV		±12	uA
Input Capacitance	+25°C	V		3	pF
POWER SUPPLY					
+Vs Current[6]	+25°C	I		1000	mA
+Vs Current[7]	+25°C			600	mA
P_{Diss} [6]	+25°C			3.3	W
P_{Diss} [7]	+25°C			2	W
P_{DISS} Power-down Mode	+25°C	I		10	mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

[2]The reference clock inputs are configured to accept a 1 V p-p (minimum) dc offset sine wave centered at ½ the applied Vdd or a 3 V TTL-level pulse input.

[3] Change in duty cycle from 1 to 100 MHz with 1V p-p sine wave input and .5V threshold.

[4]Represents comparator's inherent jitter contribution. Input signal is a 1 volt, 40 MHz square wave. Measurement device Wavecrest DTS – 2075.

[5]Comparator input originates from DDS section via external 7-pole elliptic LPF. Single-ended input, .5V p-p. Comparator output terminated 50 Ohms.

[6]All functions engaged

[7]All functions except inverse sinc and digital multipliers engaged.

EXPLANATION OF TEST LEVELS

Test Level
- I - 100% Production Tested.
- III - Sample Tested Only.
- IV - Parameter is guaranteed by design and characterization testing.
- V - Parameter is a typical value only.
- VI - All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9852AST			
AD9852ASQ			
AD9852/PCB			

Table I. AD9852 PIN FUNCTION DESCRIPTIONS	
REFCLK	Pin 69. Single-ended reference clock input or one of two differential clock signals. Normal 3.3V CMOS logic levels or 1V p-p sine wave centered about +1.6V.
REFCLKB	Pin 68. The complementary (180 degrees out of phase) differential clock signal. User should tie this pin high or low when single-ended clock mode is selected. Same signal levels as REFCLK above.
DIFF CLK ENABLE	Pin 64. Digital input to select either differential (logic high) or single-ended (logic low) reference clock mode. In the single-ended mode, pin 68 above is switched out of the clock path, and pin 69 assumes total control of the REFCLK function. In differential mode, both pins 68 and 69 work together to provide REFCLK function.
DAC R_{SET}	Pin 56. Common connection for both sine and control DAC's to set the full-scale output current. R_{SET} = 39.9/Iout. Normal R_{SET} range is from 8k (5 mA) to 2k (20 mA).
DACBP	Pin 55. Common by-pass capacitor connection for both DAC's. A .01 μF chip cap from this pin to AVDD improves harmonic distortion and SFDR slightly. No connect is permissible (slight SFDR degradation).
A_{GND}	Pins 33, 34, 39, 40, 41, 45, 46, 47, 53, 59, 62, 66, 67. Connections for analog circuitry ground return. Same potential as D_{GND}
D_{GND}	Pins 11, 12, 26, 27, 28, 72, 75, 76, 77, 78 . Connections for digital circuitry ground return. Same potential as A_{GND}
A_{VDD}	Pins 31, 32, 37, 38, 44, 50, 54, 60, 65. Connections for the analog circuitry supply voltage. Nominally 3.3 volts more positive than A_{GND} and D_{GND}.
D_{VDD}	Pins 9, 10, 23, 24, 25, 73, 74, 79, 80. Connections for the digital circuitry supply voltage. Nominally 3.3 volts more positive than A_{GND} and D_{GND}.
MASTER RESET	Pin 71. Initializes the serial/parallel programming bus to prepare for user programming; sets programming registers to a "do-nothing" state defined by the default values seen in the *Register Layout* table. Active on logic high . Asserting MASTER RESET is essential for proper operation upon power-up.
IOUT1	Pin 48. Unipolar current output of the DDS sine wave output DAC.
IOUT1B	Pin 49. Complementary unipolar current output of the sine wave output DAC.
IOUT2	Pin 52. Unipolar current output of the auxiliary DAC. This DAC can only be programmed to accept external 12-bit data via the parallel or serial interface bus.
IOUT2B	Pin 51. Complementary unipolar current output of the auxiliary or "control" DAC.
VINP	Pin 42. Voltage input positive. The internal high-speed comparator's non-inverting input.
VINN	Pin 43. Voltage input negative. The internal high-speed comparator's inverting input.
VOUT	Pin 36. Internal high-speed comparator's non-inverted output pin. Designed to drive 10 dBm to 50-ohm load as well as standard CMOS logic levels.
nc	Pins 13, 35, 57, 58, 63. No internal connection.
D7 – D0	Pins 1 – 8. 8-bit bi-directional parallel programming data inputs. Used only in Parallel Programming mode.
WRB	Pin 21. Write parallel data to programming registers. Shared function with SCLK below.
RDB	Pin 22. Read parallel data from programming registers. Shared function with CSB below.
A5 – A0	Pins 14 – 19. 6-bit parallel address inputs for Program Registers. Used only in Parallel Programming mode. A0, A1 and A2 have a second function when the Serial Programming mode is selected. See immediately below.
SDIO	Pin 19. Bi-directional serial data input/output for use in 2-wire serial communication mode.
SDO	Pin 18. Uni-directional serial data output for use in 3-wire serial communication mode.
I/O RESET	Pin 17. Allows a RESET of the serial communications bus that is unresponsive due to improper programming protocol. Resetting the serial bus in this manner does not affect previous programming nor does it invoke the "default" programming values seen in the *Register Layout* table. Active HIGH.

Table I. AD9852 PIN FUNCTION DESCRIPTIONS…CONTINUED	
SCLK	Pin 21. Serial clock signal associated with the serial programming bus. Data is registered on the rising edge. This pin is shared with WRB when the parallel mode is selected.
CSB	Pin 22. Chip-select signal associated with the serial programming bus. Active LOW. This pin is shared with RDB when the parallel mode is selected.
S/P SELECT	Pin 70. Selects between Serial Programming mode (logic LOW) and Parallel Programming mode (logic HIGH)
I/O UD	Pin 20. Bi-directional frequency update signal. Direction is selected in Control Register. If selected as an input, a rising edge will transfer the contents of the programming registers to the internal works of the IC for processing. If I/O UD is selected as an output, an output pulse (low to high) of 8 system clock cycle duration indicates that an internal frequency update has occurred.
FSK/BPSK/ HOLD	Pin 29. Multi-function pin according the mode of operation selected in the programming control register. If in the FSK mode logic low selects F1, logic high selects F2. If in the BPSK mode, logic low selects phase 1, logic high selects phase 2. If in the CHIRP mode, logic high engages the HOLD function which will cause the frequency accumulator to halt at its current location. To resume or commence CHIRP, logic low is asserted.
SHAPED KEYING	Pin 30. Must first be selected in the programming control register to function. A logic high will cause the DDS sinewave DAC outputs to ramp-up from zero-scale to full-scale amplitude at a pre-programmed rate. Logic low causes the full-scale output to ramp-down to zero-scale at the pre-programmed rate. This pin has no effect upon the auxiliary DAC.
PLL FILTER	Pin 61. Connection for external series RC loop filter to Vdd. Recommended component values 1.3k and .01μF.

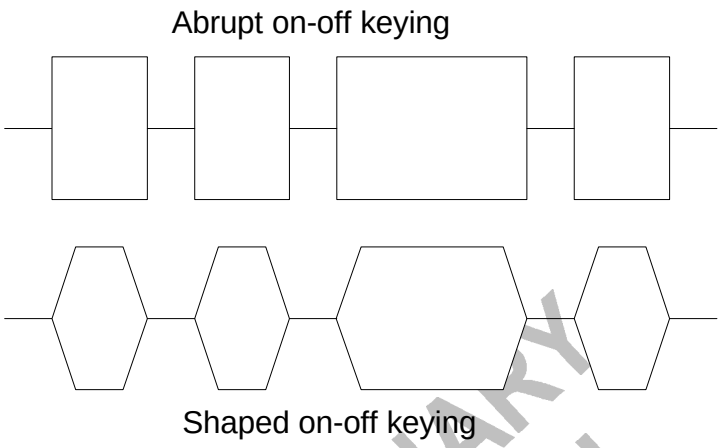
Synthesizer Functional Description

Internal & External Update Clock – This function is comprised of a bi-directional I/O pin, Pin 20, and a programmable 32-bit down-counter. *In order for programming changes to be transferred from the I/O Buffer registers to the active core of the DDS, a clock signal (low to high edge) must be externally supplied to Pin 20 or internally generated by the 32-bit Update Clock.*

An externally generated Update Clock is internally synchronized with the system clock to prevent partial transfer of program register information due to violation of data setup or hold times. This mode gives the user complete control of when updated program information becomes effective. The default mode is set for internal update clock (Int Update Clk control register bit is logic high). To switch to external update clock mode, the Int Update Clk register bit must be set to logic low. The internal update mode generates automatic, periodic update pulses whose time period is set by the user.

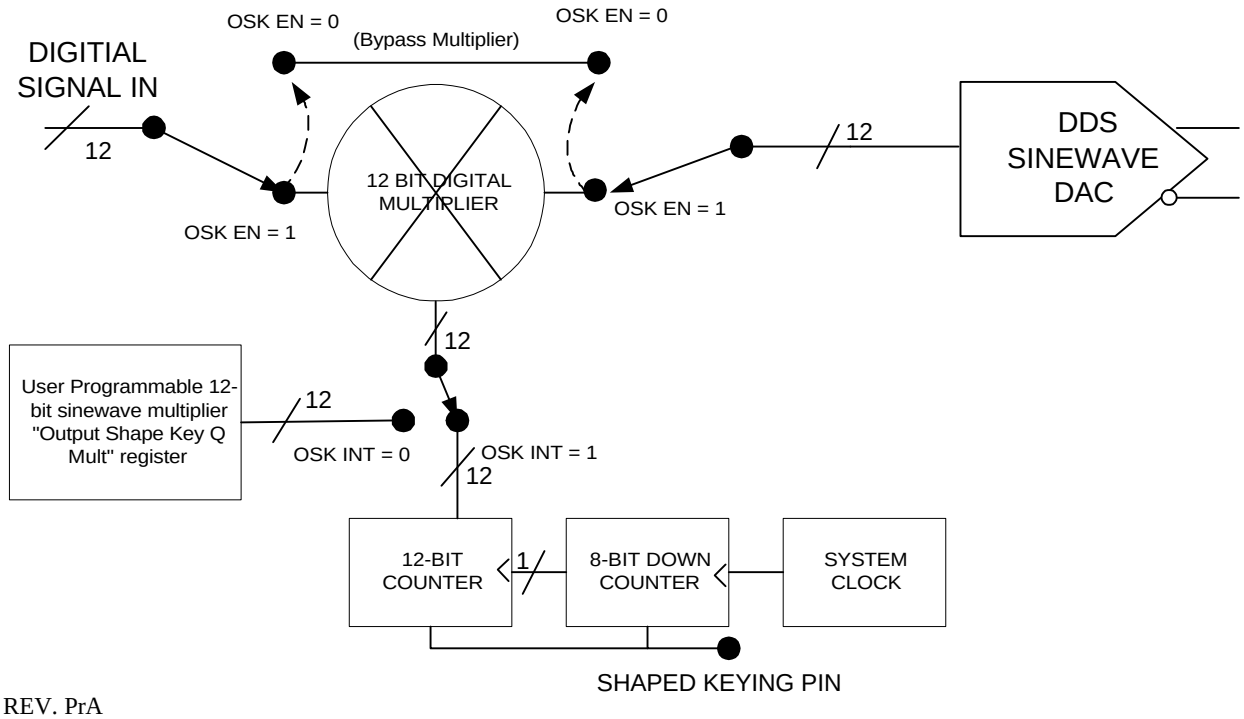
An internally generated Update Clock can be established by programming the **32-bit Update Clock** registers (address 16-19 hex) and setting the **Int Update Clk** (address 1F hex) control register bit to logic high. The update clock down-counter function operates at the system clock/2 (150 MHz maximum) and counts down from a 32-bit binary value (programmed by the user). When the count reaches 0, an automatic I/O Update of the DDS output or functions is generated. The update clock is routed internally and externally on Pin 20 to allow users to synchronize programming of update information with the update clock rate. The time period between update pulses is given as **(N+1) *(SYSTEM CLOCK PERIOD/2),** where N is the 32-bit value programmed by the user. Allowable range of N is from 1 to (2^{32} – 1). The internally generated Update pulse output on Pin 20 has a fixed duration of ten system clock cycles

Shaped On-Off Keying– Allows user to control the ramp-up and ramp-down time of an "on-off" emission from the DDS sine wave DAC. This function is used in "burst transmissions" of digital data to reduce the adverse spectral impact of short, abrupt bursts of data. Users must first enable the digital multipliers by setting the ***OSK EN*** bit (control register address 20 hex) to logic high in the control register. Otherwise, if *OSK EN* bit is set low, the digital multipliers responsible for amplitude-control are by-passed and the I and Q DAC outputs are set to full-scale amplitude.



In addition to setting the *OSK EN* bit, a second control bit, ***OSK INT*** (also at address 20 hex) must be set to logic high. Logic high selects the linear internal control of the output ramp-up or ramp-down function. A logic low in the OSK INT bit switches control of the digital multiplier to user programmable 12-bit register allowing users to dynamically shape the amplitude transition in practically any fashion. This 12-bit register, labeled **"Output Shape Key I**" is located at address's 21 through 22 hex in the register layout table. The maximum output amplitude is a function of the Rset resistor and is not programmable; however, in the OSK INT mode users can program any amplitude between zero and full-scale as the maximum output level.

Next, the transition time from zero-scale to full-scale must be programmed. The transition time is a function of two fixed elements and one variable. The variable element is the programmable 8-bit *RAMP RATE COUNTER.*. This is a down-counter being clocked at the system clock rate (300 MHz max.) that outputs one pulse whenever the counter reaches zero. This pulse is routed to a 12-bit counter that increments one LSB for every pulse received. The outputs of the 12-bit counter are connected to the 12-bit digital multiplier. When the digital multiplier has a value of all zero's at its inputs, the input signal is multiplier by zero, producing zero-scale. When the multiplier has a value of all one's, the input signal is multiplied by a value of 1, producing full-scale. There are 4094 remaining fractional multiplier values that will produce output amplitudes corresponding to their binary values.



Above: Block diagram of sine wave-pathway of the digital multiplier section responsible for Shaped Keying function.

The two fixed elements are the clock period of the system clock (that drives the Ramp Rate Counter) and the 4096 amplitude steps between zero-scale and full-scale. To give an example, assume that the System Clock of the AD9852 is 100 MHz (10 ns period). If the Ramp Rate Counter is programmed for a minimum count of 1, it will take two system clock periods (one rising edge loads the count-down value, the next edge decrements the counter from 1 to zero). The relationship of the 8-bit count-down value to the time period between output pulses is given as: **(N+1) * SYSTEM CLOCK PERIOD**, where N is the 8-bit count-down value. It will take 4096 of these pulses to advance the 12-bit up-counter from zero-scale to full-scale. Therefore, the minimum shaped keying ramp time for a 100 MHz system clock is 4096 * 2 * 10 ns = approximately 82 microseconds. The maximum ramp time will be 4096 * 256 * 10 ns * 4096 = approximately 10.5 msec.

Finally, changing the logic stage of pin 30, "shaped keying" will automatically perform the programmed output envelope functions when OSK INT is high. A logic high on Pin 30 causes the outputs to linearly ramp-up to full-scale amplitude and hold until the logic level is changed to low causing the outputs to ramp-down to zero-scale.

DDS DAC – the 300 MSPS (maximum) sine wave output whose maximum output amplitude is set by the DAC $\mathbf{R_{SET}}$ resistor at pin 56. This is a current-out DAC with a full-scale maximum output of 20 mA; however, a nominal 10 mA output current provides best spurious-free dynamic range (SFDR) performance. The value of R_{SET} = 39.93/Iout, where Iout is in amps. DAC output compliance limits the maximum useable voltage developed at the outputs to -.5 to +1V. Voltages developed beyond this limitation will cause excessive DAC distortion and possibly permanent damage. The user must choose a proper load impedance to limit the output voltage swing to <= compliance limits. Both DAC outputs, true & complement, should be terminated equally for best SFDR, especially at higher output frequencies where harmonic distortion is at its worst.

The DDS DAC is preceded by an inverse SIN (X)/X filter (a.k.a. inverse sinc filter) that pre-compensates for DAC output amplitude variations over frequency to achieve flat amplitude response from dc to Nyquist. A digital multipliers follows the inverse sinc filter to allow amplitude control, amplitude modulation and amplitude shaped keying. The inverse sinc filter (address 20 hex, **Bypass Inv Sinc** bit)) and digital multiplier (address 20 hex, **OSK EN** bit) can be bypassed for power conservation by setting those bits high. Both DACs can be powered-down by setting the **DAC PD** bit high (address 1D of control register) when not needed.

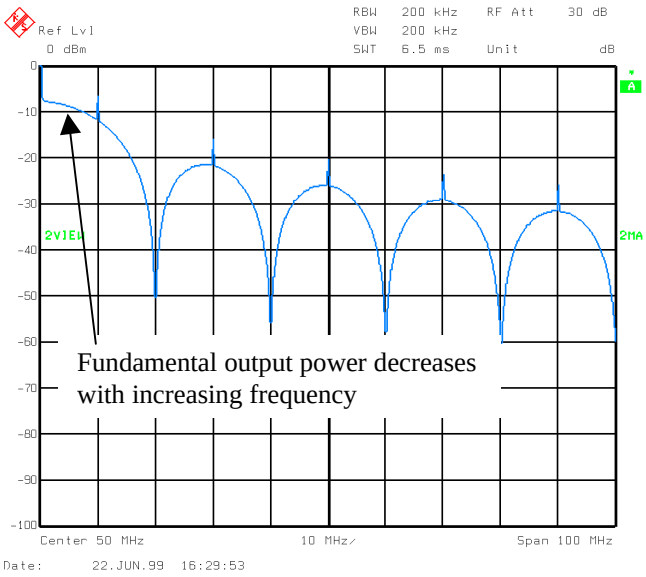
The DDS DAC outputs are designated as IOUT1 and IOUT1B, pins 48 and 49 respectively.

Control DAC –The 12- bit auxiliary or control DAC can provide DC or AC signals to external circuitry, or enable pulse-width modulation (PWM), or duty cycle control, of the on-board comparator when appropriately configured in the clock generator application. 12-bit data is supplied by the user through the serial or parallel interface to the 12-bit **Q DAC** register (address 26 and 27 hex) at 100 MHz (maximum) data rate. The control DAC will be updated with the Q DAC register information any time an internal or external I/O UD pulse is generated or supplied by the user at pin 20. This DAC is clocked at the system clock, 300 MSPS (maximum), and has the same maximum output current capability as that of the sine DAC. The single R_{SET} resistor on the AD9852 sets the full-scale output current for both DACs. The control DAC can be separately powered-down for power conservation when not needed by setting the **Q DAC POWER-DOWN** bit high (address 1D hex).

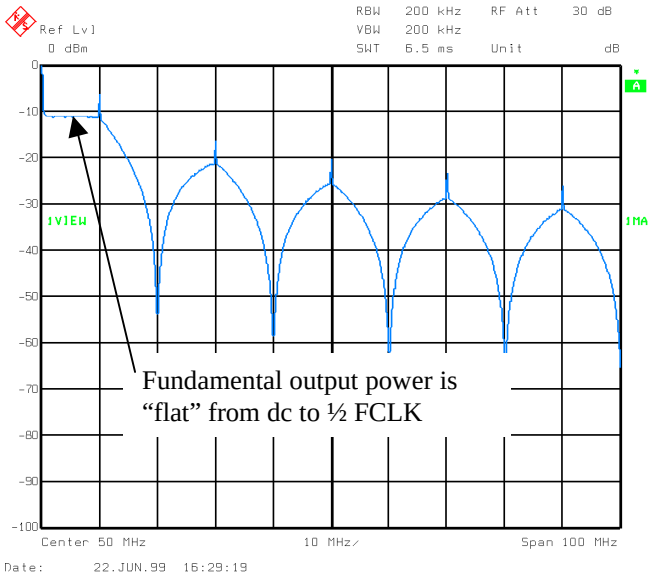
Control DAC outputs are designated as IOUT2 and IOUT2B, pins 52 and 51 respectively.

Inverse SINC function – this filter pre-compensates input data to the sine DAC for the SIN (X)/X roll-off function to allow wide bandwidth signals (such as QPSK) to be output from the sine DAC without appreciable amplitude variations that will cause increased EVM (error vector magnitude). The inverse SINC function may be by-passed to significantly reduce power consumption, especially at higher clock speeds. The control DAC is not equipped with the inverse since function.

Inverse sinc is engaged by default and is bypassed by bringing the "**Bypass Inv Sinc**" bit high in control register 20 (hex) in the Register Layout Table.



Normal Sin x/x power envelope



Inverse Sin x/x (inverse sinc) filter engaged

REFCLK Multiplier – this is a programmable PLL reference clock multiplier that allows the user to select an integer clock multiplying value over the range of 4× to 20× by which the REFCLK input will be multiplied. Use of this function allows users to input as little as 15 MHz to produce a 300 MHz **system clock.** Five bits in control register 1E hex set the multiplier value as follows:

Multiplier Value	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0

The PLL function can be bypassed to allow direct clocking of the AD9852 from an external clock source. The **system clock** for the AD9852 is either the output of the REFCLK Multiplier (if it is engaged) or the REFCLK inputs. REFCLK may be either a single-ended or differential input by setting pin 64, **Diff Clk Enable,** low or high respectively.

A "**PLL Range**" bit in the control register (address 1E hex) allows the VCO "gain" to be increased (logic high) or decreased (logic low). Decreased gain means that the VCO becomes less responsive to changes in control voltage. Increased gain makes the VCO more responsive to changes in control voltage and will increase the VCO frequency range. Any noise on the VCO control voltage line will cause an increase in phase noise of the oscillator. If the VCO gain is increased, then phase noise will increase as well. The default value of this bit is logic high – highest gain – to accommodate a maximum clock speed of 300 MHz. If the system clock is to be less than 200 MHz, it is best to set this bit low for best phase noise performance.

Pin 61. **PLL Filter**, is the connection for an external RC loop filter consisting of a 1.3k resistor in series with a .01 μF capacitor tied to 3.3 volts. The filter is user supplied and must be present for proper REFCLK Multiplier functioning. The filter is connected directly to the PLL phase detector charge pump output stage. Users should exercise care to avoid injecting noise onto this line that controls the VCO output frequency.

When REFCLK multiplier is not needed it can be powered-down by setting the **PLL POWER-DOWN** bit high or by-passed by setting the "**Bypass PLL**" bit high in control register address 1D and 1E (hex) respectively.

Differential REFCLK Enable: Bringing pin 64 high enables the differential clock mode. In this mode, REFCLK and REFCLKB (pins 69 and 68) are assumed to carry clock signals (3.3V CMOS logic levels or 1V p-p dc offset (to ½ Vdd) sine waves) whose phases differ by 180 degrees. Differential clock signals are preferred over single-ended clocking of the AD9854/52.

When pin 64 (Diff Clk Enable) is tied low, REFCLK (pin 69) is the only active clock input. This is referred to as the **single-ended** mode. In this mode, pin 68 (REFCLKB) should be tied low or high but not left floating.

Parallel/Serial programming mode - setting pin 70 high invokes parallel mode, whereas setting pin 70 low will invoke the serial programming mode. Refer to the extensive description of the serial and parallel programming protocol elsewhere in this data sheet.

Two control bits located at address 20 hex in the Register Layout table apply only to the serial programming mode. **LSB First** when high dictates that serial data will be loaded starting with the LSB of the word. When low (the default value) serial data is loaded starting with the MSB of the word. **SDO Active** when high indicates that the SDO pin, Pin 18, is dedicated to reading back data from the AD9852 registers. When SDO Active is low (default value), this indicates that the SDIO pin, Pin 19 acts as a bi-directional serial data input and output pin and Pin 18 has no function in the serial mode.

Modes of Operation – single-tone, FSK, ramped FSK, CHIRP and PSK modes are selected according to three MODE bits in control register 1F (hex) in the Register Layout Table. The following table applies:

M[2]	M[1]	M[0]	FUNCTION INVOKED
0	0	0	Single-tone
0	0	1	Frequency-shift keying (FSK)
0	1	0	Ramped FSK
0	1	1	CHIRP
1	0	0	Phase-shift keying (BPSK)

Each mode will initially use the default conditions that are invoked upon power-up and Master Reset. The default conditions setup a "do-nothing" state at the DAC outputs (0 Hz, 0 degrees phase, minimum amplitude. A brief discussion of each mode, associated programming registers and control bits follows:

Single-Tone Mode: This is the default mode after a master reset. The frequency is determined by the 48-bit Frequency Tuning Word 1 register at address 4 – 9 hex, and the phase is set in 14-bit Phase Adjust Register 1 at address 0-1 hex. Sine wave output DAC amplitude can be adjusted in the 12-bit digital multiplier register located at register address 21&22 hex. Default values of frequency, phase and amplitude are all zero. To set the output amplitudes to full-scale (not adjustable) change the *OSK EN*, address 20 hex, bit to logic low (see amplitude discussion under previous **Shaped Keying** heading).

As with all Analog Devices DDS's, the value of the frequency tuning word is determined

using the following equation: **FTW = (desired output frequency * 2^N)/SYSCLK**. Where N is the phase accumulator resolution (48 bits in this instance), frequency is expressed in Hertz, and the FTW, frequency tuning word, is a decimal number. Once a decimal number has been calculated, it must be converted to binary format – a series of 48 binary-weighted 1's or 0's. The fundamental sine wave DAC output frequency range is from dc to ½ SYSCLK.

Phase adjust Register #2 and Frequency Tuning Word #2 are not accessible in this mode. Pin 29, "FSK, BPSK,HOLD", has no effect.

Changing the value in the Phase Adjust Register 1 as suggested above will change the phase of the sine wave DAC output relative to some other event.

Changes in frequency are phase continuous – that is, the new frequency uses the last phase of the old frequency as a reference point to compute the first new frequency phase step.

FSK Mode: When selected, the output frequency of the DDS is a function of the values loaded into Frequency Tuning Word registers 1 & 2 AND the logic level of Pin 29. A logic low on Pin 29 (FSK/BPSK/HOLD) chooses F1 (frequency tuning word 1, address 4 – 9 hex) and a logic high chooses F2 (frequency tuning word 2, register address A – F hex). Changes in frequency are practically instantaneous and phase continuous. Other than F2 and Pin 29 becoming active, this mode is identical to single-tone.

BPSK Mode: Abbreviation for binary, bi-phase or bipolar-phase-shift-keying. Nearly identical to the FSK mode except P1 (14-bit phase tuning word 1, register address 0 – 1 hex) and P2 (phase tuning word 2, register address 2 – 3 hex) are selected according to the logic state of pin 29. The output frequency is set in frequency tuning word 1 registers. The 14-bit phase values range from all 0's = 0 degrees offset to all 1's = 359.978 degrees offset. The value of 1 LSB is 360/16384 or .022033691 degrees.

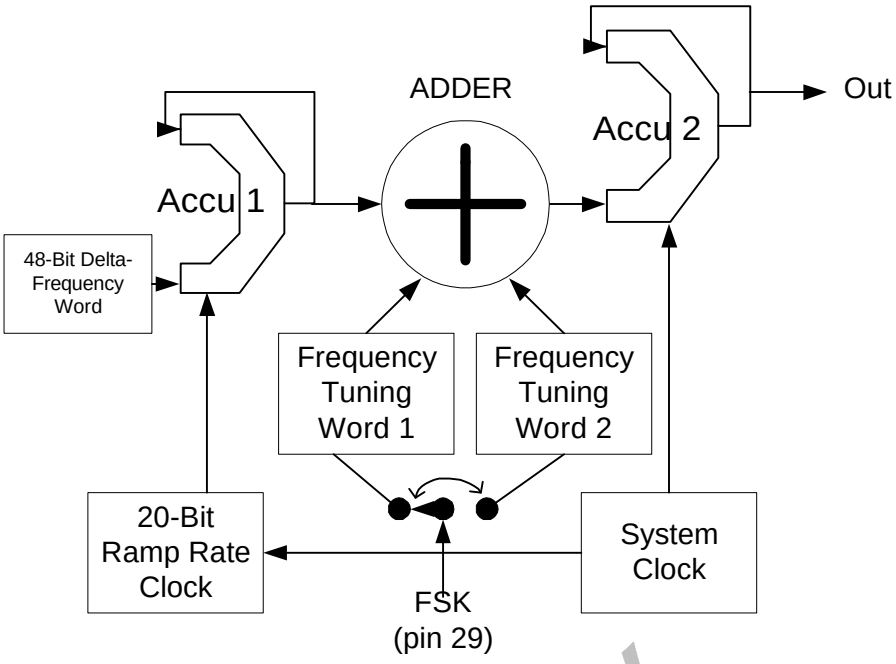
Ramped FSK: A method of FSK whereby changes from F1 to F2 are not instantaneous but instead are accomplished in a frequency sweep or "ramped" fashion. This means that many intermediate frequencies may be output in addition to the primary F1 and F2. The purpose of ramped FSK is to provide better bandwidth containment by "softening" the instantaneous frequency changes with more gradual changes. The dwell time at F1 and F2 can be equal to or much greater than the time spent at each intermediate frequency. The user controls the dwell time at F1 and F2, the number of intermediate frequencies and time spend at each frequency. Unlike unramped FSK, ramped FSK requires the lowest frequency to be loaded into F1 registers and the highest frequency into F2 registers.

Several registers must be programmed to instruct the DDS regarding the resolution of intermediate frequency steps and the time spent at each step.

Register addresses 1A – 1C hex comprise the **Ramp Rate Clock**" register. This is a count-down counter that outputs a pulse whenever the count reaches zero. This counter is being clocked at the System Clock Rate, 300 MHz maximum, and it operates exactly as the 8-bit ramp rate counter described in the previous section labeled "Shaped On-Off Keying". The output of this counter is clocking the **48-bit Frequency Accumulator** shown as "Accu 1" below. The Ramp Rate Clock determines the time spent at each intermediate frequency between F1 and F2. The "dwell time" spent at F1 and F2 is determined by the duration that the FSK input pin, pin 29, is held high or low after the destination frequency has been reached.

Register addresses 10 – 15 hex are for the **48-bit "Delta Frequency Word**". This 48-bit word is accumulated (added to itself) every time it receives a pulse from the ramp rate clock. The output of this accumulator is added to or subtracted from the F1 or F2 frequency

word which is fed to the input of the **48-bit Phase Accumulator** that forms the numerical phase steps for the sine wave output. In this fashion, the output frequency is ramped-up and down according to the state of Pin 29 and the speed at which this happens is a function of the 20-bit ramp rate clock. Once the destination frequency is achieved, the ramp rate clock is stopped and this halts the frequency accumulation process.



The control register contains a **Triangle Bit** at register address 1F. Setting the bit high causes an automatic ramp-up and ramp-down between F1 and F2 without having to toggle Pin 29. This uses the ramp-rate-clock time period and the delta-frequency-word step size to form a continuously sweeping linear ramp from F1 to F2 and back to F1. This is not FSK or ramped FSK; it is simply an easily implemented function that users may find useful for linear frequency sweeping of the DDS output.

To make the linear, ramped FSK mode even more flexible, users can change the 48-bit delta frequency word and/or the 20-bit ramp-rate counter ***on-the-fly*** (during the ramping from F1 to F2). To create **non-linear** frequency changes it is necessary to combine several linear ramps in a **piece-wise** fashion whose slopes are different. This is done by starting a linear ramp at some rate or "slope" and then changing the slope (by changing the ramp rate clock or delta frequency word or both) as often as necessary to form the desired non-linear frequency response before the destination frequency has been reached. These changes can be precisely timed using the **32-bit Internal Update Clock** (see detailed description elsewhere in this data sheet).

Finally, two additional control bits are available to allow even more options. **CLR ACC1**, register address 1F hex, if set high will clear the frequency accumulator (ACC 1) output with a one-shot pulse of one system clock duration. The effect is to interrupt the current ramp, reset the frequency back to the start point, F1, and then continue to ramp up at the previous rate. Next, **CLR ACC2** control bit (register address 1F hex) is available to clear the phase accumulator (ACC 2). When this bit is set high, the output of ACC2 is set to zero resulting in 0 Hz output from the DDS at a phase angle existing just before the CLR ACC2 bit was set to logic high. As long as this bit is set high, the phase

accumulator will be cleared and 0 Hertz will be output. To resume normal DDS operation, CLR ACC2 must be logic low.

FM CHIRP – Allows precise, internally generated linear or non-linear FM over a user defined frequency range, duration, frequency resolution and sweep direction(s). The user programs a start or base frequency into Frequency Tuning Word 1 (register address 4 – 9 hex), the frequency step resolution into the 48-bit Delta Frequency Word (register address 10 – 15 hex) and rate of change into the 20-bit Ramp Rate Clock (Register address 1A – 1C). Chirp stops on a HOLD command, logic high on Pin 29, or when a value of 0 is loaded as a Delta Frequency Word. In this state, the output frequency remains at the frequency just before the halting action was asserted.

Several control bits permit numerous options in the Chirp mode. Any of these options may use either linear or non-linear frequency progression. The control bits that provide these options are: CLR ACC1, CLR ACC2, INT UPDATE CLK, OSK EN, OSK INT. The following is a brief description of what these control bits do:

1) CLR ACC1 control bit causes the output of the 48-bit Frequency Accumulator to be set to zero for one system clock period. The effect is to return the Chirp signal to its origin (F1). This is similar to a re-triggerable one-shot event. As long as CLR ACC1 bit is logic high, a zeroing of the frequency accumulator output will occur on every Update Clock rising edge. After the accumulator has been zeroed, it will resume normal accumulation functions using all-zeros as the beginning point. This bit defaults to logic low, which prevents zeroing of the frequency accumulator from this source.

2) CLR ACC2 control bit causes the output of the 48-bit Phase Accumulator to be zero'ed. This causes the output frequency to go to 0 Hertz as long as this control bit is set to logic high. In addition, this results in a zeroing of the Frequency Accumulator. The condition persists for both accumulators until the CLR ACC2 bit is returned to logic low (default value). Upon return to logic low, the DDS output will return to the frequency programmed into Frequency Tuning Word 1 registers (F1) and the chirp will resume as previously programmed.

3) The UPDATE CLK control bit allows precisely timed Update Clock pulses to be internally generated according to the setting of the 32-bit Update Clock down-counter described on page 6. Between internally generated update clock pulses, the user can write changes to the program registers that will take effect upon receipt of a new update pulse. Pin 20, I/O UD, will be pulsed high for 10 system clock cycles as evidence that an internal update has occurred. This is especially useful for non-linear Chirp where intensive programming of various registers is required.

4) OSK EN and the OSK INT control bits allow users to control the amplitude of the DDS output either directly via the parallel or serial port and automatically using the 8-bit Ramp Rate down-counter and 12 bit up-counter. The registers associated with these control bits and logic states controlling these bits are covered in the "Shaped On-Off Keying" section of this preliminary data sheet.

As with the ramped FSK mode, a non-linear chirp is created by constructing the progression in a piece-wise fashion.

Chirp operation of the AD9852 is less automated than the ramped FSK mode particularly regarding the destination frequency, which is not actually specified in the programming registers. It is incumbent upon the user to know when the destination frequency has been achieved. The value of the 48-bit Delta Frequency Word(s) and the 20-bit Ramp Rate Clock value(s) are all that are needed to calculate when the destination frequency will occur. It is up to the user to determine what occurs when the destination frequency is reached. Here are a few of the choices:

a) Stop and hold at the destination frequency using the HOLD pin, Pin29, or by loading zero into the Frequency Accumulator register of ACC 1. Either method will work.

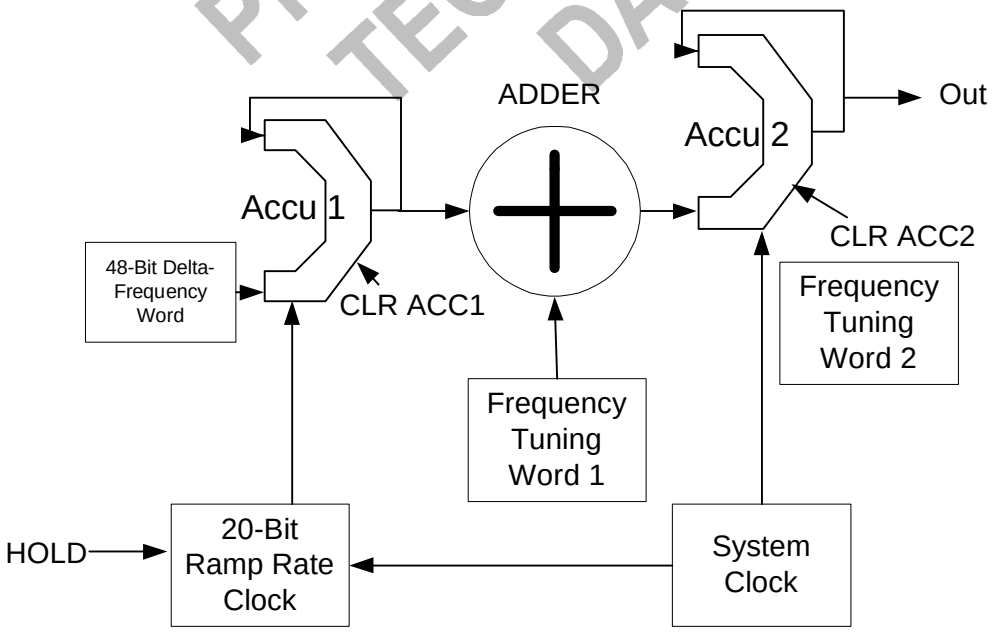
b) Stop, hold and then ramp-down the output amplitude using the digital multiplier stages and the Shaped Keying pin, Pin30, or via program register control (address's 21 – 24 hex).

c) Stop and abruptly terminate the transmission using the CLR ACC 2 bit.

d) Continue chirp by reversing direction and returning to the same or another destination frequency in a linear or user directed manner. If this involves going down in frequency then a negative 48-bit Delta Frequency Word (the MSB is set to "1") must be loaded into registers 10 – 15 hex. Any decreasing frequency step of the Delta Frequency Word requires the MSB to be set to logic high.

e) Continue chirp by immediately returning to the F1 beginning frequency in a saw tooth fashion and repeat the previous chirp process again. This is where CLR ACC1 control bit is used. An automatic chirp can be setup using the 32 bit Update Clock to issue CLR ACC1 commands at precise time intervals.

The figure below shows how the various chirp registers, accumulators, etc. are connected.



I/O Port Buffers – 100 MHz, 8-bit parallel or 10 MHz serial loading, SPI compatible. The programming mode is selected externally via the serial/parallel (S/P Select) pin. I/O Buffers can be written to, or read from, according to the signals supplied to the Read (RDB)and Write pins (WRB) and the 6-bit address (A0 – A5) in the parallel mode or to CSB, SCLK and SDIO pins in the Serial mode. Data in the I/O Port Buffers is stored until overwritten by changes in program instructions supplied by the user or until power is removed. An I/O Update clocks-in the data from the I/O Buffers to the DDS Programming Registers where it is executed.

AM – amplitude modulation of the sine wave DAC is possible using the I/O port to control the 12-bit digital multiplier stage that precedes the DAC. The multiplier can also be used to set the DAC output between zero and full-scale for static amplitude adjustment. See the "Shaped On-Off Keying" description for more information. This function does not apply to the control DAC.

High Speed Comparator – optimized for high speed, > 300 MHz toggle rate, low jitter, sensitive input, built-in hysteresis and an output level of one Volt p-p minimum into 50 ohms or CMOS logic levels into high impedance loads. The comparator can be separately powered-down to conserve power. This comparator is used in "clock generator" applications to square-up a bandpass or lowpass filtered sine wave.

Eight-bit Ramp Rate Clock – when Shaped On-Off Keying is engaged, this down-counter operates at the system clock (300 MHz maximum), and counts down from a user-provided binary value to produce a user-defined clock. The counter outputs one pulse every time the counter counts down to zero. This clock is used to set the rate-of-change of the 12-bit digital multiplier of the sine wave DAC to perform an output envelope shaping function.

Twenty-bit Ramp Rate Clock – when selected, this down-counter operates at the system clock (300 MHz maximum), and counts down from a user-provided binary value to produce a user-defined clock. The counter outputs one pulse every time the counter counts down to zero. This clock is used to set the rate-of-frequency-change of the ramped FSK or FM CHIRP modes.

Forty-eight-bit Delta Frequency Register – is used only in the CHIRP and ramped FSK modes. This register is loaded with a 48-bit word that represents the frequency increment value of the Frequency Accumulator (ACCU 1) whose output will be added to a base frequency that is set in F1 frequency registers. This register is periodically incremented at a rate set by the 20-bit ramp rate clock (150 MHz maximum).

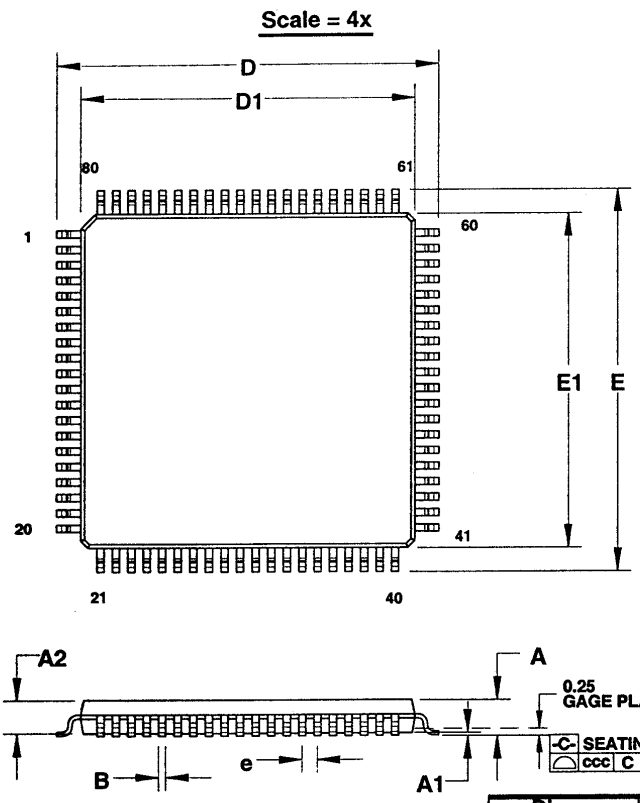
Forty-eight-bit Delta Phase Register – is programmed with a 48-bit Frequency Tuning Word that is input to the 48-bit Phase Accumulator (ACCU 2) and determines the output frequency of the DDS in the single-tone mode. When ramped-FSK or Chirp modes are selected, the contents of this register are summed with the output of ACCU 1 before being input to ACCU 2. Therefore, the signal sent to ACCU 2 may be either static or changing at a rate of up to 150 million 48-bit frequency tuning words per second.

Power-Down - Several individual stages, when not needed, can be powered-down to reduce power consumption via the programming registers while still maintaining functionality of desired stages. These stages are identified in the Register Layout table, address 1D hex. Power-down is achieved by setting the specified bits to logic high. A logic low indicates that the stages are powered-up

Furthermore, and perhaps most significantly, two intensely digital stages, the Inverse Sinc filter and the Digital Multiplier stage can be bypassed to achieve significant power reduction through programming of the control registers in address 20 hex. Again, logic high will cause the stage to be by-passed. Of particular importance is the Inverse Sinc filter. When clocked at the maximum 300 MHz, this single stage consumes nearly .75 watts. If low power consumption is a critical factor then bypassing of the Inverse Sinc filter should be considered.

A full power-down occurs when all five PD Bits in control register 1D hex are set to logic high. This reduces power consumption to approximately 10 mW (3 ma).

Master RESET – logic high active, must be held high for a minimum of 10 system clock cycles. Causes the communications bus to be initialized and loads default values listed in the Register Layout table.



Dim	Min.	Nom.	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
D		16.00 BSC	
D1		14.00 BSC	
E		16.00 BSC	
E1		14.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
B	0.22	0.32	0.38
e		0.65 BSC	
θ	0°	3.5°	7°
θ1	0°		
θ2	11°	12°	13°
θ3	11°	12°	13°
R1	0.08		
R2	0.08		0.20
c	0.09		0.20
S	0.20		
ccc			0.10

NOTES:

1. All Dimensions per JEDEC Standards MO-136-BQ
2. Controlling Dimensions are in mm.

Title: 80 LEAD TQFP
14 x 14 x 1.4 mm
Package Outline
Customer

Above: AD9854 and AD9852 Package dimensions

Parallel Address	Serial Address	AD9854/52 Register Layout								
Hex	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default Value
00 01	0	Phase Adjust Register #1 <13:8> (Bits 15, 14 open) Phase Adjust Register #1 <7:0>						Phase 1		00h
02 03	1	Phase Adjust Register #2 <13:8:> (Bits 15, 14 open) Phase Adjust Register #2 <7:0>						Phase 2		00h
04 05 06 07 08 09	2	Frequency Tuning Word 1 <47:0> Frequency Tuning Word 1 <39:32> Frequency Tuning Word 1 <31:24> Frequency Tuning Word 1 <23:16> Frequency Tuning Word 1 <15:8> Frequency Tuning Word 1 <7:0>							Frequency 1		000000h
0A 0B 0C 0D 0E 0F	3	Frequency Tuning Word 2 <47:40> Frequency Tuning Word 2 <39:32> Frequency Tuning Word 2 <31:24> Frequency Tuning Word 2 <23:16> Frequency Tuning Word 2 <15:8> Frequency Tuning Word 2 <7:0>						Frequency 2		000000h
10 11 12 13 14 15	4	Delta Frequency Word <47:40> Delta Frequency Word <39:32> Delta Frequency Word <31:24> Delta Frequency Word <23:16> Delta Frequency Word <15:8> Delta Frequency Word <7:0>								00000h
16 17 18 19	5	Update Clock <31:24> Update Clock <23:16> Update Clock <15:8> Update Clock <7:0>								64(dec)
1A 1B 1C	6	Ramp Rate Clock <19:16> (Bits 23, 22, 21, 20 open) Ramp Rate Clock <15:8> Ramp Rate Clock <7:0>								000h
1D	7	Open	Open	Open	CompPD	PLL PD	QDAC PD	DAC PD	DIG PD	00h
1E		Open	PLL Range	Bypass PLL	Ref Mult 4	Ref Mult 3	Ref Mult 2	Ref Mult 1	Ref Mult 0	64h
1F		CLR Acc 1	CLR Acc 2	Triangle	SRC QDAC	Mode 2	Mode 1	Mode 0	Int Update Clk	01h
20		Open	Bypass Inv Sinc	OSK EN	OSK INT	Open	Open	LSB First	SDO Active	20h
21 22	8	Output Shape Key 1 Mult <11:8> (Bits 15, 14, 13, 12 open) Output Shape Key 1 Mult <7:0>								000h
23 24	9	Output Shape Key Q Mult <11:8> (Bits 15, 14, 13, 12 open) Output Shape Key Q Mult <7:0>								000h
25	A	Output Shape Key Ramp Rate <7:0>								128(dec)
26 27	B	QDAC <11:8> (Bits 15, 14, 13, 12 open) QDAC <7:0>								00h

Table 1: Register Layout. Shaded bits above comprise the "Control Register"

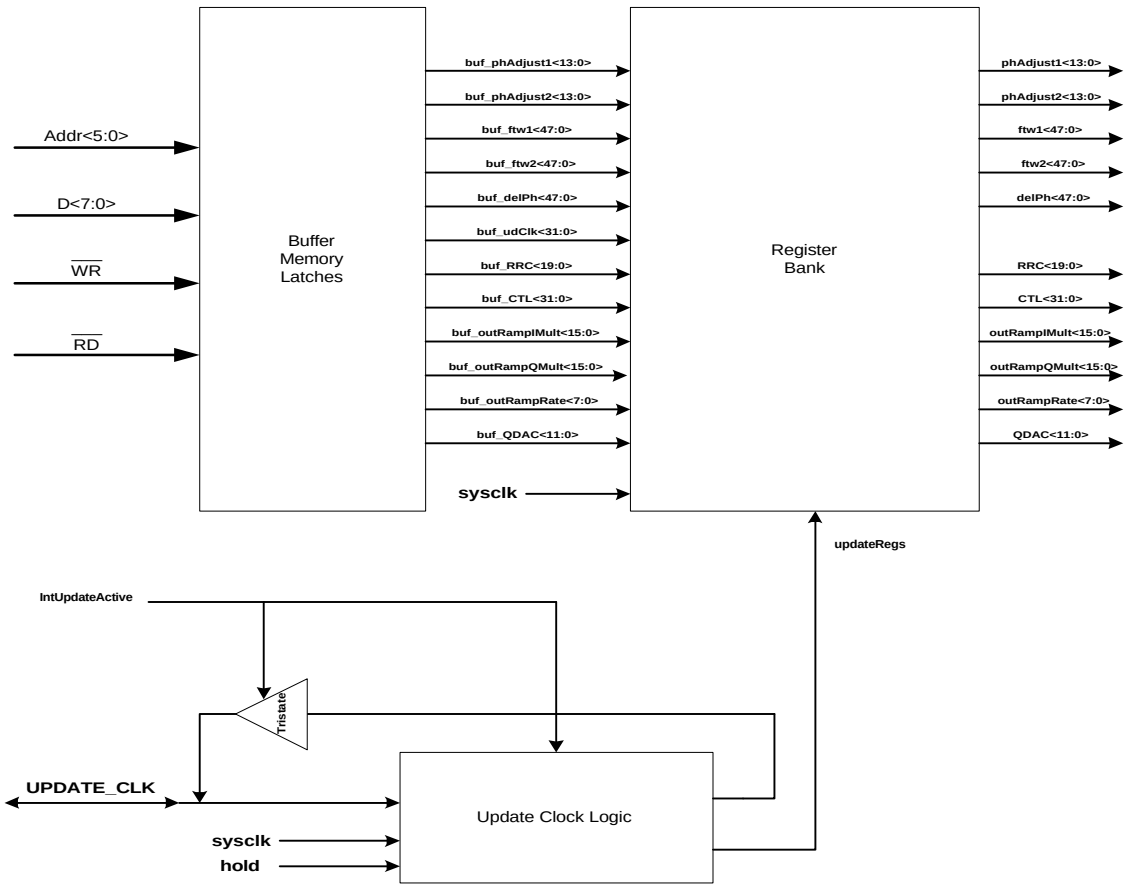
Programming the AD9854/52

The AD9854/52 Register Layout, shown in Table 1, contains the information that programs the chip for the desired functionality. While many applications will require very little programming to configure the AD9854/52, some will make use of all 12 registers that are accessible. The AD9854/52 supports an 8-bit parallel IO operation or a SPI compatible serial IO operation. All registers accessible can be written and read back in either IO operating mode.

An external pin, SPSELECT, is used to configure the IO mode. Systems that use the parallel IO mode must tie the SPSELECT pin to VDD. Systems that operate in the serial IO mode must tie the SPSELECT pin to GND.

Regardless of mode, the IO port data is written to a buffer memory that does NOT affect operation of the part until the contents of the buffer memory is transferred to the register bank. This transfer of information occurs synchronous to the system clock and occurs in one of two ways, 1) internally controlled at a rate programmable by the user or, 2) externally controlled by the user. IO operations can occur in the absence of REFCLK but the data cannot be moved from the buffer memory to the register bank without REFCLK. See the Update Clock Operation section of this document for details.

AD9854/52 IO Port Block Diagram



Parallel IO Operation

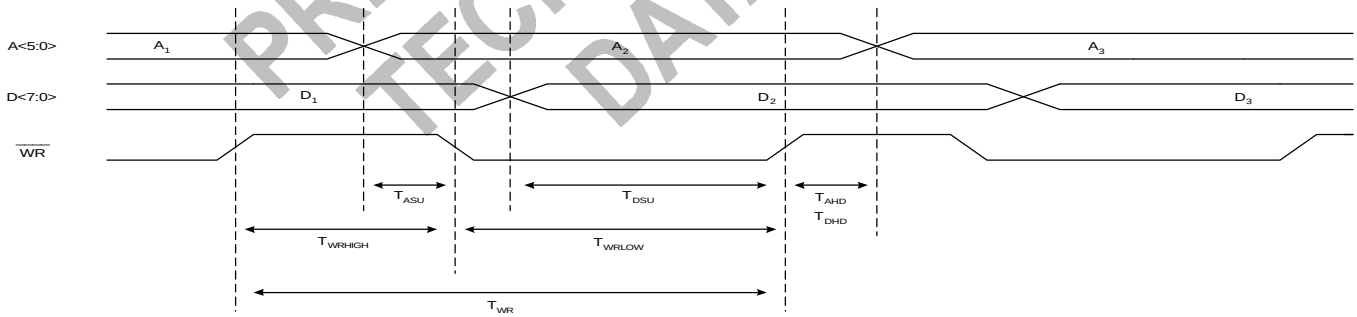
With the SPSELECT pin tied high, the parallel IO mode is active. The IO port is compatible with industry standard DSPs and micro-Controllers. Six address bits, 8 bi-directional data bits and separate write/read control inputs make up the IO port pins (Figure above).

Parallel IO operation allows write access to each byte of any register in a single IO operation at 100Mhz**.** Read back capability for each register is included to ease designing with the AD9854/52. Reads are not guaranteed at 100Mhz as they are intended for software debug only.

Parallel IO operation timing diagrams and are shown in the figures below.

AD9854/52 Parallel Port Write Timing Diagram

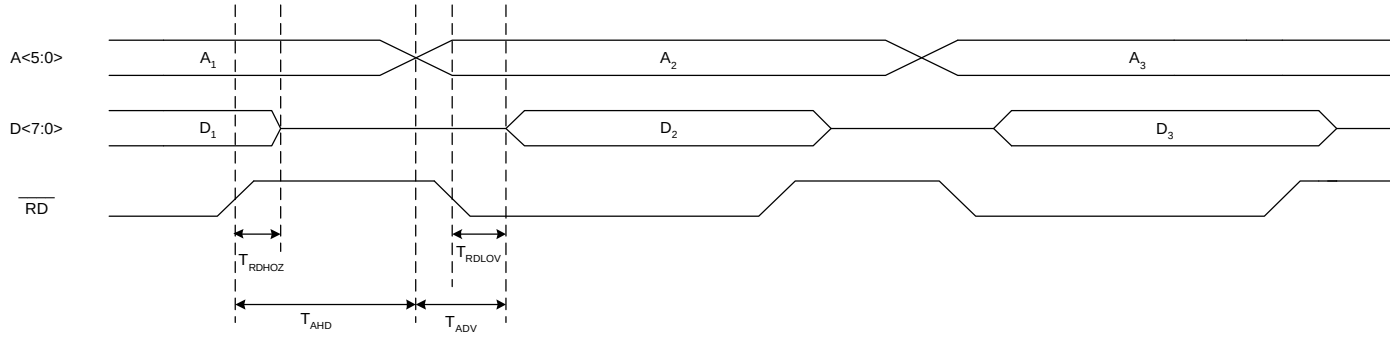
February 22, 1999



Specification	Value	Description
T_{ASU}	~3ns	Address Setup Time To WR Singal Active
T_{DSU}	~3ns	Data Setup Time To WR Signal Inactive
T_{ADH}	~3ns	Address Hold Time To WR Signal Inactive
T_{DHD}	~3ns	Data Hold Time To WR Signal Inactive
T_{WRLOW}	~5ns	WR Signal Minimum Low Time
T_{WRHIGH}	$T_{ASU} + T_{AHD}$	WR Signal Minimum High Time
T_{WR}	$T_{WRLOW} + T_{WRHIGH}$	WR Signal Minimum Period

AD9854/52 Parallel Port Read Timing Diagram

February 22, 1999



Specification	Value	Description
T_{ADV}	tbd	Address To Data Valid Time (maximum)
T_{ADH}	tbd	Address Hold Time To RD Signal Inactive (minimum)
T_{RDLOV}	tbd	RD Low to Output Valid (maximum)
T_{RDHOZ}	tbd	RD High To Data Tristate (maximum)

Serial Port IO Operation

With the SPSELECT pin tied low, the serial IO mode is active. The AD9854/52 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6905/11 SPI and Intel 8051 SSR protocols. The interface allows read/write access to all 12 registers that configure the AD9854/52 and can be configured as a single pin IO (SDIO) or two unidirectional pins for in/out (SDIO/SDO). Data transfers are supported in most significant bit (msb) first format or least significant bit (lsb) first format at up to 10Mhz.

When configured for serial IO operation, most pins from the AD9854/52 parallel port are inactive; some are used for the serial IO. Table x below describes pin requirements for serial IO.

Pin Number	Pin Name	Serial IO Description
1,2,3,4,5,6,7,8	D[7:0]	The parallel data pins are not active, tie to VDD or GND
14,15,16	A[5:3]	The parallel address pins A5, A4, A3 are not active, tie to VDD or GND
17	A2	IORESET
18	A1	SDO
19	A0	SDIO
20	I/O UD	Update Clock. Same functionality for Serial Mode as Parallel Mode
21	WRB	SCLK
22	RDB	CSB – Chip Select

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9854/52. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9854/52, coincident with the first 8 SCLK rising edges. The instruction byte provides the AD9854/52 serial port controller with information regarding the data transfer cycle, which is phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, and the register address in which to transfer data to/from.

The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9854/52. The remaining SCLK edges are for phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9854/52 and the system controller. The number of data bytes transferred in Phase 2 of the communication cycle is a function of the register address. The AD9854/52 internal serial IO controller expects every byte of the register being accessed to be transferred. Table below describes how many bytes must be transferred

Serial Register Address	Register Name	Number of Bytes Transferred
0	Phase OffsetTuning Word Register#1	2 bytes
1	Phase OffsetTuning Word Register #2	2 bytes
2	Frequency Tuning Word #1	6 bytes
3	Frequency Tuning Word #2	6 bytes
4	Delta FrequencyRegister	6 bytes
5	Update Clock Rate Register	4 bytes
6	Ramp Rate Clock Register	3 bytes
7	Control Register	4 bytes
8	I Path Digital Multiplier Register	2 bytes
9	Q Path Digital Multiplier Register	2 bytes
A	Shaped On-Off Keying Ramp Rate Register	2 bytes
B	Q DAC Register	2 bytes

At the completion of any communication cycle, the AD9854/52 serial port controller expects the next 8 rising SCLK edges to be the instruction byte of the next communication cycle. In addition, an active high input on the IORESET pin immediately terminates the current communication cycle. After IORESET returns low, the AD9854/52 serial port controller requires the next 8 rising SCLK edges to be the instruction byte of the next communication cycle.

All data input to the AD9854/52 is registered on the rising edge of SCLK. All data is driven out of the AD9854/52 on the falling edge of SCLK.

Figures 2 and 3 are useful in understanding the general operation of the AD9854/52 Serial Port.

Figure 2. Using SDIO as a Read/Write Transfer

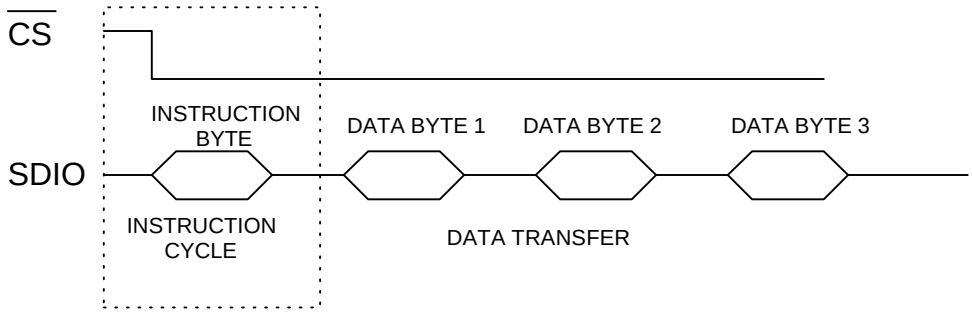
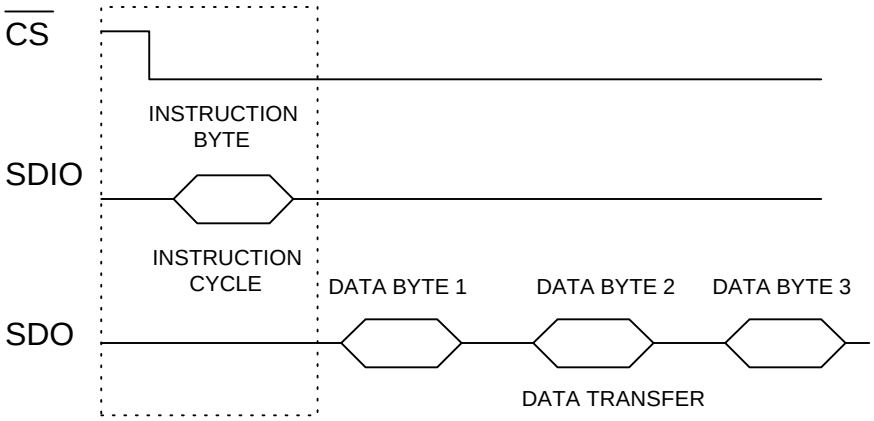


Figure 3. Using SDIO as an Input, SDO as an Output



Instruction Byte

The instruction byte contains the following information:

Instruction Byte Information

MSB	D6	D5	D4	D3	D2	D1	LSB
$\overline{R/W}$	X	X	X	A3	A2	A1	A0

$\overline{R/W}$ - Bit 7 of the instruction byte determines whether a read or write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic zero indicates a write operation.

Bits 6, 5 and 4 of the instruction byte are don't care.

A3, A2, A1, A0 – Bits 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. See Table 1 for register address details

Serial Interface Port Pin Description

SCLK - Serial Clock (Pin21). The serial clock pin is used to synchronize data to and from the AD9854/52 and to run the internal state machines. SCLK maximum frequency is 10 MHz.

CSB - Chip Select (Pin 22). Active low input that allows more than one device on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. If driven high during any communications cycle, that cycle is suspended until CSB is reactivated low. Chip Select can be tied low in systems that maintain control of SCLK.

SDIO - Serial Data I/O (Pin 19). Data is always written into the AD9854/52 on this pin. However, this pin can be used as a bi-directional data line. The configuration of this pin is controlled by bit 1 of register address 20h. The default is logic zero, which configures the SDIO pin as bi-directional.

SDO - Serial Data Out (Pin 18). Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9854/52 operates in a single bi-directional I/O mode, this pin does not output data and is set to a high impedance state.

SYNC I/O – Synchronize IO Port (Pin 17). Synchronizes the I/O port state machines without affecting the addressable registers contents. An active high input on SYNC I/O pin causes the current communication cycle to terminate. After SYNC I/O returns low (logic 0) another communication cycle may begin, starting with the instruction byte write.

Notes on Serial Port Operation

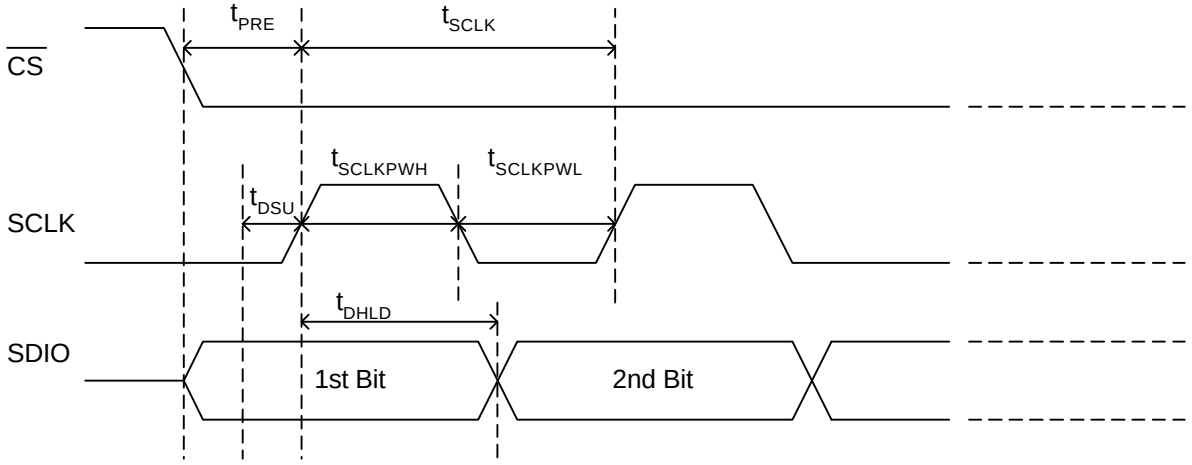
The AD9854/52 serial port configuration bits reside in bits 1 and 0 of register address 7h. It is important to note that the configuration changes IMMEDIATELY upon writing

this register. For multibyte transfers, writing this register may occur during the middle of a communication cycle. Care must be taken compensate for this new configuration for the remainder of the current communication cycle.

The system must maintain synchronization with the AD9854/52 or the internal control logic will not be able to recognize further instructions. For example, if the system sends the instruction to write a 2-byte register, then pulses the SCLK pin for a 3-byte register (24 additional SCLK rising edges), communication synchronization is lost. In this case, the first 16 SCLK rising edges after the instruction cycle will properly write the first two data bytes into the AD9854/52 but the next 8 rising SCLK edges are interpreted as the next instruction byte, NOT the final byte of the previous communication cycle.

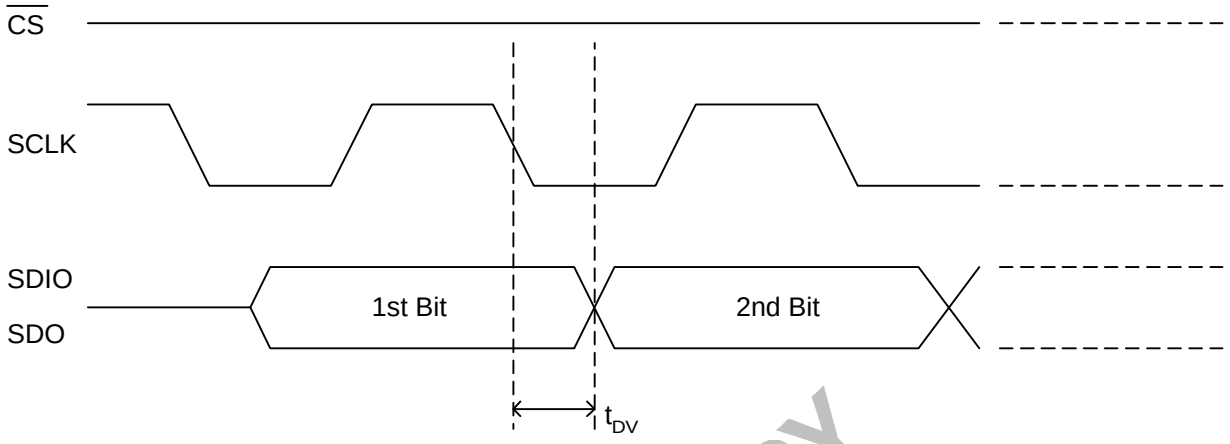
In the case where synchronization is lost between the system and the AD9854/52, the SYNC I/O pin provides a means to re-establish synchronization without re-initializing the entire chip. Asserting the SYNC I/O pin (active high) resets the AD9854/52 serial port state machine, terminating the current IO operation and putting the device into a state in which the next 8 SCLK rising edges are understood to be an instruction byte. The SYNC IO pin must be de-asserted (low) before the next instruction byte write can begin. Any information that had been written to the AD9854/52 registers during a valid communication cycle prior to loss of synchronization will remain intact.

Timing Diagram for Data Write to AD9854/52



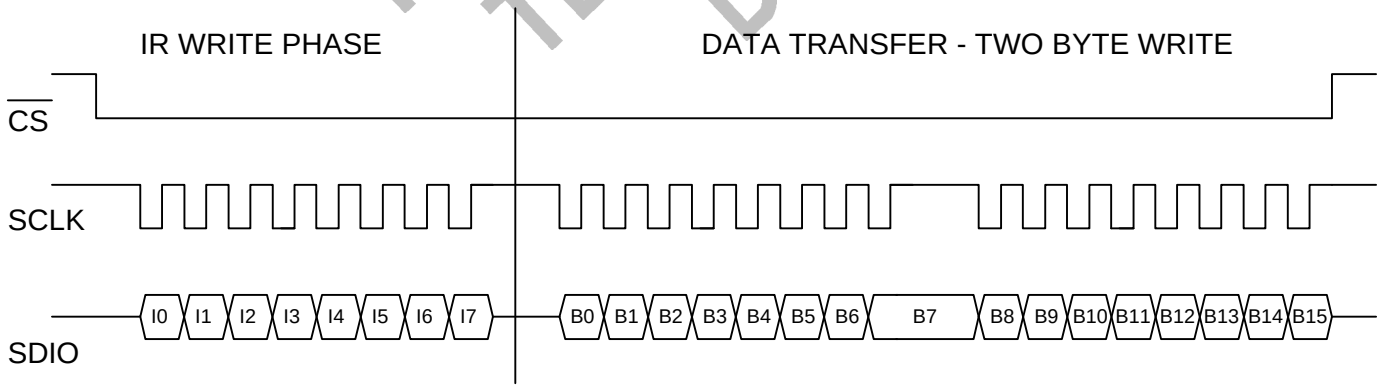
SYMBOL	DEFINITION	MIN
t_{PRE}	CS Set up Time	30 ns
t_{SCLK}	Period of Serial Data Clock	100 ns
t_{DSU}	Serial Data Set up Time	30 ns
$t_{SCLKPWH}$	Serial Data Clock Pulse Width High	40 ns
$t_{SCLKPWL}$	Serial Data Clock Pulse Width Low	40 ns
t_{DHLD}	Serial Data Hold Time	0 ns

Timing Diagram for Read from AD9854/52

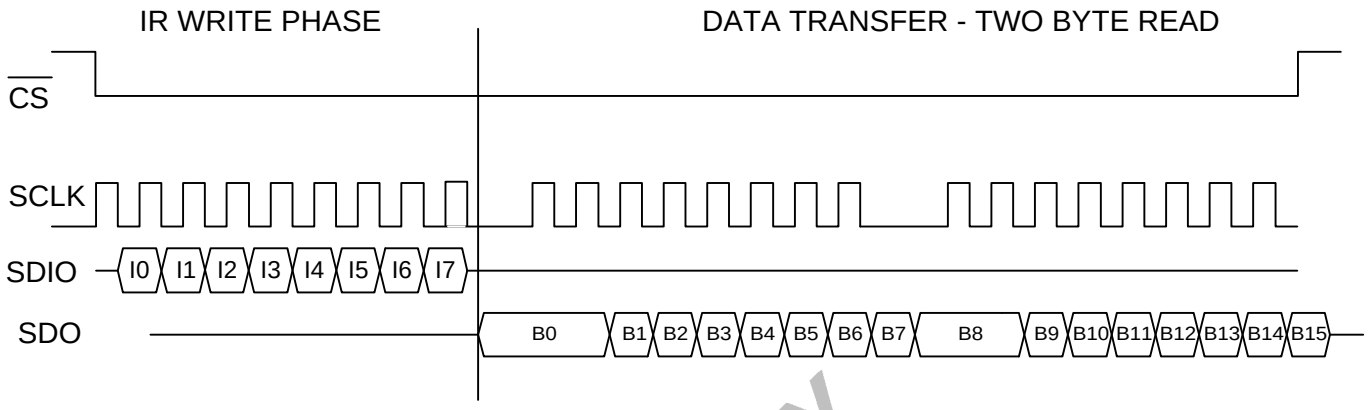


SYMBOL	DEFINITION	MAX
t_{DV}	Data Valid Time	30 ns

DATA WRITE CYCLE, SCLK IDLE HIGH



Data read cycle, 3-wire configuration, SCLK IDLE Low



MSB/LSB Transfers

The AD9854/52 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by the REG0<6> bit. When REG0<6> is set active high, the AD9854/52 serial port is in LSB first format. REG0<6> defaults low, to the MSB first format. The instruction byte must be written in the format indicated by REG0<6>. That is, if the AD9854/52 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit.

Multi-byte data transfers in MSB format can be completed by writing an instruction byte which includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multi-byte communication cycle. Multi-byte data transfers in LSB first format can be completed by writing an instruction byte which includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multi-byte communication cycle.

Update Clock Operation

Programming the AD9854/52 is asynchronous to the system clock with all data being stored in a buffer memory that does not immediately affect the part operation. The buffer memory is transferred to the register bank synchronous to system clock. The register bank information affects part operation.

This transfer of data can occur automatically, with frequency of updates programmable by the user, or can occur completely under user control.

Complete user control, referred to as external update mode, allows the user to drive the UPDATE_CLK signal from their ASIC or DSP. The AD9854/52 UPDATE_CLK pin is configured as an input in external update mode. A rising edge on UPDATE_CLK indicates to the AD9854/52 that the contents of the buffer memory is to be transferred to the register bank. The design uses an edge detector to signal the AD9854/52 to transfer data which allows a very small minimum high pulse width requirement (two system clock periods). Its important to note that if the user keeps UPDATE_CLK high, the AD9854/52 will NOT continuously update the register bank.

Internal update mode, in which the AD9854/52 transfers data from the buffer memory to the register bank automatically, configures the AD9854/52 UPDATE_CLK pin as an output. The AD9854/52 generates a high pulse on UPDATE_CLK pin to signal the user that the buffer memory has just been transferred to the register bank. The minimum high pulse width is designed to be 8 system clock cycles (min). The UPDATE_CLK signal can be used as an interrupt within the system. Its important to note that as an output UPDATE_CLK pin will not have anything approaching a 50/50 duty cycle for slower update rates.

Programming the Update Clock register for values less than 5 will cause the UPDATE_CLOCK pin to remain high. The update clock functionality still works, its just that the user cannot use the signal as an indication that data is transferring. This is an affect of the minimum high pulse time when UPDATE_CLK is an output.

For internal update clock operation, the rate which the updates occur is programmed into the update clock register. The update clock register is 32 bits and the value written into the register corresponds to HALF the number of clock cycles between updates. That is, if a value of 00_00_00_0a (hex), is written into the update clock register the rising edge of the UPDATE_CLOCK pin will occur every 20 cycles (0a hex equals 10 decimal).

Control Register

The Control Register is located in the shaded portion of the Register Layout table at address 1D through 20 hex. It is composed of 32 bits. Bit 31 is located at the top left position and bit 0 is located in the lower right position of the shaded table portion. The register has been sub-divided below to make it easier to locate the text associated with specific control categories.

Power down functions:

Four bits are available to power down the AD9854/52. Each bit is active high, that is, they default low and a logic 1 causes the power down function to be working, The four bits all reside in the same control byte such that one IO write cycle can complete a full power down by writing all four bits true simultaneously. The four bits are located in Control Register[28, 26:24] and are described below. The default state for these bits is logic zero, inactive.

CR[31:29] are open

CR[28] is the comparator power down bit. When set (logic 1), this signal indicates to the comparator that a power down mode is active.

CR[27] must always be written to logic zero. Writing this bit to logic one causes the AD9854/52 to stop working until a master reset is applied.

CR[26] is the control DAC power down bit. When set (logic 1), this signal indicates to the control DAC that the power down mode is active.

CR[25] is the full DAC power down bit. When set (logic 1), this signal indicates to both the sine and control DACs (as well as the DAC reference) that a power down mode is active.

CR[24] is the digital power down bit. When set (logic 1), this signal indicates to the digital section that a power down mode is active. Within the digital section, the clocks will be forced to DC, effectively powering down the digital section. The REFCLK input will still be seen by the PLL and the PLL will continue to output the higher frequency.

PLL functions:

Seven Control register bits, located in the Control Register[22:16] positions, relate to the PLL.

CR[23] is open

CR[22] is the PLL range bit. The PLL range bit controls the VCO gain. The power up state of the PLL range bit is logic 1, higher gain for high frequencies.

CR[21] is the bypass PLL bit, active high. When active the PLL is powered down and the REFCLK input is used to drive the system clock signal. The power up state of the bypass PLL bit is logic 1, PLL bypassed.

CR[20:16] bits are the PLL multiplier factor. These bits are the REFCLK multiplication factor unless the bypass PLL bit is set. The PLL multiplier valid range is from 4 to 20, inclusive.

Other operational functions:

CR[15] is the clear accumulator 1 bit. This bit has a one shot type function. When written active, logic one, a clear accumulator 1 signal is sent to the DDS logic, resetting the accumulator value to zero. The bit is then automatically reset but the buffer memory is not reset. This bit allows the user to easily create a saw wave output with very little (or no) user input required. This bit is intended for chirp mode only but there is no logic to suppress its functionality in other modes.

CR[14] is the clear accumulators bit. This bit, active high, holds both the accumulator 1 and accumulator 2 values at zero for as long as the bit is active. This allows the DDS phase to be initialized via the IO port.

CR[13] is the triangle bit. When this bit is set the AD9854/52 will automatically perform a continuous frequency sweep from the mark to space frequencies and back. The effect is a triangular frequency sweep. When this bit is set, the operating mode must be set to ramped fsk.

CR[12] is the source Q DAC bit on the AD9854 only. When set, the Q path DAC accepts data from the QDAC Register. For the AD9852, this bit does not require a logic one as the only data available to the Q path DAC is from the QDAC Register.

CR[11:9] are the three bits that describe the five operating modes of the AD9854/52:
0h = single tone mode

1h = fsk mode
2h = frequency-ramped fsk mode
3h = chirp mode
4h = psk mode

CR[8] is the internal update active bit. When this bit is set to logic 1, the UPDATE_CLOCK pin is an output and the AD9854/52 generates the UPDATE_CLK signal. When logic 0, external update_clock functionality is performed, the UPDATE_CLK pin is configured as an input.

CR[7] is open

CR[6] is the bypass the inverse sinc filter bit. When set, the data from the DDS block goes directly to the output ramp logic and the clock to the inverse sinc filter is stopped. Default is clear, filter enabled.

CR[5] is the output amplitude enable bit. When set the output amplitude shaping function is enabled and is performed in accordance with the CR[4] bit requirements.

CR[4] is the internal/external output ramp control bit. When set, logic 1, a linear output shape function will be internally generated and applied to the sine DAC data path. When clear, the 12-bit digital multiplier is externally controlled by the user. Defaults low external ramp factors used. The register that holds the 12-bit digital multiplier word also defaults low such that the output is off at power up and until the device is programmed by the user.

CR[3:2] are open.

CR[1] is the serial port msb/lsb first bit. Defaults low, msb first.

CR[0] is the serial port SDO active bit. Defaults low, inactive.