Single Supply V.35 Transceiver

Preliminary Technical Information ADM1345

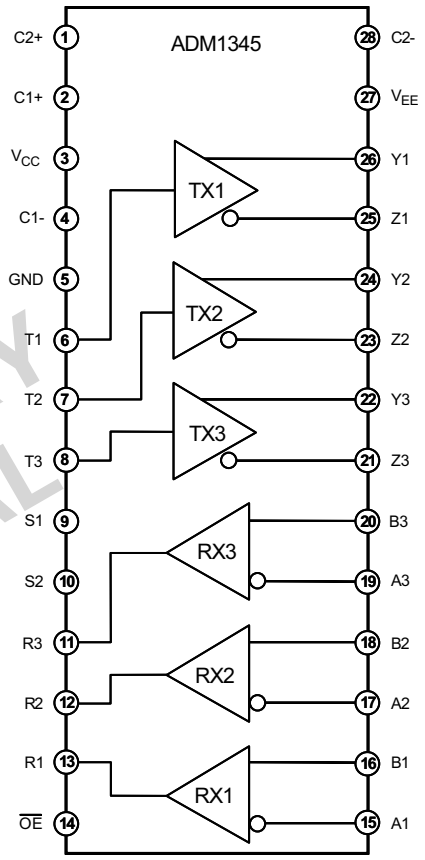
FEATURES

Provides All V.35 Differential Clock and Data Signals on One Chip
Single +5V Supply
Shutdown Mode 1μA Typical I_{CC}
Pin-Selectable DCE or DTE Configuration
ESD-Protected Transmitter Outputs and Receiver Inputs up to 10kV
Failsafe Transmitter Outputs are High Impedance when Disabled, Shutdown or Power Off
Short-Circuit Protected Transmitter Outputs
Complies With CCITT V.35 Specification
Flow-through Pinout for Easy PCB Layout
Second Source for LTC1345

APPLICATIONS

Modems
Telecommunications
Data Routers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM1345 is a line transmitter/receiver that can send and receive the differential clock and data signals for a V.35 interface while requiring only a single +5V supply. The device contains three current output differential line transmitters, three differential receivers, and a charge pump to generate an on-chip negative supply.

The ADM1345 operates at data rates up to 10Mbaud. Transmitter outputs are short-circuit protected and are failsafe, assuming a high impedance state when the transmitters are disabled, the device is shut down, or the power is off. A Receiver Output Enable pin allows the receiver outputs to be forced into a high impedance state.

The receiver inputs and transmitter outputs are both protected against repeated electrostatic discharge (ESD) up to ±10kV.

A complete DCE or DTE V.35 port can be implemented using only an ADM1345 and 4 x 1μF capacitors for the charge pump, an external resistor termination network, and an ADM208E for the control signals.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ADM1345–SPECIFICATIONS

(V_{CC} = Full Operating Range, $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Transmitter Differential Output Voltage, V_{OD}	0.44	0.55	0.66	V	Figure 2, -4V ≤ V_{OS} ≤ 4V
Transmitter Common-Mode Output Voltage, V_{OC}	-0.6	0	0.6	V	Figure 2, V_{OS} = 0V
TransmitterOutputHighCurrent, I_{OH}	-12.6	-11	-9.4	mA	$V_{Y, Z}$ = 0V
Transmitter Output Low Current, I_{OL}	9.4	11	12.6	mA	$V_{Y, Z}$ = 0V
Transmitter Output Leakage Current, I_{OZ}		+1	+100	µA	Sl = S2 = 0V, -5V ≤ $V_{Y,Z}$ ≤ 5V
Transmitter Output Impedance, R_O		100		kΩ	-2V ≤ $V_{Y, Z}$ ≤ 2V
Differential Receiver Input Threshold Voltage, V_{TH}			25	200 mV	-7V ≤ (V_A + V_B)/2 ≤ 7V
Receiver Input Hysteresis, ΔV_{TH}		50		mV	-7V ≤ (V_A + V_B)/2 ≤ 7V
Receiver Input Current (A, B), I_{IN}			0.4	mA	-7V ≤ $V_{A, B}$ ≤ 7V
Receiver Input Impedance, R_{IN}	17.5	30		kΩ	-7V ≤ $V_{A, B}$ ≤ 7V
Receiver Output High Voltage, V_{OH}	3	4.5		V	I_O = 4mA, $V_{B, A}$ = 0.2V
Receiver Output Low Voltage, V_{OL}		0.2	0.4	V	I_O = 4mA, $V_{B, A}$ = -0.2V
Receiver Output Short-Circuit Current, I_{OSR}	7		85	mA	0V < V_O < V_{CC}
Receiver Three-State Output Current, I_{OZR}			±10	µA	S1 = S2 = 0V, 0V ≤ V_O ≤ V_{CC}
Logic Input High Voltage, V_{INH}	2			V	Transmitter Inputs, S1, S2, OE
Logic Input Low Voltage, V_{INL}			0.8	V	Transmitter Inputs, S1, S2, OE
Logic Input Current, I_{IN}			±10	µA	Transmitter Inputs, S1, S2, OE
V_{CC} Supply Current, I_{CC}		118	170	mA	Figure 2, V_{OS} = 0, S1 = S2 = HIGH
		19	30	mA	No Load, S1 = S2 = HIGH
		1	100	µA	Shutdown, S1 = S2 = 0V
Generated Negative Supply Voltage, V_{EE}		-5.5		V	No Load, S1 = S2 = HIGH
Transmitter Rise or Fall Time, t_r, t_f		7	40	ns	Figures 2 and 4, V_{OS} = 0V
Transmitter Input to Output Propagation Delay, Low to High, t_{PLH}		25	70	ns	Figures 2 and 4, V_{OS} = 0V
Transmitter Input to Output Propagation Delay, High to Low, t_{PHL}		25	70	ns	Figures 2 and 4, V_{OS} = 0V
Transmitter Output to Output Skew, t_{SKEW}		0		ns	Figures 2 and 4, V_{OS} = 0V
Receiver Input to Output Propagation Delay, Low to High, t_{PLH}		49	100	ns	Figures 2 and 5, V_{OS} = 0V
Receiver Input to Output Propagation Delay, High to Low, t_{PHL}		52	100	ns	Figures 2 and 5, V_{OS} = 0V
Differential Receiver Skew, (t_{SKEW} = t_{PLH} - t_{PHL})		3		ns	Figures 2 and 5, V_{OS} = 0V
Receiver Enable to Output LOW, t_{ZL}		40	70	ns	Figures 3 and 6, C_L = 15pF
Receiver Enable to Output HIGH, t_{ZH}		35	70	ns	Figures 3 and 6, C_L = 15pF
Receiver Disable From LOW, t_{LZ}		30	70	ns	Figures 3 and 6, C_L = 15pF
Receiver Disable From HIGH, t_{HZ}		35	70	ns	Figures 3 and 6, C_L = 15pF
Charge Pump Oscillator Frequency, f_{OSC}		200		kHz	
Maximum Data Rate, BR_{MAX} (Note 3)	10	15		Mbaud	

Notes

1. All currents into device pins are termed positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.
2. All typicals are given for Vcc = 5V, C1 = C2 = C3 = lµF ceramic capacitors and T_A = 25°C.
3. Maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes. Data rate is guaranteed by correlation and is not tested.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

Supply Voltage, V_{CC} 6V
Input Voltage
  Transmitters ..... -0.3V to (Vcc + 0.3V)
  Receivers ..... -18V to 18V
  S1, S2, OE ..... -0.3V to (Vcc + 0.3V)
Output Voltage
  Transmitters ..... -18V to 18V
  Receivers ..... -0.3V to (Vcc + 0.3V)
  V_{EE} ..... -10V to 0.3V
Short-Circuit Duration
  Transmitter Output ..... Indefinite
  Receiver Output ..... Indefinite
  V_{EE} ..... 30 sec
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... -40°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

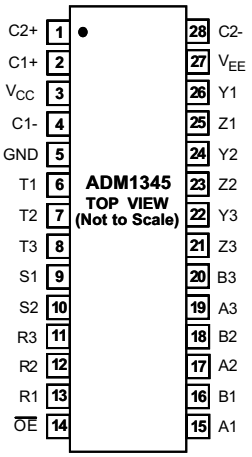


Figure 1. ADM1345 Pin Configuration Diagram

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM1345JN	0°C to +70°C	N-28
ADM1345JR	0°C to +70°C	R-28
ADM1345AN	–40°C to +85°C	N-28
ADM1345AR	–40°C to +85°C	R-28

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1345 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	C2+	Capacitor C2 Positive Terminal.This is the positive side of the capacitor for the second stage of the charge pump.
2	C1+	Capacitor C1 Positive Terminal. This is the positive side of the capacitor for the first stage of the charge pump.
3	V_{CC}	Positive Supply, 4.75 ≤ Vcc ≤ 5.25V.
4	C1-	Capacitor C1 Negative Terminal. This is the negative terminal of the capacitor for the first stage of the charge pump.
5	GND	Ground. The positive terminal of C3 is connected to ground.
6	Tl	Transmitter 1 Input. TTL/CMOS-compatible logic input.
7	T2	Transmitter 2 Input. TTL/CMOS-compatible logic input.
8	T3	Transmitter 3 Input. TTL/CMOS-compatible logic input.
9	S1	Select Input 1. TTL/CMOS-compatible logic input.
10	S2	Select Input 2. TTL/CMOS-compatible logic input.
11	R3	Receiver 3 Output. TTL/CMOS-compatible logic output.
12	R2	Receiver 2 Output. TTL/CMOS-compatible logic output.
13	R1	Receiver 1 Output. TTL/CMOS-compatible logic output.
14	OE	Receiver Output Enable. TTL/CMOS-compatible logic input.
15	A1	Receiver 1 Inverting Input.
16	B1	Receiver 1 Noninverting Input.
17	A2	Receiver 2 Inverting Input.
18	B2	Receiver 2 Noninverting Input.
19	A3	Receiver 3 Inverting Input.
20	B3	Receiver 3 Noninverting Input.
21	Z3	Transmitter 3 Inverting Output. Differential current source output. Sources current when T3 low. Sinks current when T3 high.
22	Y3	Transmitter 3 Noninverting Output. Differential current source output. Sinks current when T3 low. Sources current when T3 high.
23	Z2	Transmitter 2 Inverting Output. Differential current source output. Sources current when T2 low. Sinks current when T2 high.
24	Y2	Transmitter 2 Noninverting Output. Differential current source output. Sinks current when T2 low. Sources current when T2 high.
25	Z1	Transmitter 1 Inverting Output. Differential current source output. Sources current when T1 low. Sinks current when T1 high.
26	Yl	Transmitter 1 Noninverting Output. Differential current source output. Sinks current when T1 low. Sources current when T2 high.
27	V_{EE}	Charge Pump Output. Connected to negative terminal of capacitor C3.
28	C2-	Capacitor C2 Negative Terminal.

Typical Performance Characteristics

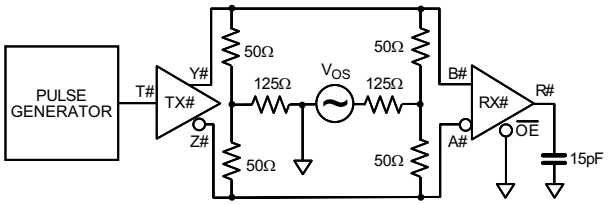


Figure 2. V.35 Transmitter/Receiver Test Circuit

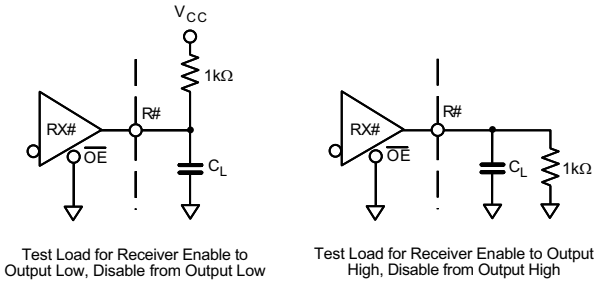


Figure 3. Receiver Test Loads for t_{ZL}, t_{ZH}

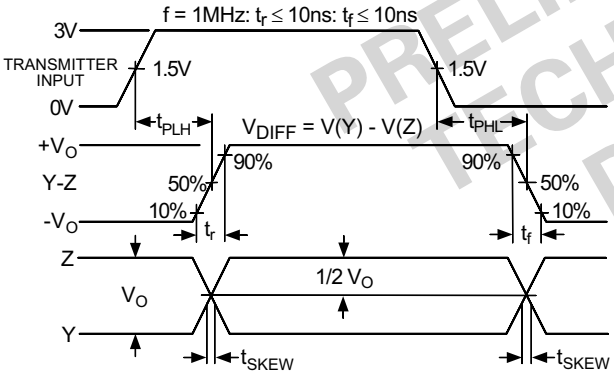


Figure 4. V.35 Transmitter Propagation Delays

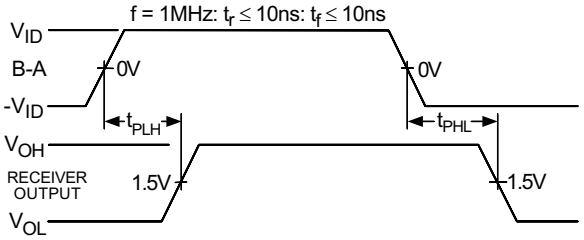


Figure 5: V.35 Receiver Propagation Delays

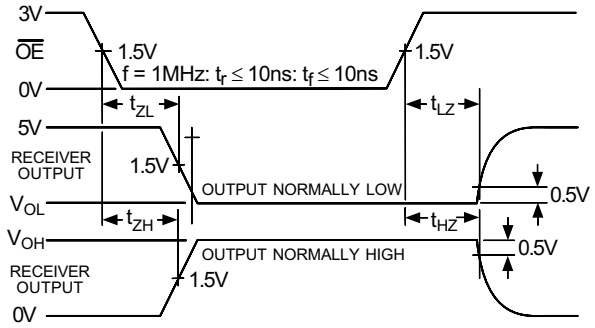


Figure 6. Receiver Enable and Disable Times

Figure 7. Transmitter Output Waveforms

Figure 8. Receiver Output Waveforms

Figure 9. Transmitter Output Current vs. Temperature

Figure 12. Receiver Skew vs. Temperature

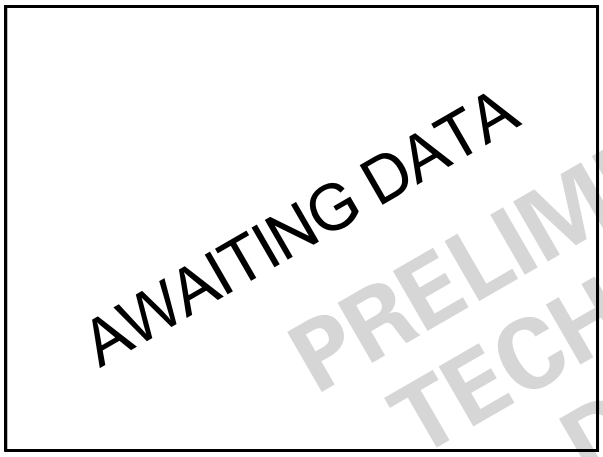


Figure 10. Transmitter Output Current vs. Output Voltage

Figure 13. Supply Current vs. Temperature

Figure 11. Transmitter Output Skew vs. Temperature

Figure 14. V_{EE} vs. Temperature

CIRCUIT DESCRIPTION

The ADM1345 contains three transmitters with TTL/CMOS-compatible inputs and complementaryl current-source outputs, three receivers with differential inputs and TTL/CMOS-compatible outputs, and an inverting charge pump to provide a negative supply rail (V_{EE}).

TRANSMITTER OUTPUTS

The internal CMOS logic of the transmitter controls an output stage consisting of switched complementary current sources, as shown in figure 15.

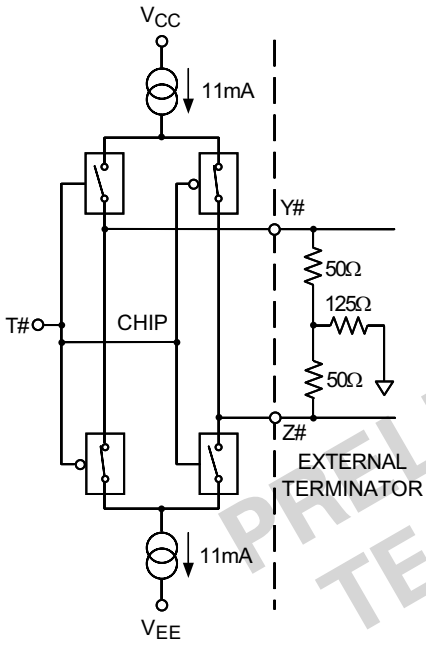


Figure 15. Transmitter Equivalent Output Circuit

With a logic zero at the transmitter input, the inverting output Z sources 11mA (positive current flows out of the pin) and the non-inverting output Y sinks 11mA (positive current flows into the pin). With a logic 1 at the transmitter input, the converse is true, Z sinks 11mA and Y sources 11mA.

The differential transmitter output voltage is set by the termination resistors. With both transmitter and receiver terminated with differential 50Ω resistors, the output voltage is set to (50Ω x 11mA) = 550mV.

If the transmitter and receiver grounds are at the same potential, then the output voltages of the transmitter will be symmetrical above and below zero and there will be no common-mode voltage (assuming that the current sources and 50Ω resistors are matched). However, the transmitter outputs have a common-mode range of ±2V, which allows for a ground difference between transmitter and receiver of ±4V. In this case, a common-mode current will flow in the 125Ω resistors. More information on terminating resistors is given in the Applications Information section.

RECEIVER INPUTS

All receiver inputs have a 30kΩ resistance to ground and require additional, external terminating resistors. Receivers feature hysteresis of 50mV to improve noise immunity. The receivers have a common Output Enable (OE) pin, which enables the receiver outputs when low and puts the receiver outputs into a high impedance state when high. OE should be held low for normal operation.

SELECT INPUTS

The ADM1345 can be configured by two select inputs, which may be hardwired or under software control. Using these two inputs, four modes can be selected, as shown in the following truth table.

Table I. Transmitter and Receiver Configuration

S1	S2	Condition
0	0	Shutdown Mode, all transmitters and receivers inactive
0	1	All receivers active, TX3 shut down (DTE Mode)
1	0	All transmitters active, RX3 shut down (DCE Mode)
1	1	All transmitters and receivers active

In the DTE mode, the output of the shut-down transmitter (TX3) assumes a high-impedance state. In the DCE mode, the output of the shut-down receiver (RX3) assumes a high impedance state.

In the shutdown mode (S1 and S2 low) the charge pump is switched off, V_{EE} is clamped to ground, and all transmitter and receiver outputs assume a high impedance state.

Truth tables for the various transmitter and receiver input conditions are given below.

Table II. Transmitter Truth Table

	Inputs			Outputs			
Configuration	S1	S2	T	Y1 & Y2	Z1 & Z2	Y3	Z3
DTE	0	1	0	0	1	Z	Z
DTE	0	1	1	1	0	Z	Z
DCE or all ON	1	X	0	0	1	0	1
DCE or all ON	1	X	1	1	0	1	0
Shutdown	0	0	X	Z	Z	Z	Z

Table III. Receiver Truth Table

	Inputs			Outputs		
Configuration	S1	S2	OE	B-A	R1 & R2	R3
DTE or all ON	X	1	0	⊕0.2V	1	1
DTE or all ON	X	1	0	≤-0.2V	0	0
DCE	1	0	0	⊕0.2V	1	Z
DCE	1	0	0	≤-0.2V	0	Z
Disabled	X	X	1	X	Z	Z
Shutdown	0	0	X	X	Z	Z

Z = high impedance

CHARGE PUMP

A negative supply voltage is required to achieve the negative portion of the transmitter output common-mode range. This is achieved by a charge-pump voltage-doubler/inverter.

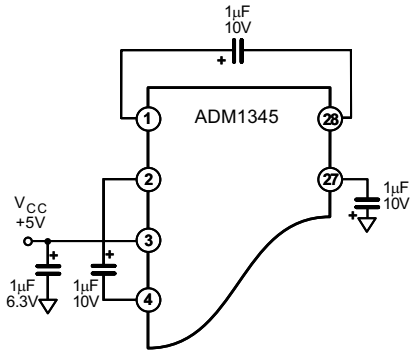


Figure 16. Connection of Charge Pump Capacitors

The charge pump requires 3, 1µF capacitors, and the the 5V supply should also be decoupled with a 1µF capacitor close to the V_{CC} pin More details about charge pump capacitors and supply decoupling are given in the Applications Information.

ESD PROTECTION

The receiver inputs and transmitter outputs of the ADM1345 have built-in protection against repeated electrostatic discharge (ESD) transients of up to ±10kV. As the ESD protection depends on clamping the transient to V_{CC} or V_{EE} by on-chip diodes, the impedance seen at these pins must be low, which means that capacitors with low equivalent series resistance (ESR) must be used on these pins.

ESD testing is carried out using the Human Body Model.

APPLICATIONS INFORMATION

CHARGE PUMP CAPACITORS AND SUPPLY DECOUPLING

For proper operation of the charge pump, the capacitors should have an equivalent series resistance (ESR) less than 1Ω. As the charge pump draws current pulses from V_{CC}, the V_{CC} decoupling capacitor should also have low ESR. The V_{CC} decoupling capacitor and V_{EE} reservoir capacitor should also have low ESR because they determine how effectively ESD pulses are clamped to V_{CC} or V_{EE} by the on-chip clamp diodes. Tantalum or monolithic ceramic capacitors are suitable for these components. If using tantalum capacitors, do not forget to observe polarity.

CABLE TERMINATION

Both the transmitter and receiver end of the cable connected between ADM1345s must be properly and identically terminated. Termination requires a differential resistance of 100Ω between the transmitter outputs (or receiver inputs) and a common-mode resistance of 150Ω to ground to allow common-mode current to flow if the transmitter and receiver grounds are at different potentials.

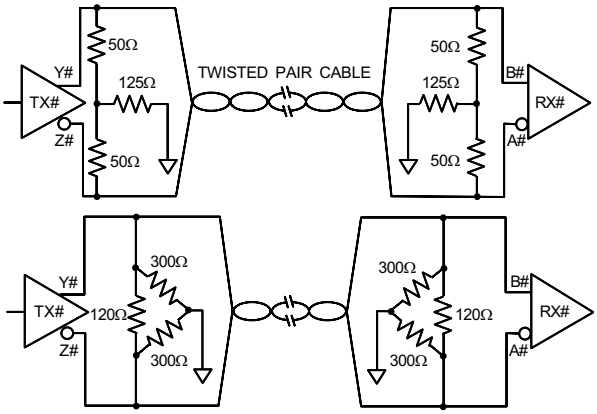


Figure 17. Termination Networks

This requirement can be met using either a Y network or an equivalent D network, as shown in figure 18. Standard 1/8W surface mount or through-hole resistors may be used but resistor tolerance should be 5% or better to maintain the proper differential output swing. Alternatively, a complete package containing 5 terminating networks in a 14-pin SO-IC or DIP can be obtained from:

BI Technologies (Formerly Beckman Industrial)

Resistor Networks,

4200 Bonita Place

Fullerton, CA 92635

Phone: (714) 447-2357 Fax: (714) 447 2500

Part #: BI Technologies 627T500/1250 (SOIC)
BI Technologies 899TR50/125 (DIP)

DCE/DTE PORT APPLICATION

The ADM1435 is ideally suited for implementation of a Data Terminal Equipment (DTE) or Data Circuit Terminating Equipment (DCE) port. Figure 18 (facing page) shows a complete V.35 DTE/DCE interface using only two ICs, one terminating resistor network, and 9 capacitors for each side of the interface. The ADM1345 is used to transmit and receive the high-speed data and clock signals, while the ADM208Es are used for the lower speed control signals.

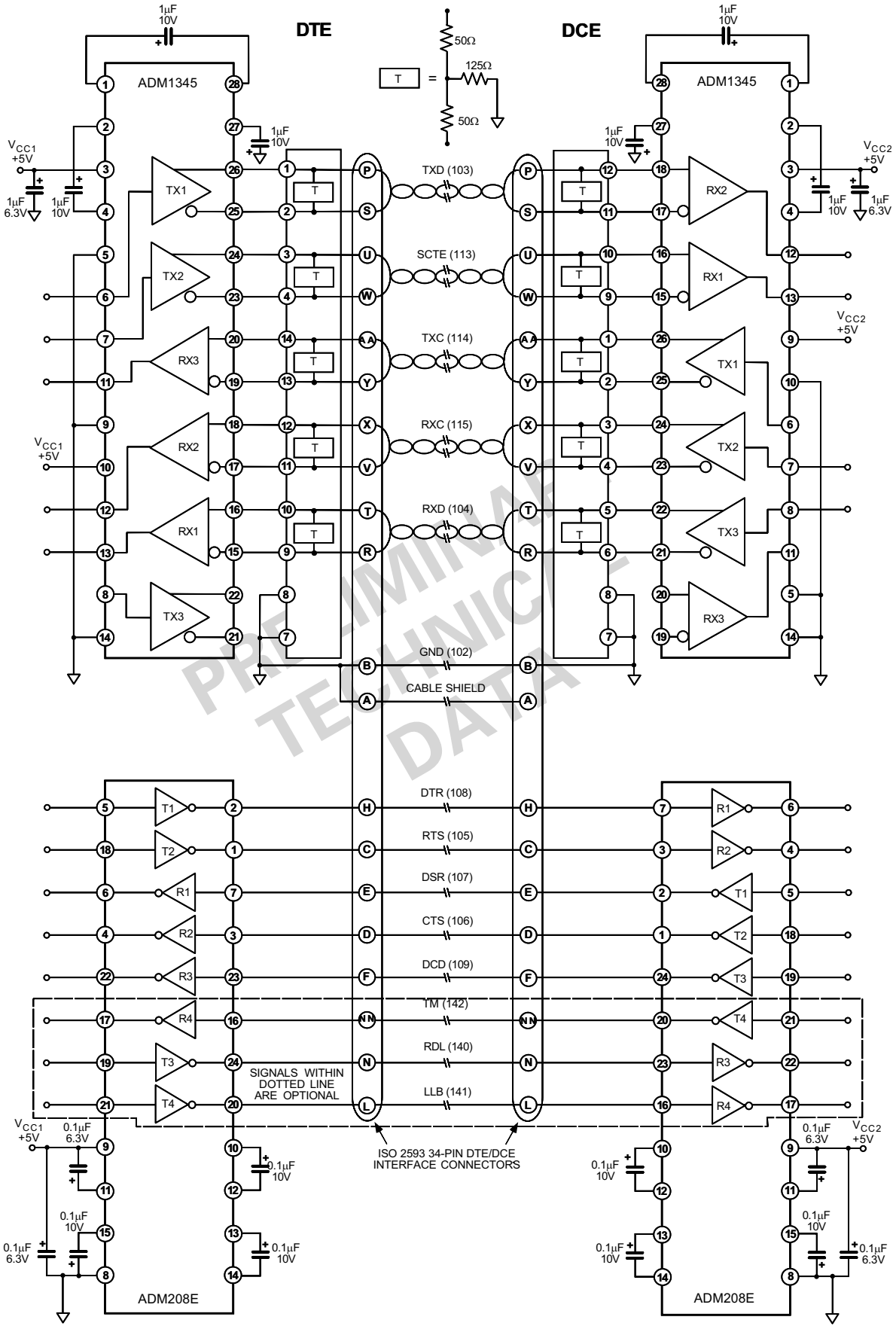


Figure 18. Complete DTE/DTE Interface Operating from Single +5V Supply

RS422/RS485 APPLICATIONS

The receivers in the ADM1345 are ideally suited to RS422 and RS485 applications. Using the circuit of figure 19, the receiver can reconstruct the data stream at data rates up to 10Mbaud while meeting the RS422 and RS485 common-mode voltage requirements of -7V to +12V.

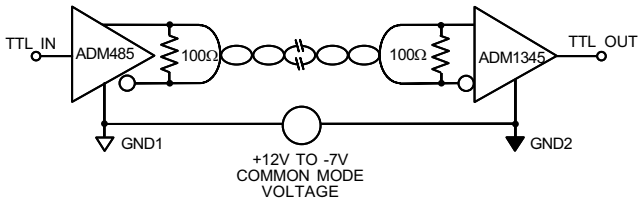
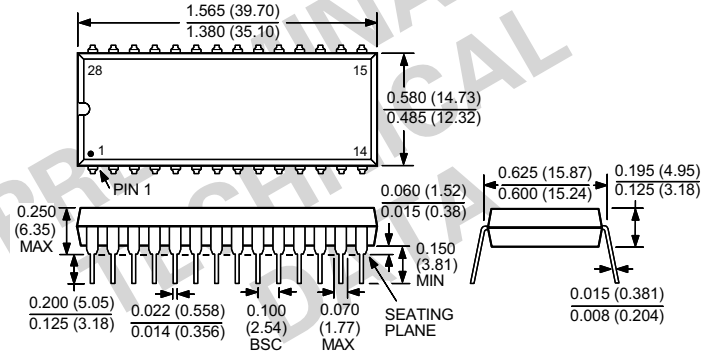


Figure 19. RS422/RS485 Application

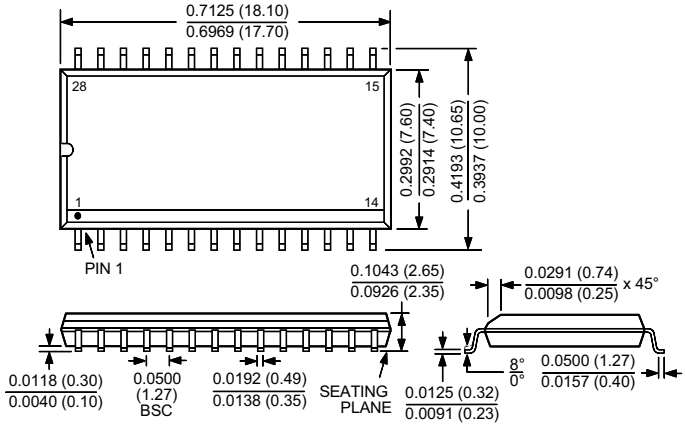
OUTLINE DIMENSIONS

Dimenions shown in inches and (mm)

28-Lead Plastic DIP (N-28)



28-Lead Plastic DIP (N-28)



28-Lead SOIC (R-28)