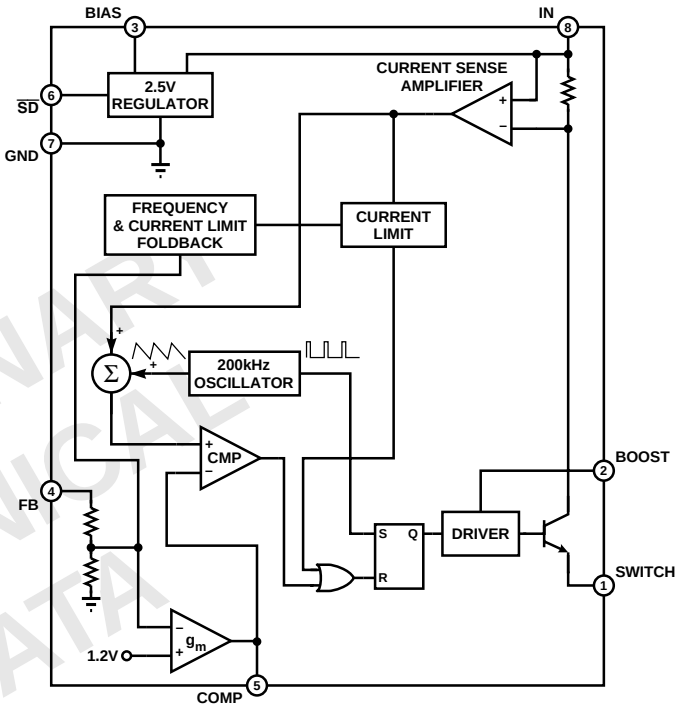
200 kHz, 1 A Step-Down High-Voltage Switching Regulator

Preliminary Technical Data — ADP3050

FEATURES
- Wide Input Voltage Range: 3.6 V to 30 V
- Adjustable and Fixed (3.3 V, 5 V) Output Options
- Saturating Power Switch for Higher Efficiency
- Uses Small Surface-mount Components
- Cycle-by-cycle Current Limiting
- Peak Input Voltage (100 ms): 60 V
- Thermally Enhanced 8-Lead SOIC Package

APPLICATIONS
- Pre-regulator for Linear Regulators
- Distributed Power Systems
- Automotive Systems
- Battery Chargers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3050 is a current-mode monolithic buck (step-down) PWM switching regulator that contains a high current 1A switch and all control, logic and protection functions. It uses a unique compensation scheme which allows the use of any type of output capacitor (tantalum, ceramic, electrolytic, OS-CON). Unlike some buck regulators, the design is not restricted to using a specific type of output capacitor or ESR value.

A special boosted drive stage is used to saturate the NPN power switch, providing a system efficiency higher than conventional bipolar buck switchers. Further efficiency improvements are obtained by using the low voltage regulated output to provide the device's internal operating current. A high switching frequency allows the use of small external surface-mount components. A wide variety of standard off-the-shelf devices can be used, providing a great deal of design flexibility. A complete regulator design requires only a few external devices.

The ADP3050 includes a shutdown input which places the device in a low-power mode, reducing the total supply current to under 20 μA. Internal protection features include thermal shutdown circuitry and a cycle-by-cycle current-limit for the power switch to provide complete device protection under fault conditions.

The ADP3050 provides excellent line and load regulation, maintaining ±3% output voltage accuracy over temperature and under all input voltage and output current conditions.

The ADP3050 is specified over the industrial temperature range of -40°C to +85°C and is available in a thermally enhanced 8-lead SOIC package.

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ADP3050–SPECIFICATIONS[1] (V_{IN} = 10.0 V, T_A = -40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
FEEDBACK						
Feedback Voltage	V_{FB}					
ADP3050			1.16	1.2	1.24	V
ADP3050-3.3			3.20	3.3	3.40	V
ADP3050-5			4.85	5.0	5.15	V
Line Regulation		V_{IN} = 10 V to 30 V, no load	–0.2	0.01	0.2	%/V
Load Regulation		I_{LOAD} = 100 mA to 1 A	–1.3	0.1	1.3	%/A
Input Bias Current	I_{FB}	ADP3050AR only		0.65	2	µA
ERROR AMPLIFIER						
Transconductance[2]	g_m			1250		µMho
Voltage Gain[2]	A_{VOL}			300		V/V
Output Current						
ADP3050		COMP = 1.0 V, FB = 1.1 V to 1.3 V		±115		µA
ADP3050-3.3		COMP = 1.0 V, FB = 3.0 V to 3.6 V		±120		µA
ADP3050-5		COMP = 1.0 V, FB = 4.5 V to 5.5 V		±135		µA
OSCILLATOR						
Oscillator Frequency[3]	f_{OSC}		170	200	240	kHz
Minimum Duty Cycle	D_{MIN}			10		%
Maximum Duty Cycle	D_{MAX}			90		%
SWITCH						
Average Current Limit[4]	$I_{CL(AVG)}$					
ADP3050		BOOST = 15 V, FB = 1.1 V	1.0	1.25	1.5	A
ADP3050-3.3		BOOST = 15 V, FB = 3.0 V	1.0	1.25	1.5	A
ADP3050-5		BOOST = 15 V, FB = 4.5 V	1.0	1.25	1.5	A
Peak Current Limit	$I_{CL(PEAK)}$			1.5		A
Saturation Voltage		BOOST = 15 V, I_{LOAD} = 1 A		0.65	0.95	V
Leakage Current				50		nA
SHUTDOWN						
Input Voltage Low					0.4	V
Input Voltage High			2.0			V
SUPPLY						
Minimum Input Voltage[5]	V_{IN}				3.6	V
Minimum BIAS Voltage	V_{BIAS}				3.0	V
Minimum BOOST Voltage	V_{BOOST}				3.0	V
IN Supply Current[6]	I_Q					
Normal Mode		$\overline{BIAS}$ = 5.0 V		0.7	1.5	mA
Shutdown Mode		$\overline{SD}$ = 0 V, VIN ≤ 30 V		15	40	µA
BIAS Supply Current	I_{BIAS}	BIAS = 5.0 V		4.0	6.0	mA
BOOST Supply Current	I_{BOOST}	BOOST = 15 V , I_{SW} = 0.5 A		18		mA
		BOOST = 15 V , I_{SW} = 1.0 A		20	40	mA

NOTES

1 All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

2 Transconductance and voltage gain measurements refer to the internal amplifier without the voltage divider. To calculate the transconductance and gain of the fixed voltage parts, divide the values shown by FB/1.21.

3 The switching frequency is reduced when the feedback pin is lower than 0.8 × FB.

4 Switch current limit is measured with no diode, inductor, or capacitor connected to output pin.

5 Minimum input voltage is not measured directly, but is guaranteed by other tests. The actual minimum inputvoltage needed to keep the output in regulation will depend on output voltage and load current.

6 I_Q is a function of the no-load input current.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

IN Voltage
- Steady State ..... 30 V
- Peak (<100 ms) ..... 60 V

BOOST Voltage ..... 45 V
$\overline{SD}$, BIAS Voltage ..... -0.3 V to IN + 0.3 V
FB Voltage ..... -0.3 V to 8 V
Operating Ambient Temperature Range . -40°C to +85°C
Operating Junction Temperature Range -40°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
θ_{JA} ..... 86°C/W
Lead Temperature Range (Soldering, 60 sec.) ..... 300°C

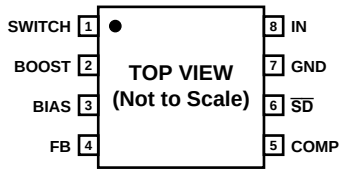
*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND

ORDERING GUIDE

Model	Output Voltage	Temperature Range	Package*
ADP3050AR	ADJ	-40°C to +85°C	SO-8
ADP3050AR-3.3	3.3 V	-40°C to +85°C	SO-8
ADP3050AR-5	5.0 V	-40°C to +85°C	SO-8

* SO = Small Outline Package

PIN CONFIGURATION
R-8



PIN DESCRIPTION

Pin	Name	Function
1	SWITCH	This is the emitter of the internal NPN power switch. The voltage at this pin switches between V_{IN} and approximately -0.5 V.
2	BOOST	This pin is used to provide a boosted voltage (higher than V_{IN}) for the drive stage of the NPN power switch. With the higher drive voltage, the power switch can be saturated, greatly reducing the switch power losses.
3	BIAS	Connect this pin to the regulated output voltage to maximize system efficiency. When this pin is above 2.7 V, most of the ADP3050 operating current will be taken from the output instead of the input supply. Leave unconnected if not used.
4	FB	This feedback pin senses the regulated output voltage. Connect this pin directly to the output (fixed output versions).
5	COMP	This pin is used to compensate the regulator with and external resistor and capacitor. This pin can be used to override the control loop, but the voltage on this pin should not exceed about 2 V, as the pin is internally clamped to ensure a fast transient response. Use a pull-up resistor if this pin is to be pulled higher than 2V.
6	$\overline{SD}$	Use this pin to turn the device on and off. If this feature is not needed, tie this pin directly to V_{IN}.
7	GND	Connect this pin to local ground plane.
8	IN	Connect this pin to the input supply voltage. A input bypass capacitor must be placed close to this pin to ensure proper regulator operation.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

The ADP3050 is a fixed frequency, current mode buck regulator. Current mode systems provide excellent transient response, and are much easier to compensate than voltage mode systems. Refer to the functional block diagram. At the beginning of each clock cycle, the oscillator sets the latch, turning on the power switch. The signal at the non-inverting input of the comparator is a replica of the switch current (summed with the oscillator ramp). When this signal reaches the appropriate level set by the output of the error amplifier, the comparator resets the latch and turns off the power switch. In this manner, the error amplifier sets the correct current trip level to keep the output in regulation: if the error amplifier output increases, more current is delivered to the output; if it decreases, less current is delivered to the output.

The current sense amplifier provides a signal proportional to switch current to both the comparator and to a cycle-by-cycle current limit. If the current limit is exceeded, the latch will be reset, turning the switch off until the beginning of the next clock cycle. The ADP3050 has a foldback current limit which reduces the switching frequency under fault conditions to reduce stress to the IC and to the external components.

Most of the control circuitry is biased from the 2.5 V internal regulator. When the BIAS pin is left open or when the voltage at this pin is less than 2.7 V, all of the operating current for the ADP3050 is drawn from the input supply. When the BIAS pin is above 2.7 V, the majority of the operating current is then drawn from this pin (usually tied to the regulator's low-voltage output) instead of from the higher-voltage input supply. This can provide substantial efficiency improvements at light-load conditions, especially for systems where the input voltage is much higher than the output voltage.

The ADP3050 uses a special drive stage which allows the power switch to saturate. An external diode and capacitor provide a boosted voltage to the drive stage that is higher than the input supply voltage. Overall efficiency is dramatically improved by using this type of saturating drive stage. Pulling the $\overline{SD}$ pin below 0.4 V puts the device in a low-power mode, shutting off all internal circuitry and reducing the supply current to under 20 μA.

Setting the Output Voltage

The output of the adjustable version (ADP3050AR) can be set to any voltage between 1.25V and 12V by connecting a resistor divider to the FB pin as shown in Figure X. The resistor value for R2 can be calculated by choosing a value between 1 kΩ and 10kΩ for R1, using the following equation:

$$R2 = R1 \times ((V_{OUT}/1.2)-1) \quad (1)$$

It is important to note that the accuracy of these resistors directly affets the accuracy of the output voltage. The FB pin threshold variation is ±3%, and the tolerances of R1 and R2 will add to this to determine the total output variation.

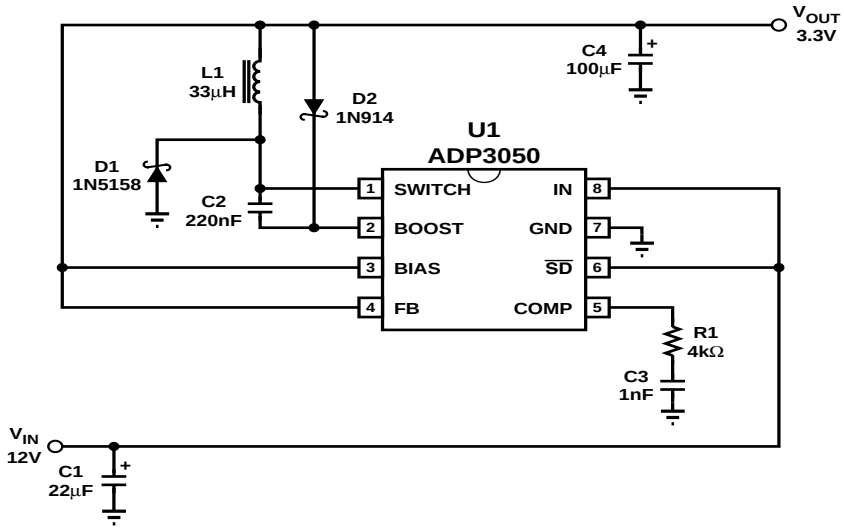
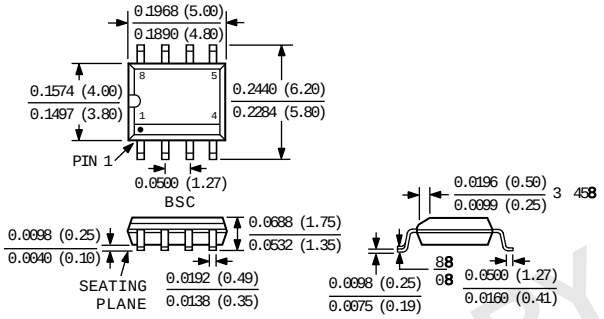


Figure 1. Typical Application Circuit.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC
R-8



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