Professional *Extended-10™* Video Encoder with 54MHz Oversampling

Preliminary Technical Data

ADV7194

FEATURES

10-Bit Extended CCIR-656 Input Data Port
6 high Quality 10-Bit Video DACs
10-Bit Internal Digital Video Processing
Multi-Standard Video Input
Multi-Standard Video Output
4xOversampling with internal 54MHz PLL
Programmable Video Control includes:
- **Digital Noise Reduction**
- **Gamma Correction**
- **Black Burst**
- **LUMA Delay**
- **CHROMA Delay**
- **Multiple Luma & Chroma Filters**
- **Luma SSAF™ (Super Sub-Alias Filter)**

Average Brightness detection
Field Counter

CGMS (Copy Generation Management System)
WSS (Wide Screen Signalling)
Closed Captioning support.
Teletext Insertion Port (PAL-WST)
2 Wire Serial MPU Interface (I^2C Compatible & Fast I^2C)
I2C Interface

Supply Voltage 5V & 3.3V Operation
80-Pin LQFP Package

APPLICATIONS

Professional DVD Playback Systems,
PC Video/Multimedia Playback Systems
Progressive Scan Playback Systems
Professional Studio Equipment

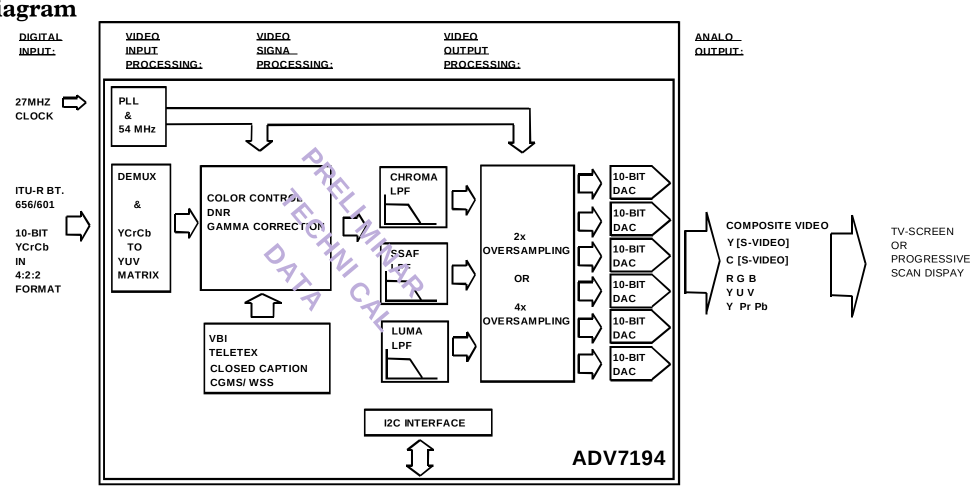
GENERAL DESCRIPTION

The ADV7194 is part of the new generation of video encoders from Analog Devices. The device builds on the performance of previous video encoders and provides new features like interfacing progressive scan devices, Digital Noise Reduction, Gamma Correction, 4xOversampling and 54MHz operation, Average Brightness Detection, Black Burst Signal Generation, Chroma Delay, an additional Chroma Filter, etc.

The ADV7194 supports NTSC-M, NTSC-N (Japan), PAL N, PAL-B/D/G/H/I and PAL-60 standards. Input standards supported include ITU-R.BT656 4:2:2 YCrCb in 8-, 10-, 16- or 20-Bit format and 3x10-Bit YCrCb progressive scan format.
The ADV7194can output Composite Video (CVBS), S-Video (Y/C), Component YUV* or RGB and analog progressive scan in YPrPb format. The analog component output is also compatible with Betacam, MII and SMPTE/EBU N10 levels, SMPTE 170M NTSC and ITU-R.BT 470 PAL.

For a more information about the ADV7194s features refer to DETAILED DESCRIPTION.

Simplified Block Diagram



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Notes:
Extended-10™ (Trademark of Analog Devices Inc.). This technology combines 10-Bit Conversion, 10-Bit Digital Video Data Processing and 10-Bit External Interfacing.
SSAF is a trademark of Analog Devices Inc.
This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights.

ITU-R and CCIR are used interchangeably in this document (ITU-R has replaced CCIR recommendations)
I^2C is a registered trademark of Philips Corporation.
Throughout the document YUV refers to digital or analog component video.

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CONTENTS

5V SPECIFICATIONS[1]

(V_{AA} = + 5V, V_{REF} = 1.235 V, $R_{SET1,2}$ =1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (each DAC)			10	Bits	
Accuracy (each DAC)					
Integral Nonlinearity[3]			±1.0	LSB	
Differential Nonlinearity[3]			±1.0	LSB	Guaranteed monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		0	+/-1	µA	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}		6	10	pF	
Input Leakage Current[8]		1		µA	
Input Leakage Current[9]		200		µA	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}		0.8	0.4	V	I_{SINK} = 3.2 mA
Tri-State Leakage Current[10]		10		µA	
Tri-State Leakage Current[11]		200		µA	
Tri-State Output Capacitance		6	10	pF	
ANALOG OUTPUTS					
Output Current(max)	4.125	4.33	4.625	mA	R_L = 300Ω
Output Current(min)		2.16		mA	R_L = 600Ω,$R_{SET1,RSET2}$ = 2400Ω
DAC to DAC Matching[3]		0.4	2.5	%	
Output Compliance, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		6		pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE					
Reference Range, V_{REF}[4]	1.112	1.235	1.359	V	
POWERREQUIREMENTS					
V_{AA}	4.75	5.0	5.25	V	
Normal Power Mode					
I_{DAC}[4]		29	35	mA	
I_{CCT} (2xOversampling)[6,7]		80	120	mA	
I_{CCT} (4xOversampling)[6,7]		120	170	mA	
I_{PLL}		6	10	mA	
Sleep Mode					
I_{DAC}		0.01		µA	
I_{CCT}		85		µA	

NOTES

1 All measurements are in 4xOversampling Mode unless otherwise specified.
2 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.
3 Guaranteed by Characterisation
4 Measurement made in 2xOversampling Mode.
5 I_{DAC} is the total current required to supply all DACs including the Vref circuitry.
6 All six DACs on.
7 I_{CCT} or the circuit current, is the continuous current required to drive the digital core without I_{PLL}.
8 For all inputs but PAL_NTSC and ALSB
9 For PAL_NTSC and ALSB inputs
10 For all outputs but VSO/TTX/CLAMP
11 For VSO/TTX/CLAMP output

Specifications subject to change without notice.

3.3V SPECIFICATIONS[1]

(V_{AA} = + 3.3V, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
STATIC PERFORMANCE					
Resolution (each DAC)			10	Bits	
Accuracy (each DAC)					
Integral Nonlinearity			±1.0	LSB	
Differential Nonlinearity			±1.0	LSB	Guaranteed Monotonic
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2		V	
Input Low Voltage, V_{INL}		0.8		V	
Input Current, I_{IN}			+/-1	µA	V_{IN} = 0.4 V or 2.4 V
Input Leakage Current[7]		1		µA	
Input Leakage Current[8]		200		µA	
Input Capacitance, C_{IN}		6	10	pF	
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}		2.4		V	I_{SOURCE} = 400 µA
Output Low Voltage, V_{OL}		0.4		V	I_{SINK} = 3.2 mA
Tri-State Leakage Current[9]		10		µA	
Tri-State Leakage Current[10]		200		µA	
Tri-State Output Capacitance		6	10	pF	
ANALOG OUTPUTS					
Output Current (max)	4.125	4.33	4.625	mA	R_L = 300Ω
Output Current (min)		2.16		mA	R_L = 600Ω,$R_{SET1, SET2}$ = 2400Ω
DAC to DAC Matching		0.4	2.5	%	
Output Compliance, V_{OC}			1.4	V	
Output Impedance, R_{OUT}		100		KΩ	
Output Capacitance, C_{OUT}		6p		pF	I_{OUT} = 0 mA
VOLTAGE REFERENCE[3]					
Reference Range, V_{REF}		1.235		V	$I_{VREFOUT}$=20µA
POWER REQUIREMENTS					
V_{AA}	3.15	3.3	3.6	V	
Normal Power Mode					
I_{DAC}(max)[4]		29		mA	
I_{CCT} (2xOversampling)[5,6]		42	54	mA	
I_{CCT} (4xOversampling)[5,6]		68	86	mA	
I_{PLL}		6		mA	
Sleep Mode					
I_{DAC}		0.01		µA	
I_{CCT}		85		µA	

NOTES

1 All measurements are made in 4xOversampling unless otherwise specified and are guaranteed by characterisation. In 2x Oversampling the power requirement for the ADV7194 is typically 3.0V

2 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.

3 Measurement made in 2xOversampling Mode.

4 I_{DAC} is the total current required to supply all DACs including the V_{REF} circuitry.

5 All 6 DACs on.

6 I_{CCT} or the circuit current, is the continuous current required to drive the digital core without I_{PLL}.

7 For all inputs but PAL_NTSC and ALSB

8 For PAL_NTSC and ALSB inputs

9 For all outputs but VSO/TTX/CLAMP

10 For VSO/TTX/CLAMP output

Specifications subject to change without notice.

5V DYNAMIC-SPECIFICATIONS[1]

(V_{AA} = + 5V ± 250mV, V_{REF} = 1.235 V, $R_{SET1,2}$ =1200Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Hue Accuracy		0.5			°
Color Saturation Accuracy		0.7		%	
Chroma Nonlinear Gain		0.7	0.9	±%	Referenced to 40 IRE
Chroma Nonlinear Phase		0.5		±°	
Chroma/Luma Intermod		0.1		±%	
Chroma/ Luma Gain Inequality		1.7		%	
Chroma/ Luma Delay Inequality		2.2		ns	
Luminance Nonlinearity		0.6	0.7	±%	
Chroma AM Noise		82		dB	
Chroma PM Noise		72		dB	
Differential Gain		0.1	0.3	%	
Differential Phase		0.4	0.5	°	
SNR (Pedestal)		78.5		dB rms	RMS
SNR (Pedestal)		78		dB p-p	Peak Periodic
SNR (Ramp)	61.7			dB rms	RMS
SNR (Ramp)	62			dB p-p	Peak Periodic
2XOVERSAMPLING MODE					
Differential Gain		0.4	0.5	%	
Differential Phase		0.15	0.3	°	
SNR (Pedestal)		78		dB rms	RMS
SNR (Pedestal)		78		dB p-p	Peak Periodic
SNR (Ramp)	61.7			dB rms	RMS
SNR (Ramp)	63			dB p-p	Peak Periodic

NOTES

1 All measurements are made in 4xOversampling unless otherwise specified and are guaranteed by characterisation.
2 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.

Specifications subject to change without notice.

3.3V DYNAMIC-SPECIFICATIONS[1] (V_{AA} = + 3.3V +/-150mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
Hue Accuracy		0.5		°	
Color Saturation Accuracy		0.8		%	
Luminance Nonlinearity		0.6		±%	
Chroma AM Noise		83		dB	
Chroma PM Noise		71		dB	
Chroma Nonlinear Gain		0.7		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		0.5		±°	
Chroma/Luma Intermod		0.1		±%	
Chroma/ Luma Gain Inequality		2.0		%	
Chroma/ Luma Delay Inequality		2.5		ns	
Differential Gain		0.2		%	
Differential Phase		0.5		°	
SNR (Pedestal)		78.5		dB rms	RMS
SNR (Pedestal)		78		dB p-p	Peak Periodic
SNR (Ramp)		62.3		dB rms	RMS
SNR (Ramp)		61		dB p-p	Peak Periodic
2XOVERSAMPLING MODE					
Differential Gain		0.5		%	
Differential Phase		0.2		°	
SNR (Pedestal)		78		dB rms	RMS
SNR (Pedestal)		78		dB p-p	Peak Periodic
SNR (Ramp)		62		dB rms	RMS
SNR (Ramp)		62.5		dB p-p	Peak Periodic

NOTES

1 All measurements are made in 4xOversampling unless otherwise specified.
2 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.

Specifications subject to change without notice.

5V TIMING–SPECIFICATIONS

(V_{AA} = + 5V ± 250mV, V_{REF} = 1.235 V, $R_{SET1,2}$ =1200Ω unless otherwise noted.
All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
MPU PORT[2]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6			µs	
ANALOG OUTPUTS[2]					
Analog Output Delay		8		ns	
DAC Analog Output Skew		0.1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
F_{CLOCK}		27		MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}	6			ns	
Data Hold Time t_{12}	5			ns	
Control Setup Time t_{11}	6			ns	
Control Hold Time t_{12}	4			ns	
Digital Output Access Time t_{13}		13		ns	
Digital Output Hold Time t_{14}		12		ns	
Pipeline Delay t_{15}(2xOversampling)		57		Clock cycles	
Pipeline Delay t_{15}(4xOversampling)		67		Clock cycles	
TELETEXT PORT[4]					
Digital Output Acces Time t_{16}		11		ns	
Data Setup Time t_{17}		3		ns	
Data Hold Time t_{18}		6		ns	
RESET CONTROL					
Reset Low Time		3	20	ns	
PLL[2]					
PLL Output Frequency		54		MHz	

NOTES

1 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.
2 Guaranteed by characterization.
3 Pixel Port consists of the following:
Data: P9-P0, Y9/P10-Y9/P19 Pixel Inputs
Control: HSYNC, VSYNC, BLANK
Clock: CLKIN Input
4 Teletext Port consists of the following:
Digital Output:TTXRQ
Data: TTX

Specifications subject to change without notice.

3.3V TIMING–SPECIFICATIONS[2]

(V_{AA} = + 3.3V +/-150mV, V_{REF} = 1.235 V, $R_{SET1,2}$ = 1200 Ω unless otherwise noted. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions
MPU PORT					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	After this period the 1st clock is generated
Setup Time (Start Condition), t_4	0.6			µs	Relevant for repeated Start Condition
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition) , t_8	0.6	2		µs	
ANALOG OUTPUTS					
Analog Output Delay		8		ns	
DAC Analog Output Skew		0.1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
F_{CLOCK}		27		MHz	
Clock High Time t_9	8			ns	
Clock Low Time t_{10}	8			ns	
Data Setup Time t_{11}[2]	6			ns	
Data Hold Time t_{12}[2]	4			ns	
Control Setup Time t_{11}[2]	2.5			ns	
Control Hold Time t_{12}[2]	3			ns	
Digital Output Access Time t_{13}		13		ns	
Digital Output Hold Time t_{14}		12		ns	
Pipeline Delay t_{15}		37		Clock cycles	
TELETEXT PORT[4]					
Digital Output Acces Time t_{16}		11		ns	
Data Setup Time t_{17}		3		ns	
Data Hold Time t_{18}		6		ns	
RESET CONTROL					
Reset Low Time		3	20	ns	
PLL					
PLL Output Frequency		54		MHz	

NOTES

1 Temperature range T_{MIN} to T_{MAX} : 0°C to +70°C.
2 Guaranteed by characterization.
3 Pixel Port consists of the following:
Data: P9-P0, Y9/P10-Y9/P19 Pixel Inputs
Control: $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{BLANK}$
Clock: CLKIN Input
4 Teletext Port consists of the following:
Digital Output:TTXRQ
Data: TTX

Specifications subject to change without notice.

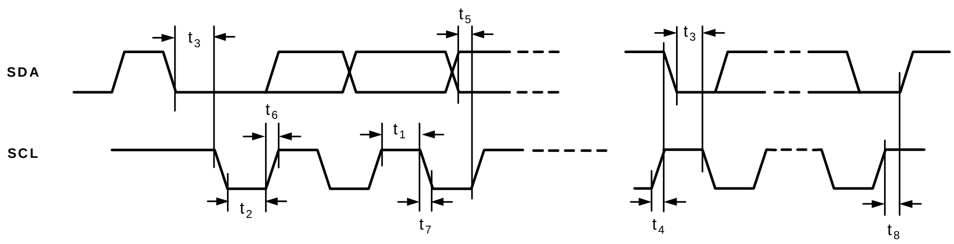


Figure 1. MPU Port Timing Diagram

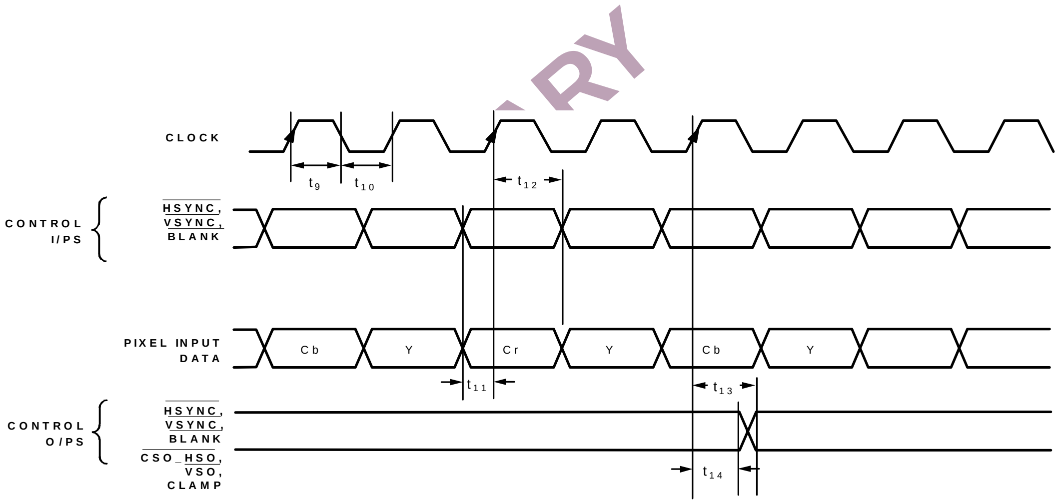


Figure 2. Pixel and Control Data Timing Diagram

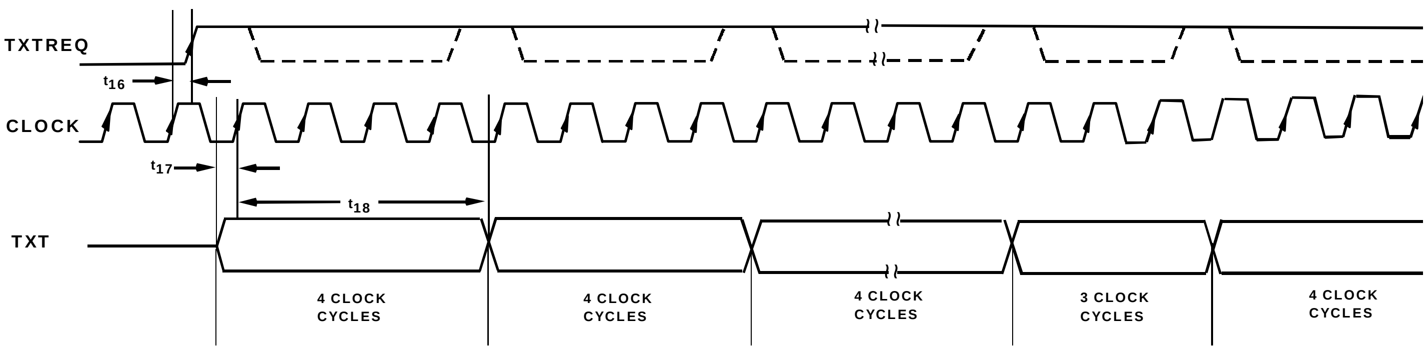


Figure 3. Teletext Timing Diagram

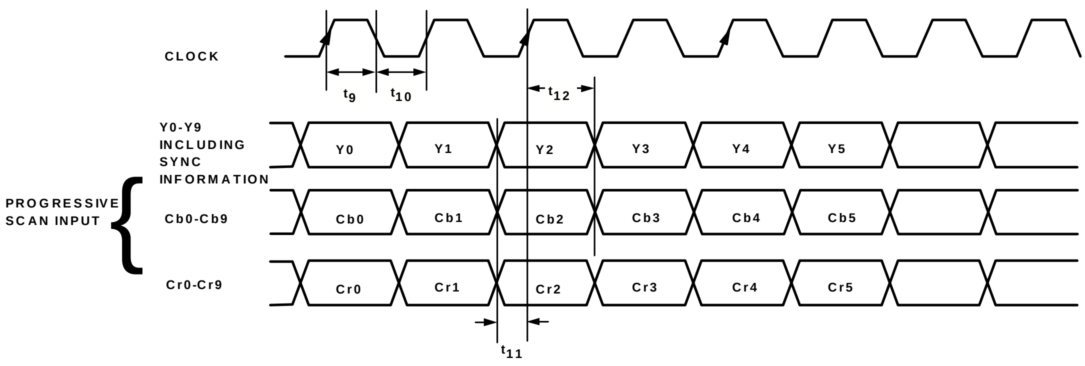


Figure 4. Progressive Scan Input Timing

ABSOLUTE MAXIMUM RATINGS *

V_{AA} to GND..7V
Voltage on any Digital Input Pin...........GND-0.5V to V_{AA}+0.5V
Storage Temperature (T_S)....................-65°C to +150°C
Junction Temperature(T_J).................................+150°C
Body Temperature (Soldering, 10 secs)................+220°C
Analog Outputs to GND[1]....................GND -0.5 to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADV7194 KST	0°C to 70°C	LQFP

PACKAGE THERMAL PERFORMANCE

The 80pin package is used for this device. The junction-to-ambient ($\theta_{J\text{-}A}$) thermal resistance in still air on a four layer PCB is 24.7°C/W.

To reduce power consumption when using this part the user can run the part on a 3.3V supply, turn off any unused DACs.

The user must at all times stay below the maximum junction temperature of 110°C. The following equation shows how to calculate this junction temperature:

Junction Temperature =
$[V_{AA} \times (I_{DAC} + I_{CCT})] \times \theta_{J\text{-}A} + 70^{o}C(T_{AMB})$

I_{DAC} = 10 mA + (sum of the average currents consumed by each powered-on DAC)

Average current consumed by each powered-on DAC = $(V_{REF} \times K) / R_{SET}$

V_{REF} = 1.235V
K = 4.2146

PIN CONFIGURATION

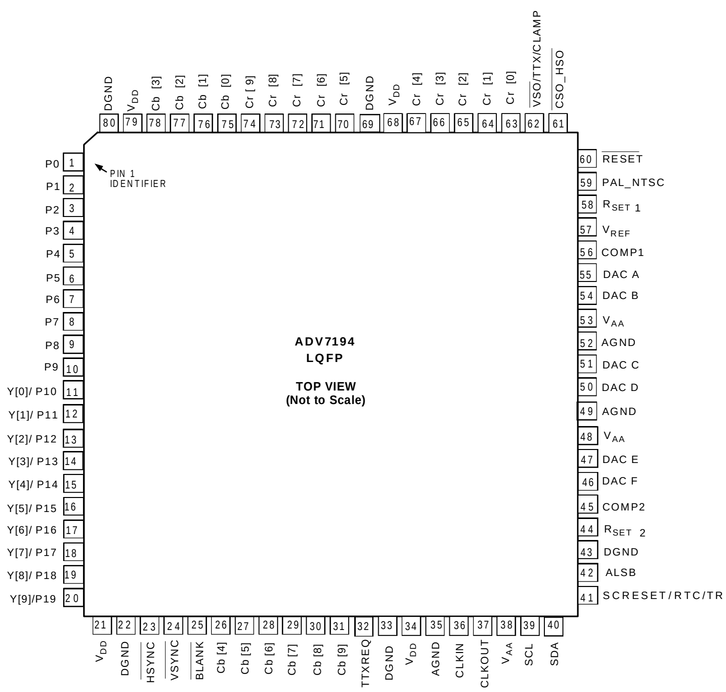


Figure 5. Pin Configuration ADV7194

PIN DESCRIPTION

Mnemonic	Input/Output	Function
AGND	G	Analog Ground
ALSB	I	TTL Address Input. This signal sets up the LSB of the MPU address.
$\overline{\text{BLANK}}$	I/O	Video Blanking Control Signal. This signal is optional. For further information see page 29.
CLKIN	I	TTL Clock Input. Requires a stable 27MHz reference clock for standard operation. Alternatively a 24.5454MHz (NTSC) or 29.5MHz (PAL) can be used for square pixel operation.
CLKOUT	O	Clock Output pin.
COMP 1	O	Compensation Pin for DACs A, B and C. Connect a 0. lμF Capacitor from COMP1 to V_{AA}.
COMP 2	O	Compensation Pin for DACs D, E and F. Connect a 0. lμF Capacitor from COMP2 to V_{AA}.
$\overline{\text{CSO\_HSO}}$	O	Dual function $\overline{\text{CSO}}$ or $\overline{\text{HSO}}$ output sync signal at TTL level.
DAC A	O	Composite/ Y (progressive scan) / Y / GREEN Analog Output. This DAC is capable ofproviding 4.33mA output.
DAC B	O	S-Video Y /Pb / U / BLUE Analog Output. This DAC is capable of providing 4.33mA output.
DAC C	O	S-Video C / Pr / V /RED Analog Output. This DAC is capable of providing 4.33mA output.
DAC D	O	Composite / Y (progressive scan) / Y / GREEN Analog Output. This DAC is capable of providing 4.33mA output.
DAC E	O	S-Video Y / Pb / U/ BLUE Analog Output. This DAC is capable of providing 4.33mA output.
DAC F	O	S-Video C / Pr /V / RED Analog Output. This DAC is capable of providing 4.33mA output
DGND	G	Digital Ground
$\overline{\text{HSYNC}}$	I/O	HSYNC (Modes 1, 2 and 3) Control Signal. This pin may be configured to be an output (Master Mode) or an input (Slave Mode) and accept Sync signals.
P0-P9	I	10-Bit or 8-Bit 4:2:2 Multiplexed YCrCb Pixel Port. The LSB of the input data is set up on pin P0 (pin number 1) in 10-Bit input mode.
Cb0 - Cb9	I	1x10Bit Progressive scan input port for Cb data.
Cr0 - Cr9	I	1x10Bit Progressive scan input port for Cr data.
PAL_NTSC	I	Input signal to select PAL or NTSC mode of operation, pin set to Logic 1 selects PAL.

SCRESET/RTC/TR	I	Multifunctional Input: Real Time Control(RTC) input, Timing Reset input, Subcarrier Reset input.
$\overline{\text{RESET}}$	I	The input resets the on-chip timing generator and sets the ADV7194 into default mode See Appendix 8 for default register settings.
R_{SET1}	I	A 1200 Ohm resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from the DAC A, B, C.
R_{SET2}	I	A 1200 Ohm resistor connected from this pin to GND is used to control full-scale amplitudes of the Video Signals from the DAC D, E, F.
SCL	I	MPU Port Serial Interface Clock Input.
SDA	I/O	MPU Port Serial Data Input/Output.
TTXREQ	O	Teletext Data Request Output Signal, used to control teletext data transfer.
V_{AA}	P	Analog Power Supply (+3.3V to + 5 V).
V_{DD}	P	Digital Power Supply (+3.3V to + 5 V).
V_{REF}	I/O	Voltage Reference Input for DACs or Voltage Reference Output (1.235V). An external V_{REF} can not be used in 4xOversampling Mode.
$\overline{\text{VSO}}$/TTX/CLAMP	I/O	Multifunctional pin. $\overline{\text{VSO}}$ Output Sync Signal at TTL level.Teletext Data Input pin. CLAMP TTL Output Signals can be used to drive external circuitry to enable clamping of all video signals.
$\overline{\text{VSYNC}}$	I/O	VSYNC control signal. This pin may be configured as an output (Master Mode) or or as an input (Slave Mode) and accept VSYNC as a control signal.
Y 0/P10 -Y9/P19	I	1x10Bit Progressive scan input for Y data or 20-Bit or 16-Bit Multiplexed YCrCb Pixel Port.

DETAILED DESCRIPTION

The ADV7194 features:

Clocking:
- **Single 27MHz Clock required to run the device**
- **4xOversampling with internal 54MHz PLL**
- **Square Pixel operation**

Advanced Power Management

Programmable Video Control features:
- **Digital Noise Reduction**
- **Black Burst Signal Generation**
- **Pedestal level**
- **Hue, Brightness, Contrast and Saturation**
- **Clamping Output signal**
- **VBI (Vertical Blanking Interval)**
- **Sub-Carrier Frequency and Phase**
- **LUMA Delay**
- **CHROMA Delay**
- **Gamma Correction**
- **Luma & Chroma Filters**
- **Luma SSAF™ (Super Sub-Alias Filter)**

Average Brightness detection
Field Counter
Interlaced/Non Interlaced Operation
Complete on-chip Video Timing Generator
Programmable Multi-Mode Master/Slave Operation
CGMS (Copy Generation Management System)
WSS (Wide Screen Signalling)
Closed Captioning support.
Teletext Insertion Port (PAL-WST)
2 Wire Serial MPU Interface
(I²C Compatible & Fast I²C)
I2C Registers synchronised to VSYNC

The ADV7194 is an integrated Digital Video Encoder that converts digital CCIR-601/656 4:2:2 10 bit (or20 bit or 8/16 bit) component video data into a standard analog baseband television signal compatible with world wide standards. Additionally there is the possibility to input video data in 3x10 bit YCrCb progressive scan format to faciliate interfacing devices such as progressive scan systems.

There are six DACs available on the ADV7194, each of these DACs is capable of providing 4.33mA of current. In addition to the composite output signal there is the facility to output S-Video (Y/C Video), RGB Video and YUV Video.
All YUV formats (SMPTRE/EBU N10, MII or Betacam) are supported.
The on-board SSAF™ (Super Sub-Alias Filter) with extended luminance frequency response and sharp stop-band attenuation enables studio quality video playback on modern TVs, giving optimal horizontal line resolution. An additional sharpness control feature allows high frequency enhancement on the luminance signal.

Digital Noise Reduction allows improved picture quality in removing low amplitude, high frequency noise.
The block diagram below shows the DNR functionality in the two modes available.

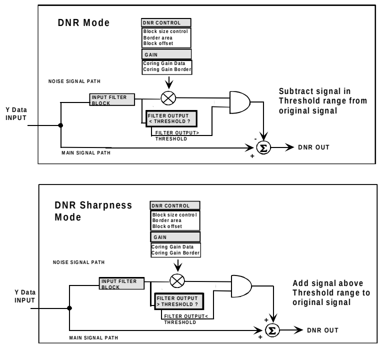


Figure xx Block diagram for DNR Mode and DNR Sharpness Mode

Programmable gamma correction is also available. The figure below shows the response of different gamma values to a ramp input signal.

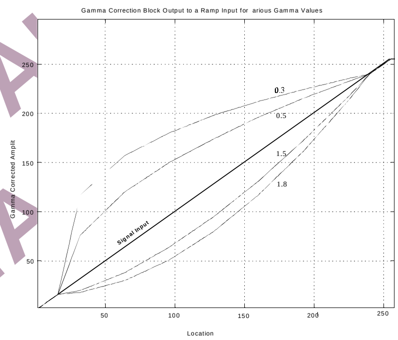


Figure xx Signal Input (Ramp) and selectable Gamma output curves

The device is driven by a 27 MHz clock. Data can be output at 27Mhz or 54Mhz (on-board PLL) when 4xOversampling is enabled.Also, the filter requirements in 4xOversampling and 2xOversampling differ, as can be seen in the figure below.

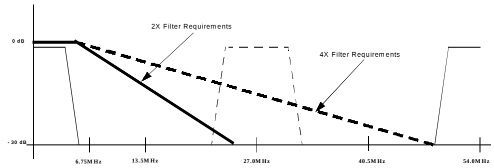
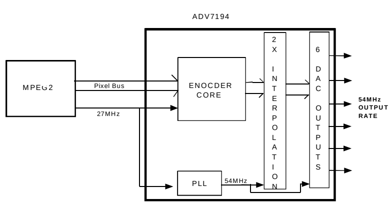


Figure xx. Output Filter Requirements in 2x- and 4xOversampling Mode



Figurexx PLL and 4xOversampling block diagram

The ADV7194 also supports both PAL and NTSC square pixel operation. In this case the encoder requires a 24.5454 MHz Clock for NTSC or 29.5MHz Clock for PAL square pixel mode operation. All internal timing is generated on-chip.

An advanced power management circuit enables optimal control of power consumption in both normal operating modes or sleep modes.

The functional features or controls are described in detail on page 26 - 30.

The Output Video Frames are synchronised with the incoming data Timing Reference Codes. Optionally the Encoder accepts (and can generate) HSYNC, VSYNC & FIELD timing signals. These timing signals can be adjusted to change pulse width and position while the part is in master mode.

HSO/CSO and VSO TTL outputs are also available and are timed to the analog output video.

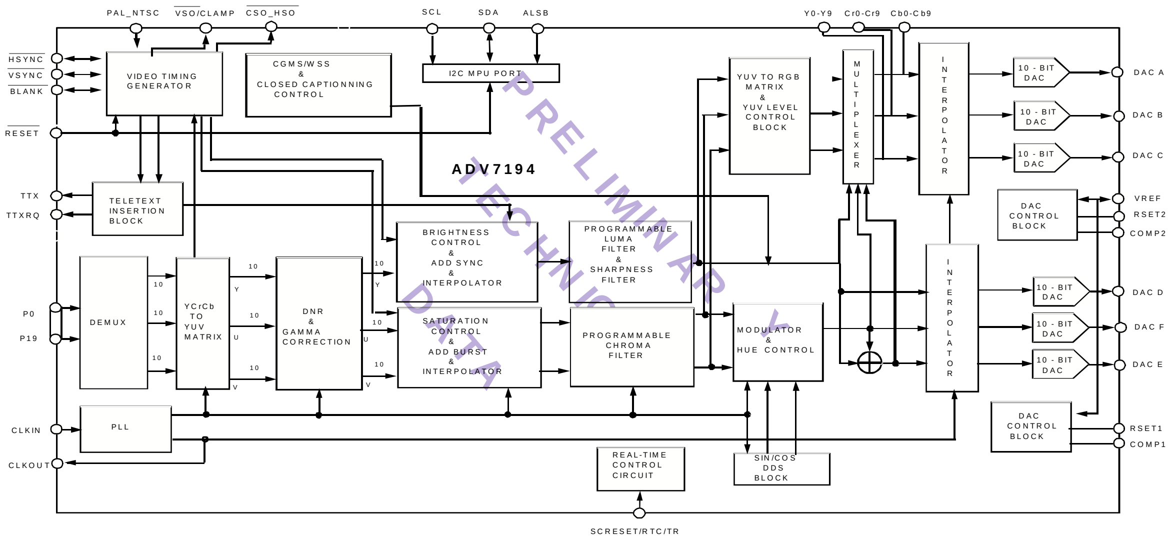
A separate teletext port enables the user to directly input teletext data during the vertical blanking interval.

The ADV 7194 also incorporates WSS and CGMS-A data control generation.

The ADV7194 modes are set up over a two wire serial bi-directional port (I^2C Compatible) with 2 slave addresses and
the device is register compatible with the ADV7172/73.

The ADV7194 is packaged in a 80-Pin LQFP package.

DETAILED BLOCKDIAGRAM



DATA PATH DESCRIPTION.

For PAL B,D,G,H,I,N and NTSC M, N modes, YCrCb 4:2:2 Data is input via the CCIR-656 /601 compatible Pixel Port at a 27MHz Data Rate. The Pixel Data is de-multiplexed to form three data paths. Y has typically a range of 16 to 235, Cr and Cb have typically a range of 128+/-112, however it is possible to input data from 1 to 254 on both Y, Cb and Cr. The ADV7194 supports PAL (B,D,G,H,I,N) and NTSC M, N (Japan)[with and without Pedestal] and PAL60 standards.

Digital Noise Reduction can be applied to the Y signal. Programmable gamma correction can also be applied to the Y signal if required.

The Y data can be manipulated for contrast control and a setup level can be added for brightness control. The Cr, Cb data can be scaled to achieve color saturation control. All settings become effective at the start of the next field when double buffering is enabled.

The appropriate sync, blank and burst levels are added to the YCrCb data. Closed-Captioning and Teletext levels are also added to Y and the resultant data is interpolated to 54MHz (4xOversampling Mode). The interpolated data is filtered and scaled by three digital FIR filters.

The U and V signals are modulated by the appropriate Sub-Carrier Sine/Cosine waveforms and a phase offset may be added onto the colour subcarrier during active video to allow hue adjustment. The resulting U and V signals are added together to make up the Chrominance Signal. The Luma (Y) signal can be delayed by up to 6 clock cycles (at 27 MHz) and the Chroma signal can be delayed by up to 8 clock cycles (at 27 MHz).

The Luma and Chroma signals are added together to make up the Composite Video Signal. All timing signals are controlled.

The YCrCb data is also used to generate RGB data with appropriate sync and blank levels. The YUV levels can be scaled to output the suitable SMPTE/EBU N10, MII or Betacam levels.

Each DAC can be individually powered off if not required. A complete description of DAC output configurations is given on page 41.

Video output levels are illustrated in Appendix 9.

When used to interface progressive scan systems, the ADV7194 allows to input YCrCb signals in Progressive Scan format (3x10Bit) before these signals are routed to the interpolation filters and the DACs.

INTERNAL FILTER RESPONSE

The Y Filter supports several different frequency responses including two low-pass responses, two notch responses, an Extended (SSAF™) response with or without gain boost/ attenuation, a CIF response and a QCIF response. The UV Filter supports several different frequency responses including five low-pass responses, a CIF response and a QCIF response, as- can be seen in the figures on the following pages.

In Extended Mode there is the option of twelve responses in the range from -4dB to +4dB. The desired response can be chosen by the user by programming the correct value via the I²C. The variation of frequency responses can be seen in the figures on the following pages. For more detailed filter plots refer to the application note ANxxx.

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE[1] (dB)	3dB BANWIDTH[2] (MHz)	STOPBAND CUTOFF[3](MHz)	STOPBAND ATTENUATION[4](dB)
	MR04	MR03	MR02				
LOW PASS (NTSC)	0	0	0	0.16	4.24	6.05	-75.2
LOW PASS (PAL)	0	0	1	0.1	4.81	6.41	-64.6
NOTCH (NTSC)	0	1	0	0.09	2.27/4.9/6.6	8.03	-87.3
NOTCH (PAL)	0	1	1	0.1	3.1/5.6/6.38	8.02	-79.7
EXTENDED (SSAF)	1	0	0	0.043	6.45	8.03	-86.6
CIF	1	0	1	0.127	3.02	5.09	-62.6
QCIF	1	1	0	Monotonic	1.5	3.74	-88.2

Figure 6. Luminance Internal Filter Specifications (4xOversampling)

FILTER TYPE	FILTER SELECTION			PASSBAND RIPPLE[1](dB)	3dB BANWIDTH[2] (MHz)	STOPBAND CUTOFF[3](MHz)	STOPBAND ATTENUATION[4](dB)
	MR07	MR06	MR05				
1.3MHzLOW PASS	0	0	0	0.09	1.397	2.46	-83.9
0.65MHzLOW PASS	0	0	1	Monotonic	0.653	2.41	-71.1
1.0MHz LOW PASS	0	1	0	Monotonic	1.0	1.89	-64.43
2.0MHz LOW PASS	0	1	1	0.048	2.22	3.1	-65.9
3.0MHz LOW PASS	1	0	0	Monotonic	3.2	5.3	- 84.5
CIF	1	0	1	Monotonic	0.653	2.41	-71.1
QCIF	1	1	0	Monotonic	0.5	1.75	-33.1

Figure 7. Chrominance Internal Filter Specifications (4xOversampling)

[1] Passband Ripple refers to the maximum fluctuations from the 0dB response in the passband, measured in [dB]. The pass band is defined to have 0 [Hz] to fc [Hz] frequency limits for a low pass filter, 0[Hz] to f1[Hz] and f2 [Hz] to infinity for a notch filter, where fc, f1, f2 are the -3dB points.

[2] 3dB bandwidth refers to the -3dB cut off frequency.

[3] Stopband Cutoff refers to the frequency [MHz] at attenuation point [dB] refered to under note 4.

[4] Stopband Attenuation refers to the attenuation[dB] at the frequency [MHz] refered to under note 3.

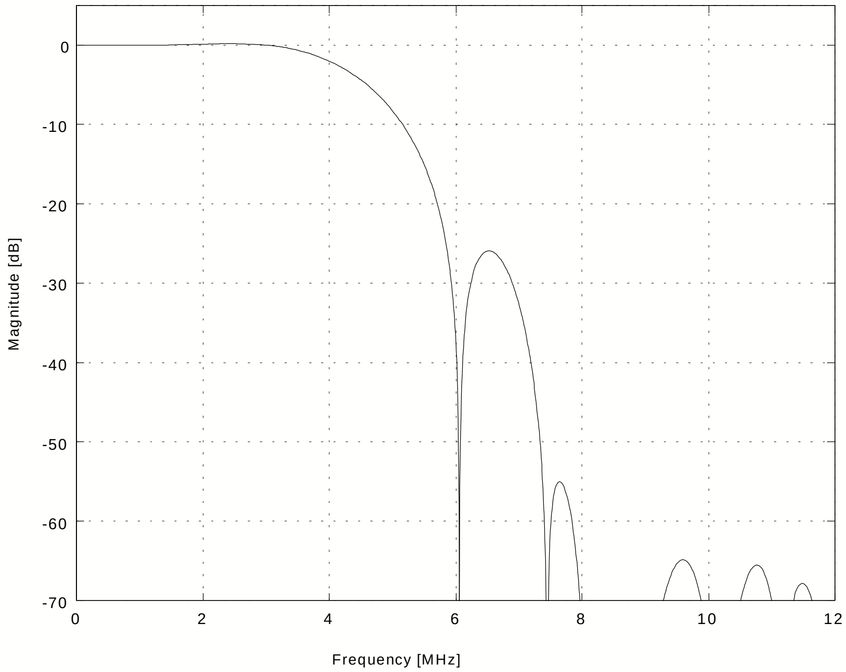


Figure 8 Luma NTSC Low Pass Filter (4xOversampling)

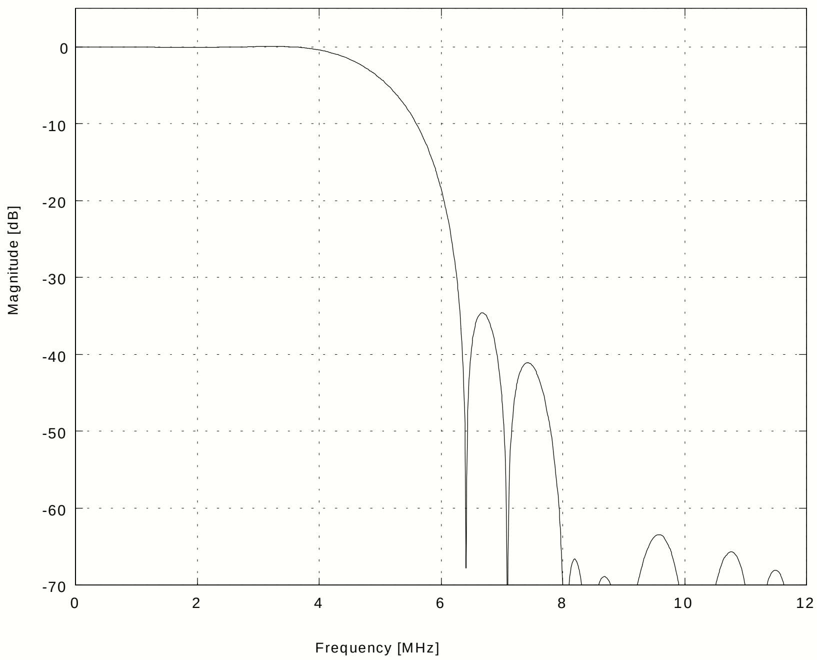


Figure 9 Luma PAL Low Pass Filter (4xOversampling)

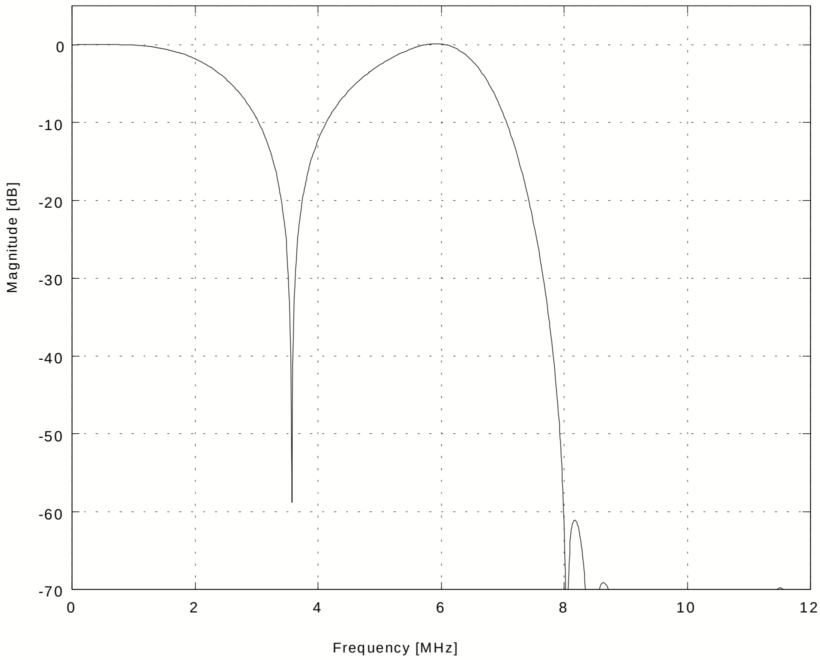


Figure 10 Luma NTSC Notch Filter (4xOversampling)

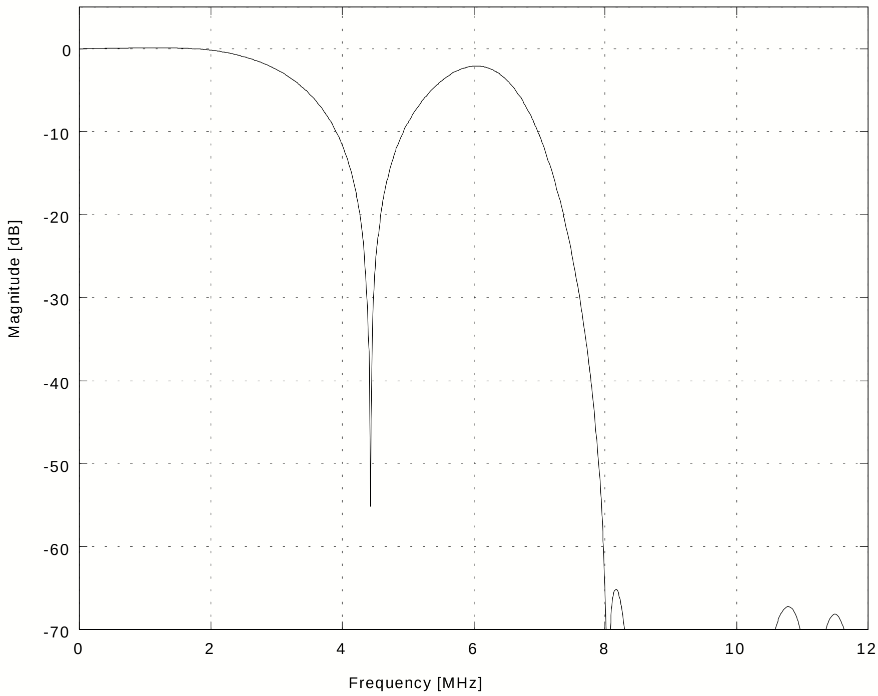


Figure 11 Luma PAL Notch Filter (4xOversampling)

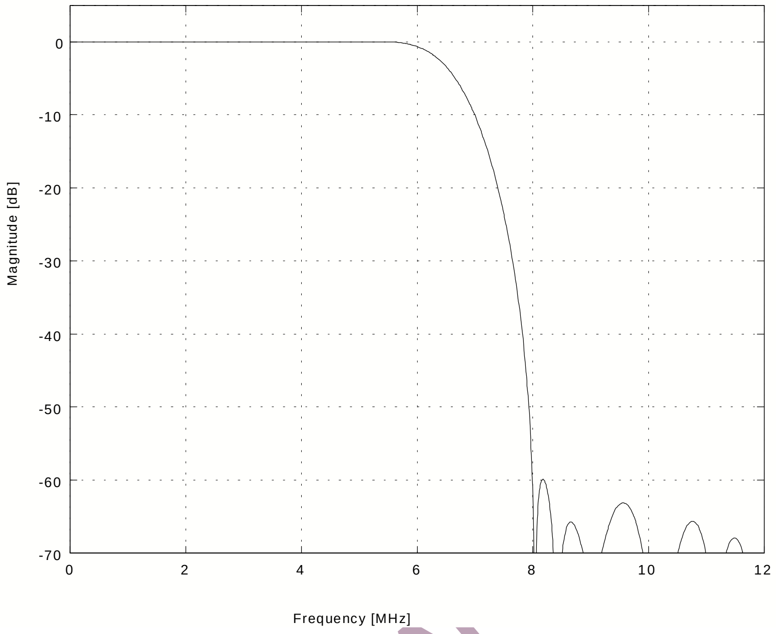


Figure 12 Extended (SSAF) Luma Filter (4xOversampling)

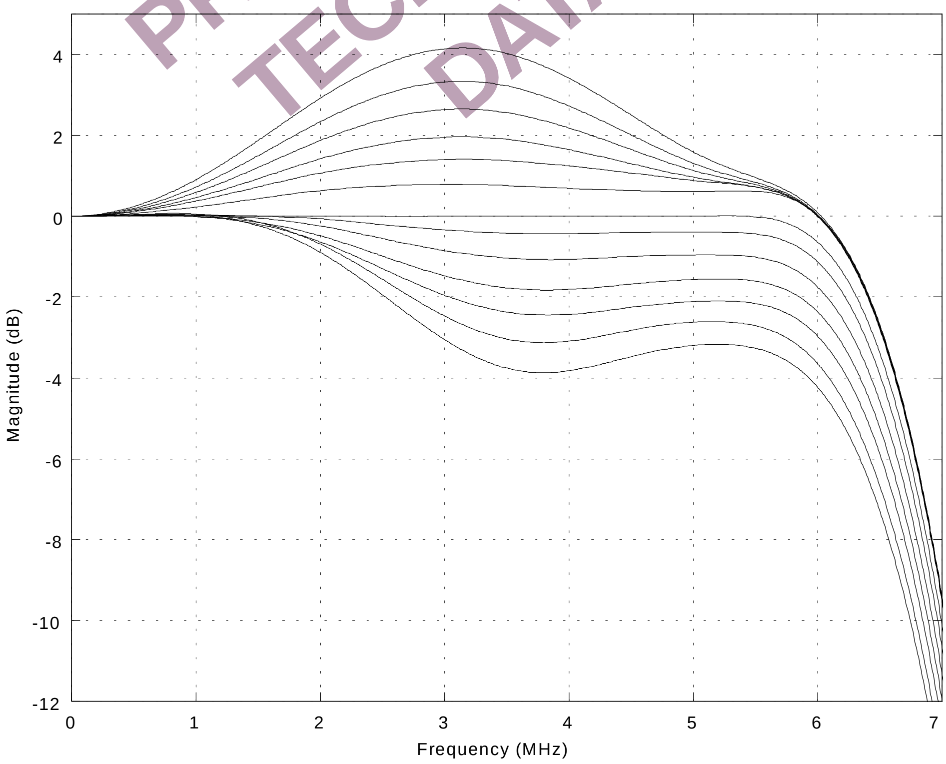


Figure 13. Extended (SSAF) Luma Filter and programmable gain/attenuation, showing range +4/-12 dB (4xOversampling Mode)

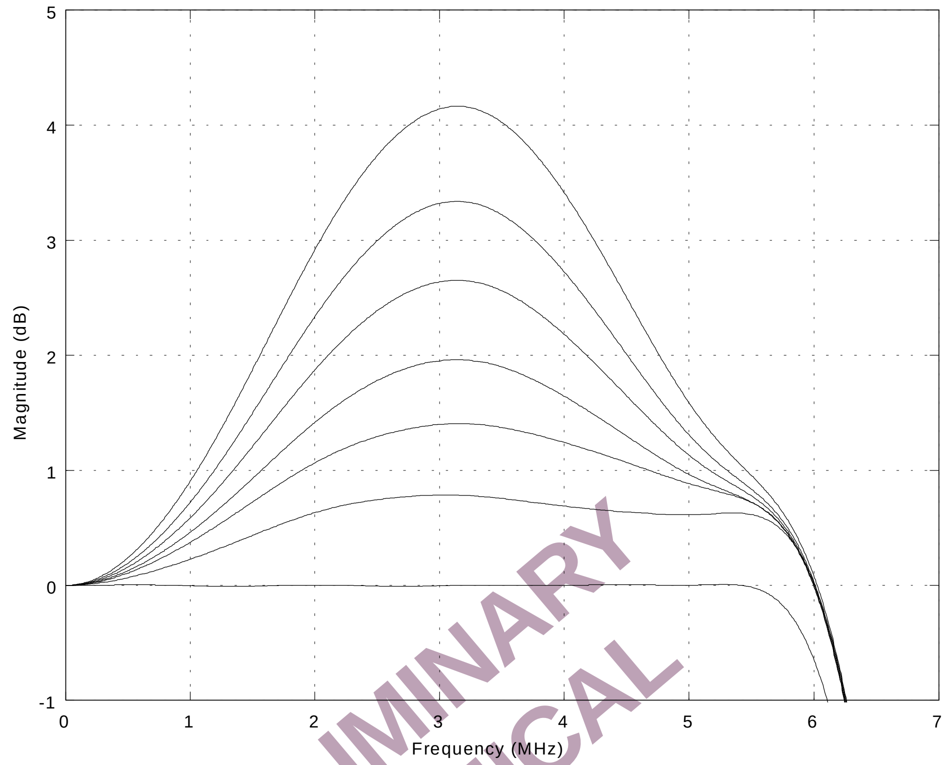


Figure 14 Extended (SSAF) Luma Filter and programmable ga
showing range -0/+4 dB (4xOversampling Mode)

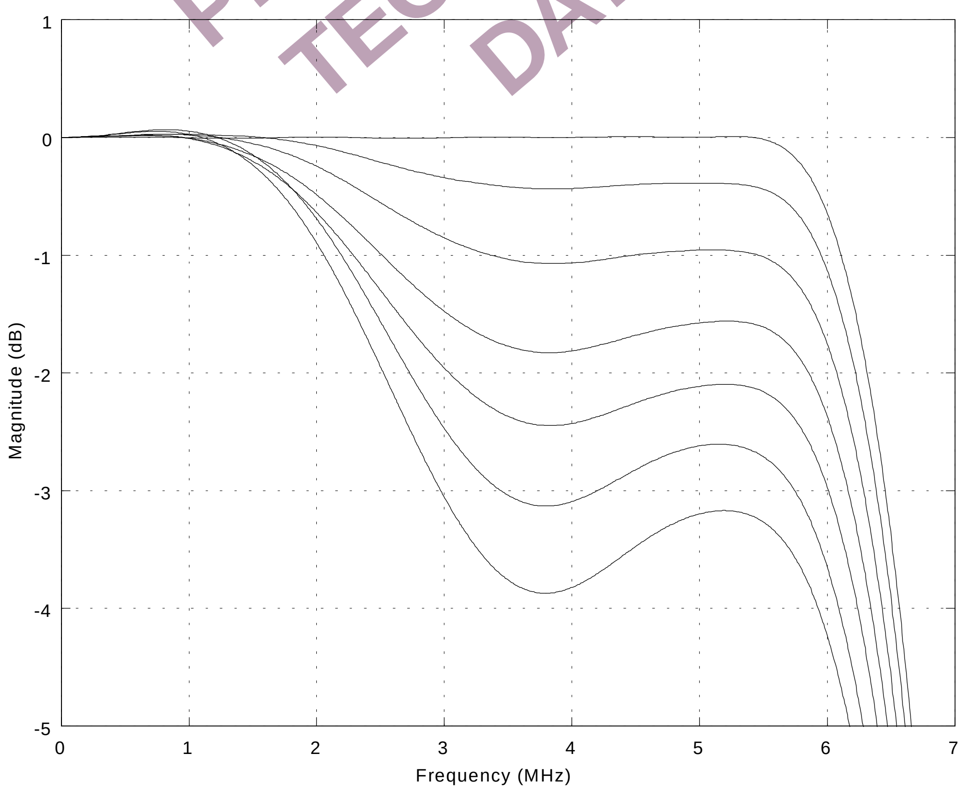


Figure 15. Extended (SSAF) Luma Filter and programmable attenuation,
showing range 0/-4dB (in 4xOversampling Mode)

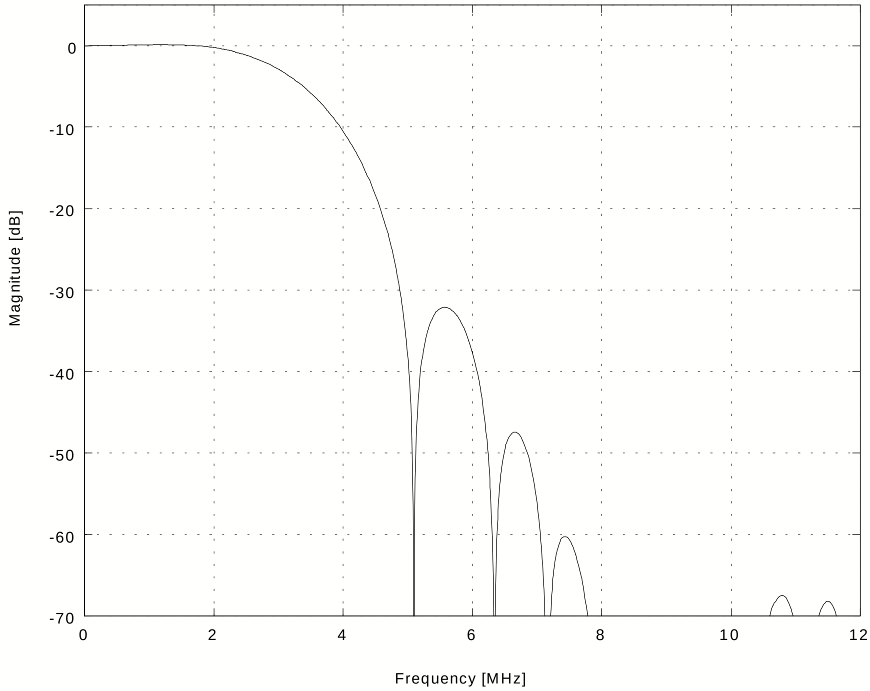


Figure 16 Luma CIF Filter (4xOversampling)

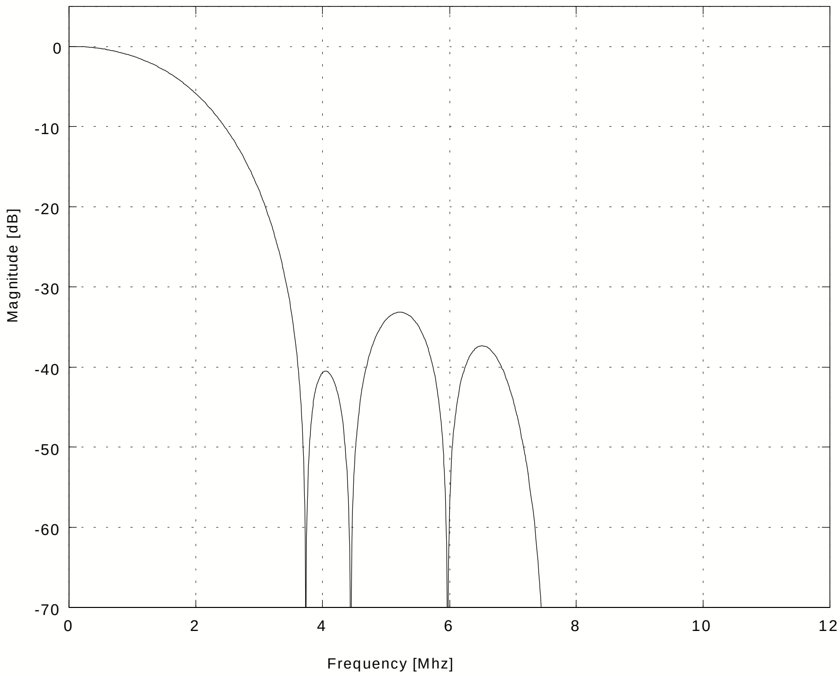


Figure 17 Luma QCIF Filter (4xOversampling)

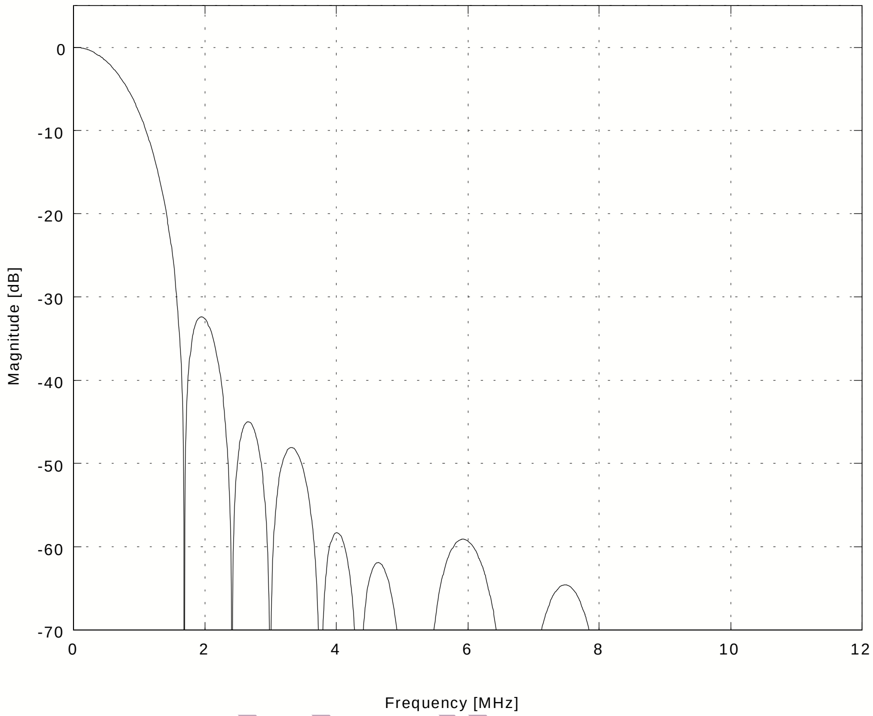


Figure 18 Chroma 0.65MHz Low Pass Filter (4xOversampling)

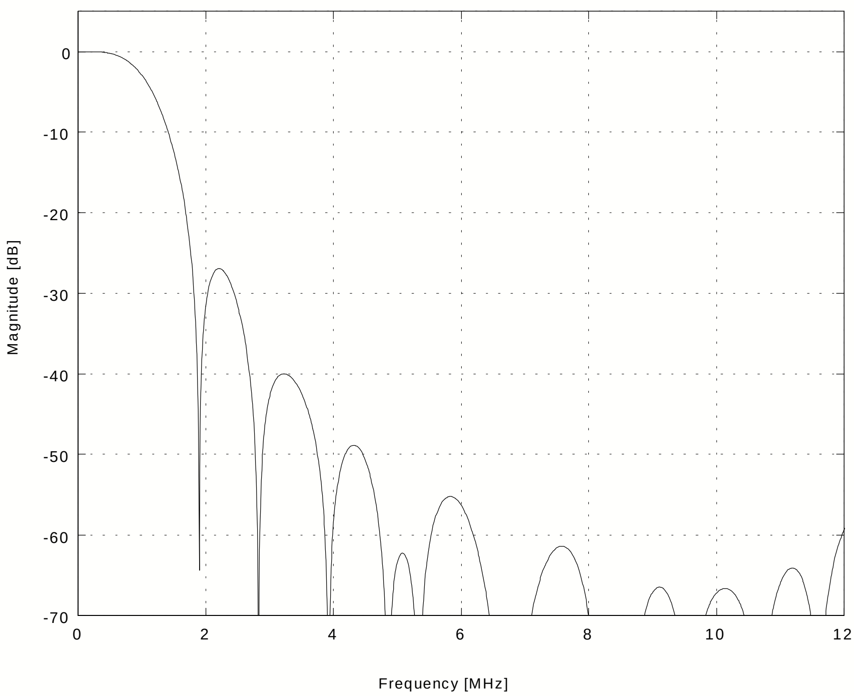


Figure 19 Chroma 1.0MHz Low Pass Filter (4xOversampling)

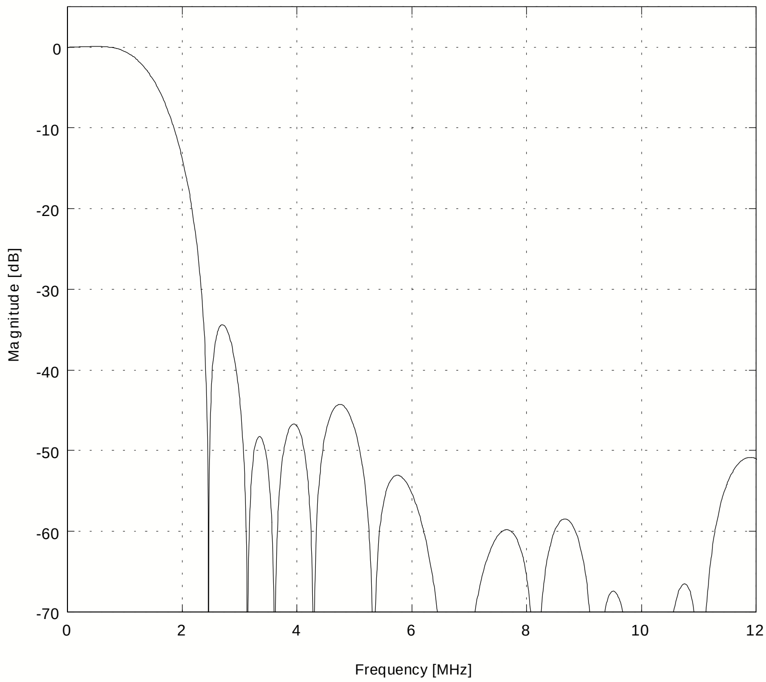


Figure 20 Chroma 1.3MHz Low Pass Filter (4xOversampling)

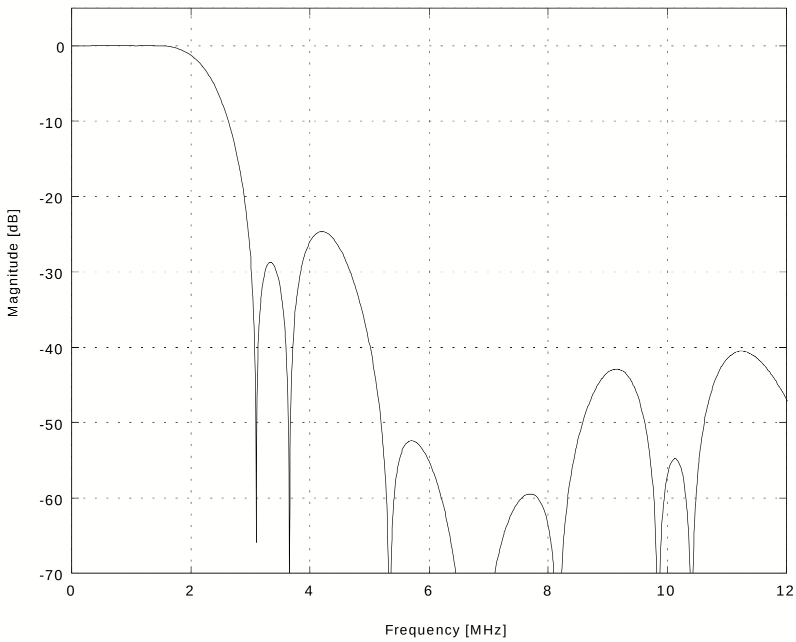


Figure 21 Chroma 2.0MHz Low Pass Filter (4xOversampling)

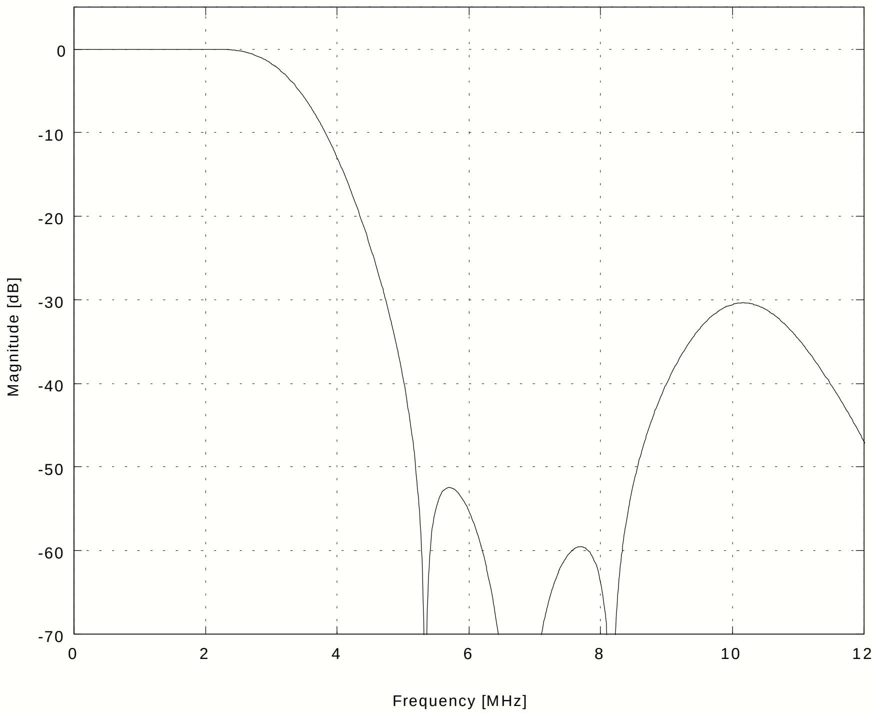


Figure 22 Chroma 3.0MHz Low Pass Filter (4xOversampling)

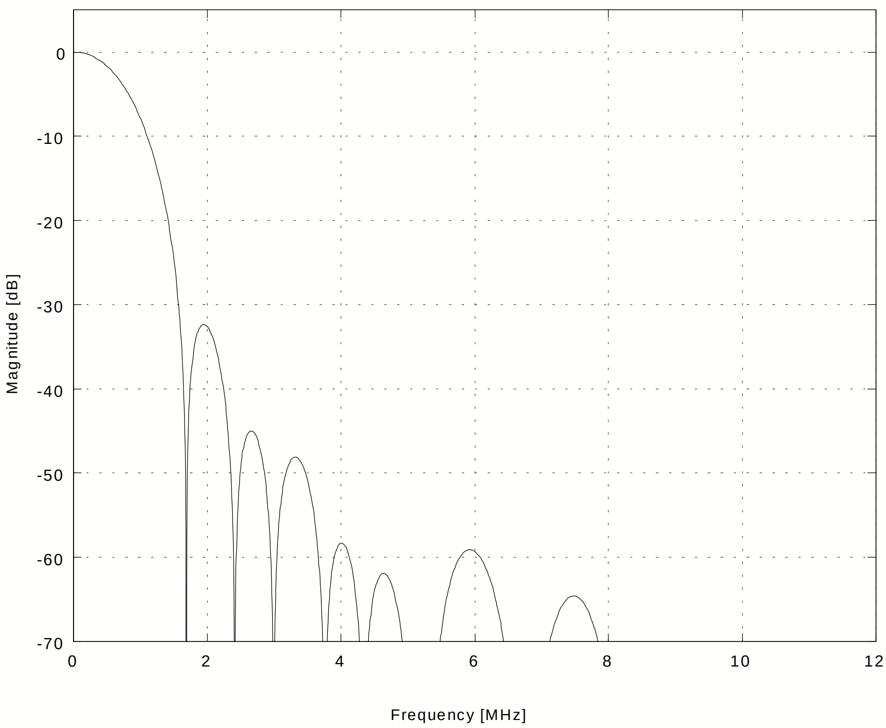


Figure 23 Chroma CIF Filter (4xOversampling)

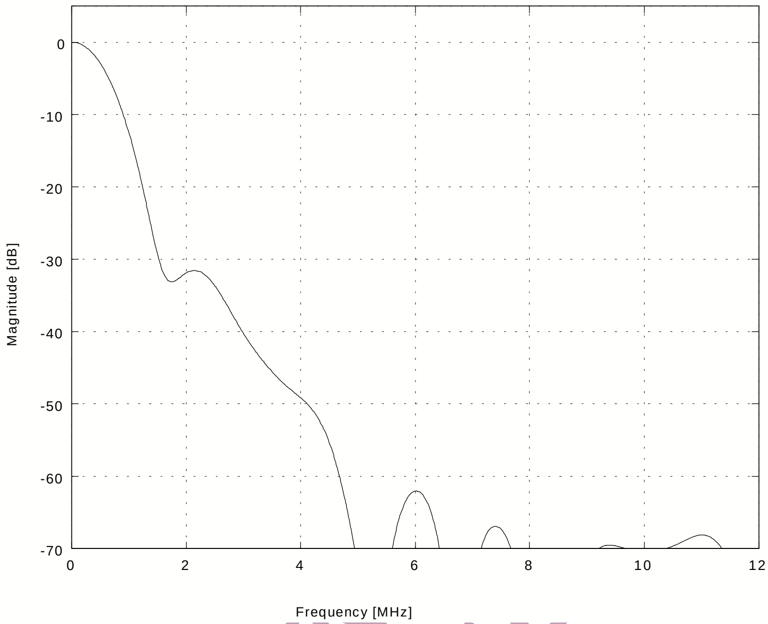


Figure 24 Chroma QCIF Filter (4xOversampling)

FEATURES: FUNCTIONAL DESCRIPTION

BLACK BURST OUTPUT

It is possible to output a black burst signal from two DACs. This signal output is very useful for professional video equipment since it enables two video sources to be locked together.[Mode Register 9].

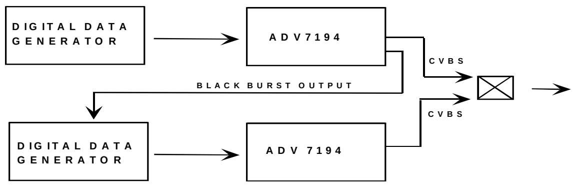


Figure 25 Possible application for the Black Burst Output signal.

BRIGHTNESS DETECT

This feature is used to monitor the average brightness of the incoming Y video signal on a field by field basis . The information is read from the I2C and based on this information the color saturation, contrast and brightness controls can be adjusted (for example to compensate for very dark pictures).[Brightness Detect Register].

CHROMA/LUMA DELAY

The luminance data can be delayed by maximum of 6 clock cycles. Additionally the Chroma can be delayed by a maximum of 8 clock cycles (one clock cycle at 27MHz). [Timing Register 0 and Mode Register 9].

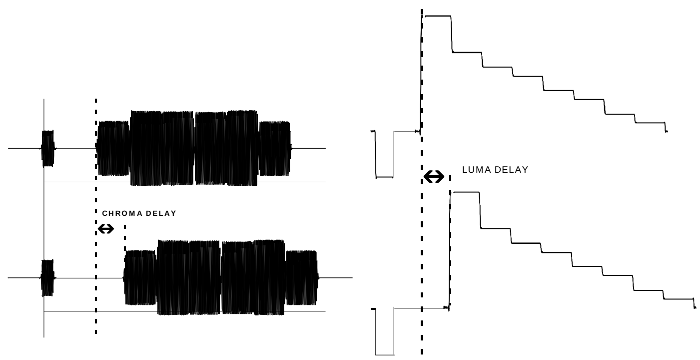


Figure 26 Chroma Delay / Luma Delay

CLAMP OUTPUT

The ADV7194 has a programmable clamp TTL output signal. This clamp signal is programmable to the front and back porch. The clamp signal can be varied by 1-3 clock cycles in a positive and negative direction from the default position. [Mode Register 5, Mode Register 7].

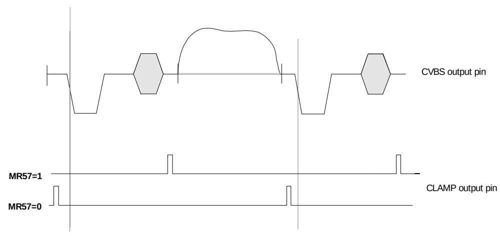


Figure 27 Clamp output timing

$\overline{\text{CSO}}$, $\overline{\text{HSO}}$ AND $\overline{\text{VSO}}$ OUTPUTS

The ADV7194 supports 3 output timing signals, $\overline{\text{CSO}}$ (composite sync signal), $\overline{\text{HSO}}$ (horizontal sync signal) and $\overline{\text{VSO}}$ (vertical sync signal). These output TTL signals are aligned with the analog video outputs. See figure below for an example of these waveforms.[Mode Register 7].

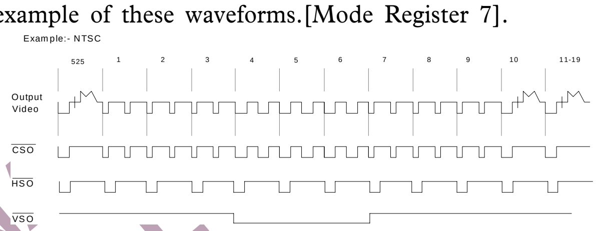


Figure 28 $\overline{\text{CSO}}$, $\overline{\text{HSO}}$, $\overline{\text{VSO}}$ timing diagram

COLOR BAR GENERATION

The ADV7194 can be configured to generate 100/7.5/75/7.5 colorbars for NTSC or 100/0/75/0 colorbars for PAL. [Mode Register 4].

COLOR BURST CONTROL

The burst information can be switched on and off the composite and chroma video output.[Mode Register 4].

COLOR CONTROLS

The ADV7194 allows the user to control the brightness, contrast, hue and saturation of the color. The control registers may be double buffered, meaning that any modification to the registers will be done outside the active video region and therefore changes made will not be visible during active video.

Contrast Control

Contrast adjustment is achieved by scaling the Y input data by a factor programmed by the user. This factor allows the data to be scaled between 0% and 150%. [Contrast Control Register].

Brightness Control

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level may be added onto the Y data. For NTSC with pedestal the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and PAL the setup can vary from -7.5IRE to 15IRE. [Brightness Control Register].

Color Saturation

Color adjustment is achieved by scaling the U and V input data by a factor programmed by the user.This factor allows the data to be scaled between 0% and 200%. [U Scale Register and V Scale Register].

Hue Adjust Control

The hue adjustment is achieved on the composite and chroma outputs by adding a phase offset onto the color subcarrier in the active video but leaving the color burst unmodified i.e. only the phase between the video and the colorburst is modified and hence the hue is shifted. The ADV7194 provides a range of +/- 22° in increments of 0.17578125°.[Hue Adjust Register].

CHROMINANCE CONTROL

The color information can be switched on and off the composite, chroma and color component video outputs. [Mode Register 4].

UNDERSHOOT LIMITER

A limiter is placed after the digital filters. This prevents any synchronization problems for TVs. The level of undershoot is programmable between -1.5 IRE, -6 IRE, -11 IRE when operating in 4xOversampling Mode. In 2xOversampling Mode the limits are -7.5IRE and 0 IRE .[Mode Register 9 and Timing Register 0].

DIGITAL NOISE REDUCTION

DNR is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal ('DNR Input Select'). The absolute value of the filter output is compared to a programmable threshold value ('DNR Threshold Control'). There are two DNR modes available: DNR Mode and DNR Sharpness Mode.
In DNR Mode, if the absolute value of the filter output is smaller than the threshold, it is assumed to be noise. A programmable amount ('Coring Gain Control') of this noise signal will be subtracted from the original signal.
In DNR Sharpness Mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise, as before. Otherwise, if the level exceeds the threshold, now being identified as a valid signal, a fraction of the signal ('Coring Gain Control') will be added to the original signal in order to boost high frequency components and to sharpen the video image.
In MPEG systems it is common to process the video information in blocks of 8x8 pixels for MPEG2 systems, or 16x16 pixels for MPEG1 systems ('Block Size Control'). DNR can be applied to the resulting block transition areas which are known to contain noise. Generally the block transition area contains 2 pixels. It is possible to define this area to contain 4 pixels ('Border Area Control').
It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the ('Block Offset Control'). [Mode Register 8, DNR Registers 0 -2].

DOUBLE BUFFERING

Double buffering can be enabled or disabled on the following registers: Closed Captioning Registers, Brightness Control, V-Scale, U-Scale, Contrast Control, Hue Adjust Register and the Gamma Curve Select bit. These registers are updated once per Field on the falling edge of the $\overline{VSYNC}$ signal. Double Buffering improves the overall performance of the ADV7194, since modifications to register settings will not be made during active video, but take effect on the start of the active video. [Mode Register 8].

GAMMA CORRECTION CONTROL

Gamma correction may be performed on the Luma data. The user has the choice to use either of two different gamma curves, A or B. At any one time one of these curves is operational if gamma correction is enabled. Gamma correction allows the mapping of the Luma data to a user defined function. [Mode Register 8, Gamma Correction Registers 0-13].

PEDESTAL CONTROL

In NTSC mode it is possible to have the pedestal signal generated on the output video signal.
[Mode Register 2].

POWER-ON RESET

After power-up, it is necessary to execute a $\overline{RESET}$ operation. A reset occurs on the falling edge of a high to low transistion on the $\overline{RESET}$ pin. This initializes the pixel port such that the data on the pixel inputs pins is ignored. See Appendix 8 for the register settings after $\overline{RESET}$ is applied. See page 30 for $\overline{RESET}$ timing sequence .

PROGRESSIVE SCAN INPUT

It is possible to input data to the ADV7194 in progressive scan format. For this purpose the input pins Y0-9, Cb0-Cb9 and Cr0-Cr9 accept 10-bit Y data, 10-bit Cr data and 10-bit Cb data. The data is clocked into the part at 27Mhz. The data is then filtered and sinc corrected in an 2xInterpolation filter and then output to three video DACs at 54 Mhz (to interface to a progressive scan monitor, for example).

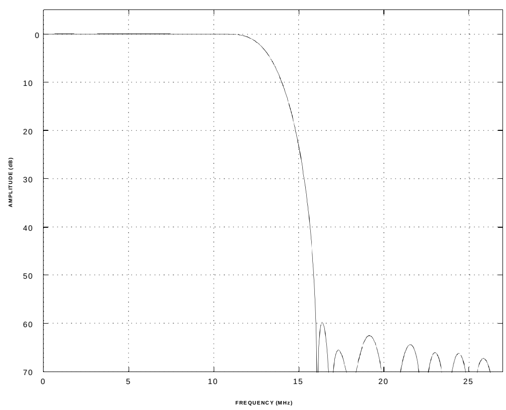


Figure 29. Plot of the interpolation filter for the Y data

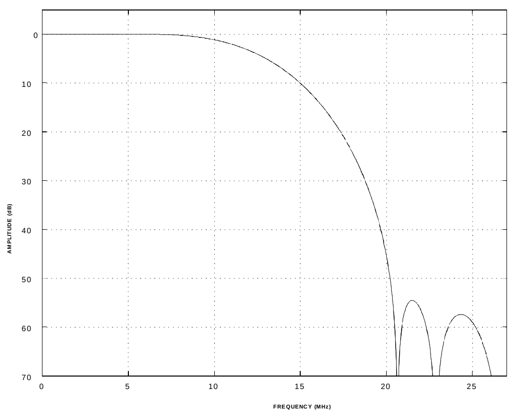


Figure 30. Plot of the interpolation filter for the CrCb data

It is assumed that there is no color space conversion or any other such operation to be performed on the incoming data. Thus if these DAC outputs are to drive a TV, all relevant timing and synchronization data should be contained in the incoming digital *Y* data.

The block diagram below shows a possible configuration for progressive scan mode using the ADV7194.

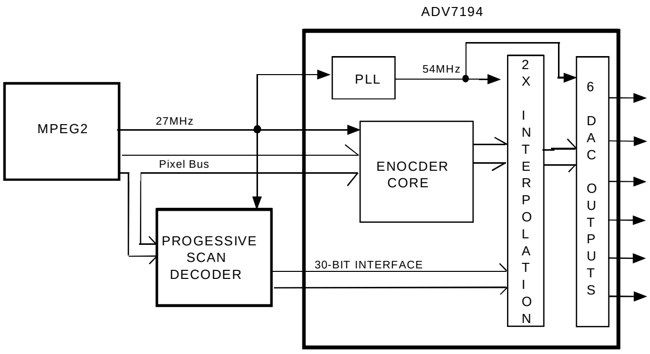


Figure 31. Block diagram of using the ADV7194 in Progressive Scan Mode

The progressive scan decoder deinterlaces the data from the MPEG2 decoder. This now means that there are 525 video lines per field in NTSC mode and 625 video lines per field in PAL mode. The duration of the video line is now 32 µs.
It is important to note that the data from the MPEG2 decoder is in 4:2:2 format. The data output from the progressive scan decoder is in 4:4:4 format. Thus it is assumed that some form of interpolation on the color component data is performed in the progressive scan decoder IC. [Mode Register 8].

REAL TIME CONTROL , SUBCARRIER RESET AND TIMING RESET

Together with the SCRESET/RTC /TR pin and of Mode Register 4 ('Genlock Selection'), the ADV7194 can be used in (a) Timing Reset Mode, (b) Subcarrier Phase Reset Mode or (c) RTC Mode.

(a) A TIMING RESET is achieved in holding this pin high. In this state the horizontal and vertical counters will remain reset. On releasing this pin (set to low), the internal counters will commence counting again. The minimum time the pin has to be held high is 37ns (1 clock cycle at 27MHz), otherwise this reset signal might not be recognized.

(b) The SUBCARRIER PHASE will reset to that of Field 0 at the start of the following field when a low to high transition occurs on this input pin.

(c) In RTC MODE, the ADV7194 can be used to lock to an external video source.
The real time control mode allows the ADV7194 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device that outputs a digital datastream in the RTC format (such as a ADV7185 video decoder, see page 31), the part will automatically change to the compensated subcarrier frequency on a line by line basis. This digital datastream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is 2 clock cycles long. 00Hex should be written into all four Subcarrier Frequency registers when using this mode.

[Mode Register 4].

SCH PHASE MODE

The SCH phase is configured in default mode to reset every four(NTSC) or eight(PAL) fields to avoid an accumulation of SCH phase error over time. In an ideal system, zero SCH phase error would be maintained forever, but in reality, this is impossible to achieve due to clock frequency variations. This effect is reduced by the use of a 32-bit DDS, which generates this SCH.
Resetting the SCH phase every four or eight fields avoids the accumulation of SCH phase error, and results in very minor SCH phase jumps at the start of the four or eight field sequence.
Resetting the SCH phase should not be done if the video source does not have stable timing or the ADV7194 is configured in RTC mode. Under these conditions (unstable video) the Subcarrier Phase Reset should be enabled but no RESET applied. In this configuration the SCH Phase will never be reset, this means that the output video will now track the unstable input video. The Subcarrier Phase Reset when applied will reset the SCH phase to Field 0 at the start of the next field (e.g. Subcarrier Phase Reset applied in Field 5(PAL) on the start of the next field SCH phase will be reset to Field 0).
[Mode Register 4].

SLEEP MODE

If after RESET , the SCRESET/RTC/TR and NTSC_PAL pins are both set high , the ADV7194 will power up in Sleep Mode to facilitate low power consumption before all registers have been initialised.
If 'Power-Up In Sleep Mode' is disabled, Sleep Mode control passes to the 'Sleep Mode' control in Mode Register 2 (i.e. control via I2C). [Mode Register 2 and Mode Register 6].

SQUARE PIXEL MODE

The ADV7194 can be used to operate in square pixel mode. For NTSC operation an input clock of 24.5454MHz is required. Alternatively, for PAL operation, an input clock of 29.5MHz is required. The internal timing logic adjusts accordingly for square pixel mode operation.Square pixel mode is not available in 4xOversampling mode. [Mode Register 2].

VERTICAL BLANKING DATA INSERTION AND BLANK INPUT

It is possible to allow encoding of incoming YCbCr data on those lines of VBI that do not have line sync or pre/post-equalisation pulses . This mode of operation is called "Partial Blanking". It allows the insertion of any VBI data (Opened VBI) into the encoded output waveform, this data is present in digitized incoming YCbCr data stream (e.g. WSS data, CGMS, VPS etc.). Alternatively the entire VBI may be blanked (no VBI data inserted) on these lines. VBI is available in all timing modes.

The complete VBI comprises of the following lines:
525/60 systems, Lines 525 to 21 for field one and Lines 262 to Line 284 for field two.
625/50 systems, Lines 624 to Line 22 and Lines 311 to 335.
The "Opened VBI" consists of:
525/60 systems, Lines 10 to 21 for field one and second half of Line 273 to Line 284 for field two.
625/50 systems, Line 7 to 22 and Lines 319 to 335.
[Mode Register 3].

It is possible to allow control over the BLANK signal using Timing Register 0. When the BLANK input is enabled (TR03 = '0' and input pin tied low), the BLANK input can be used to input externally generated blank signals in Slave Mode 1, 2 or 3. When the BLANK input is disabled (TR03 = '1' and input pin tied low or tied high) the BLANK input is not used and the ADV7194 automatically blanks all normally blank lines as per CCIR-624. [Timing Register 0].

YUV LEVELS

This functionality allows the ADV7194 to output SMPTE levels or Betacam levels on the Y output when configured in PAL or NTSC mode.

	Sync	Video
Betacam	286mV	714mV
SMPTE	300mV	700mV
MII	300mV	700mV

As the datapath is branched at the output of the filters the luma signal relating to the CVBS or S-Video Y/C output is unaltered. It is only the Y output of the YUV outputs which is scaled. This control allows color component levels to have a peak-peak amplitude of 700 mV, 1000mV or the default values of 934 mV in NTSC and 700mV in PAL. [Mode Register 5].

20/16-BIT INTERFACE

It is possible to input data in 20-bit or 16-bit format. In this case the interface only operates if the data is accompanied by separate HSYNC/VSYNC/BLANK signals. 16-bit mode is not available in Slave Mode 0 since EAV/SAV timing codes are used.
[Mode Register 8].

4xOVERSAMPLING AND INTERNAL PLL

It is possible to operate all six DACs at 27MHz (2xOversampling) or 54 MHz (4xOversampling).
The ADV7194 is supplied with a 27MHz clock synced with the incoming data.There are two options available: to run the device throughout at 27MHz or to enable the PLL. In the latter case even if the incoming data runs at 27MHz, 4xOversampling and the internal PLL will output the data at 54MHz.
Note In 4xOversampling Mode the requirements for the optional output filters are different than from those in 2xOversampling. For further details see Appendix 6. [Mode Register 1, Mode Register 6].

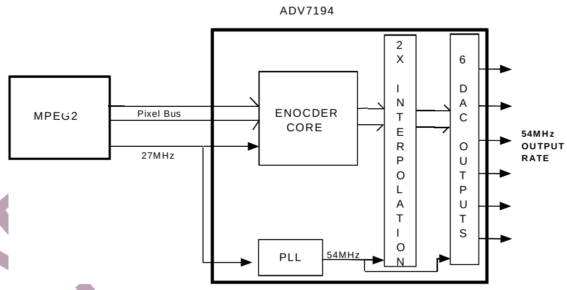


Figure32 PLL and 4xOversampling block diagram

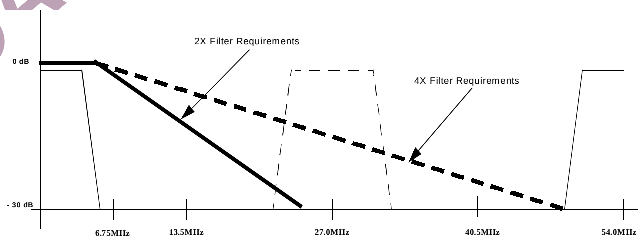


Figure 33. Output Filter Requirements in 2x- and 4xOversampling Mode

VIDEO TIMING DESCRIPTION.

The ADV7194 is intended to interface to off-the-shelf MPEG1 and MPEG2 Decoders. As a consequence the ADV7194 accepts 4:2:2 YCrCb Pixel Data via a CCIR-656 Pixel Port and has several Video Timing Modes of operation that allow it to be configured as either System Master Video Timing Generator or a Slave to the System Video Timing Generator. The ADV7194 generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The ADV7194 calculates the width and placement of analog sync pulses, blanking levels and color burst envelopes. Color bursts are disabled on appropriate lines and serration and equalisation pulses are inserted where required.

In addition the ADV7194 supports a PAL or NTSC square pixel operation (2xOversampling Mode only). The part requires an input pixel clock of 24.5454MHz for NTSC square pixel operation and an input pixel clock of 29.5MHz for PAL square pixel operation. The internal horizontal line counters place the various video waveform sections in the correct location for the new clock frequencies.

The ADV7194 has 4 distinct Master and 4 distinct Slave timing configurations.Timing Control is establised with the bi-directional HSYNC, BLANK and VSYNC pins. Timing Register 1 can also be used to vary the timing pulse widths and where they occur in relation to each other.
[Mode Register 2, Timing Register 0,1]

RESET SEQUENCE

When RESET becomes active the ADV7194 reverts to the default output configuration (see Appendix 8 for register settings).
The ADV7194 internal timing is under the control of the logic level on the NTSC_PAL pin.
When RESET is released Y, Cr, Cb values corresponding to a black screen are input to the ADV7194. Output timing signals are still suppressed at this stage. DACs A,B C are switched off and DACs D,E, F are switched on.
When the user requires valid data, 'Pixel Data Valid' Control is enabled (MR26 = '1') to allow the valid pixel data to pass through the encoder. Digital output timing signals become active and the encoder timing is now under the control of the Timing Registers. If at this stage, the user wishes to select a different video standard to that on the NTSC_PAL pin, 'Standard I2C' Control should be enabled (MR25 = '1') and the video standard required is selected by programming Mode Register 0 ('Output Video Standard Selection'). Figure 34 illustrates the RESET sequence timing.

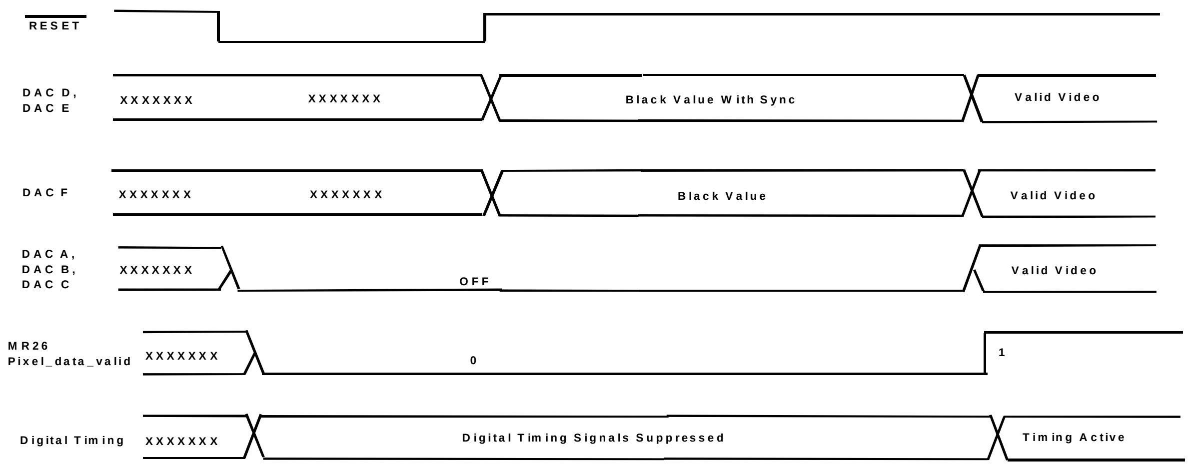
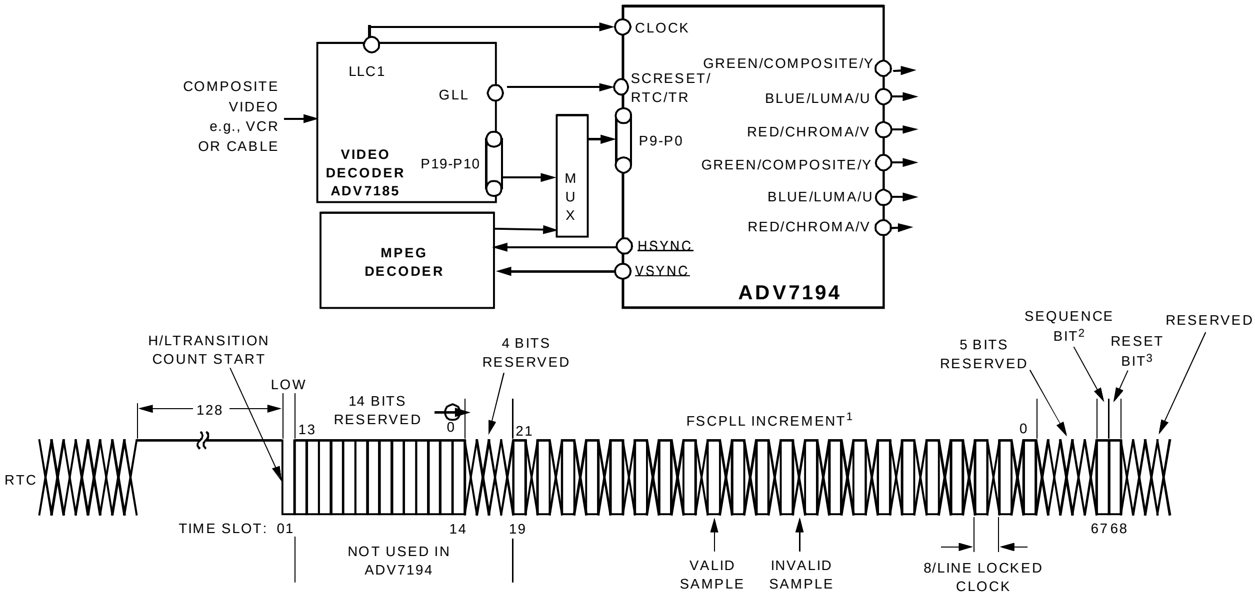


Figure 34. RESET Sequence Timing Diagram



NOTES:
[1]F_{SC} PLL INCREMENT IS 22 BITS LONG, VALUED LOADED INTO ADV7194 FSC DDS REGISTER IS F_{SC} PLL INCREMENTS BITS 21:0 PLUS BITS 0:9 OF SUB CARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUB CARRIER FREQUENCY REGISTERS OF THE ADV7194.

[2]SEQUENCE BIT
PAL: 0 = LINE NORMAL, 1 = LINE INVERTED
NTSC: 0 = NO CHANGE.

[3]RESET BIT
RESET ADV7194's DDS.

Figure 35. RTC Timing and Connections

Mode 0 (CCIR-656) :- Slave Option.
(Timing Register 0 TR0 = X X X X X 0 0 0)

The ADV7194 is controlled by the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the Pixel Data. All timing information is transmitted using a 4-byte Synchronisation Pattern. A Synchronisation pattern is sent immediately before and after each line during active picture and retrace. Mode 0 is illustrated in Figure 36. The $\overline{\text{HSYNC}}$,$\overline{\text{VSYNC}}$ and $\overline{\text{BLANK}}$ (if not used) pins should be tied high during this mode. Blank output is available.

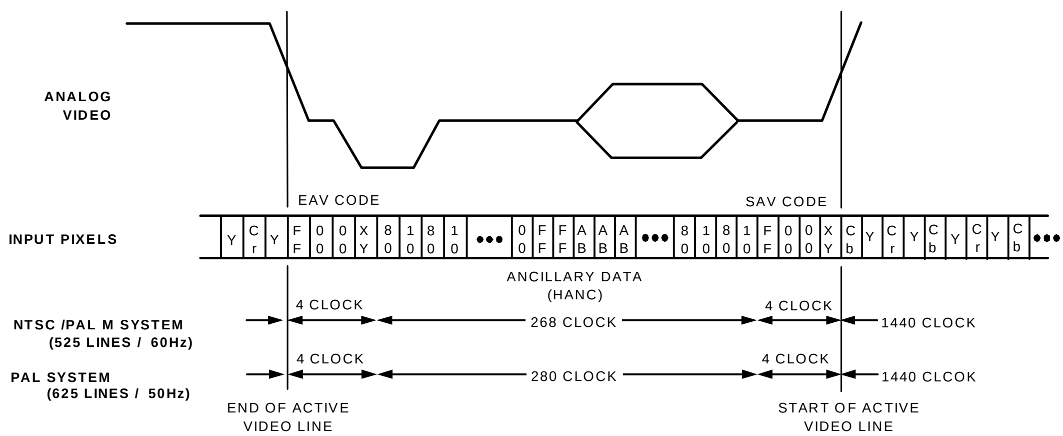


Figure 36. Timing Mode 0 (Slave Mode)

Mode 0 (CCIR-656) :- Master Option.
(Timing Register 0 TR0 = X X X X X 0 0 1)

The ADV7194 generates H, V and F signals required for the SAV (Start Active Video) and EAV (End Active Video) Time Codes in the CCIR656 standard. The H bit is output on the $\overline{HSYNC}$ pin, the V bit is output on the $\overline{BLANK}$ pin and the F bit is output on the $\overline{VSYNC}$ pin. Mode 0 is illustrated in Figure 37(NTSC) and Figure 38(PAL). The H, V and F transitions relative to the video waveform are illustrated in Figure 39.

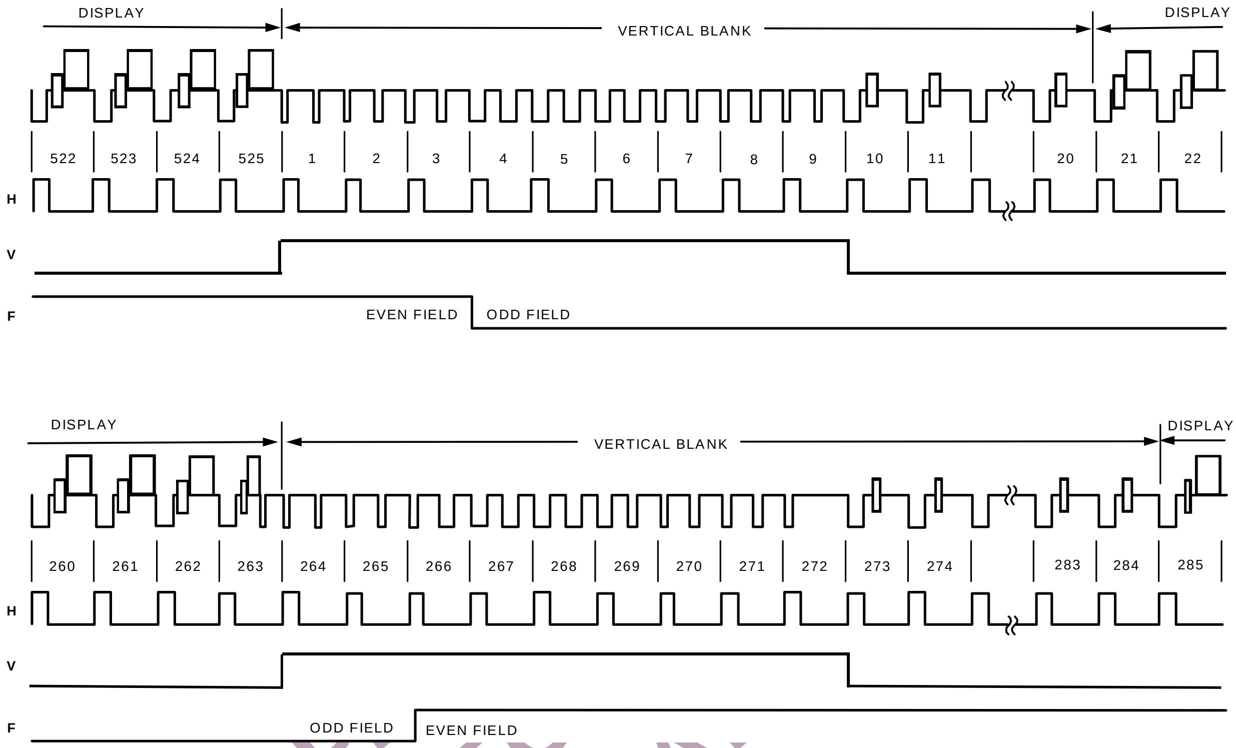


Figure 37. Timing Mode 0 (NTSC Master Mode)

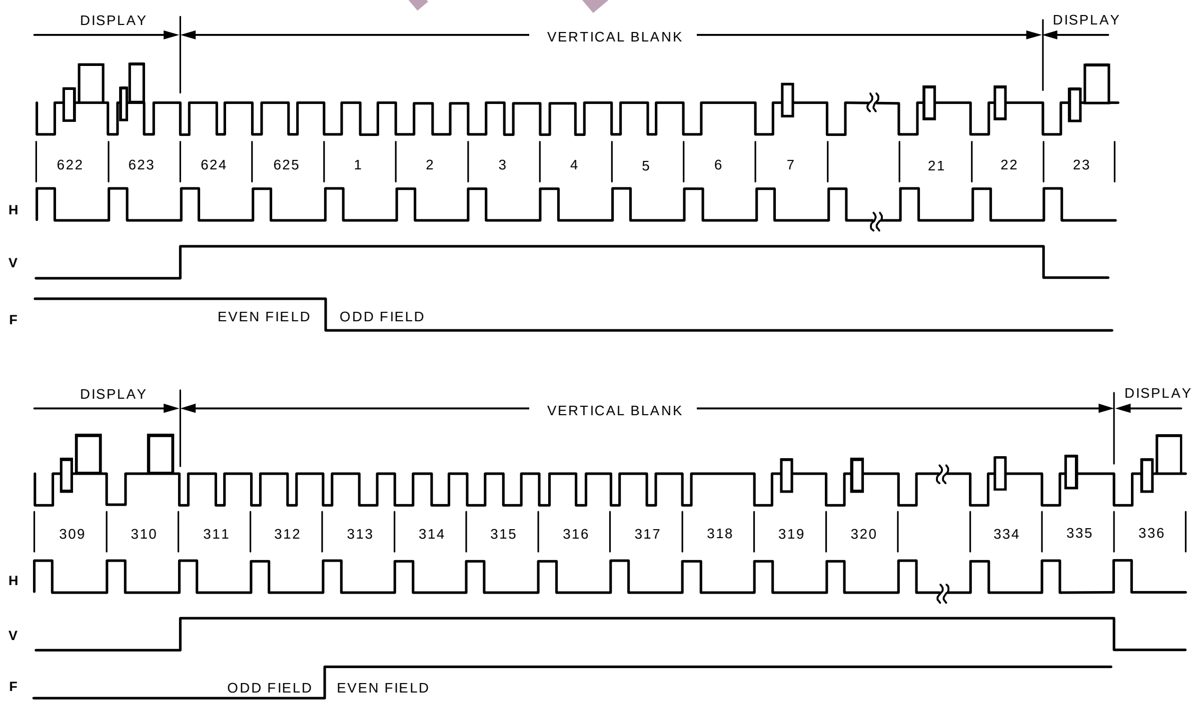


Figure 38. Timing Mode 0 (PAL Master Mode)

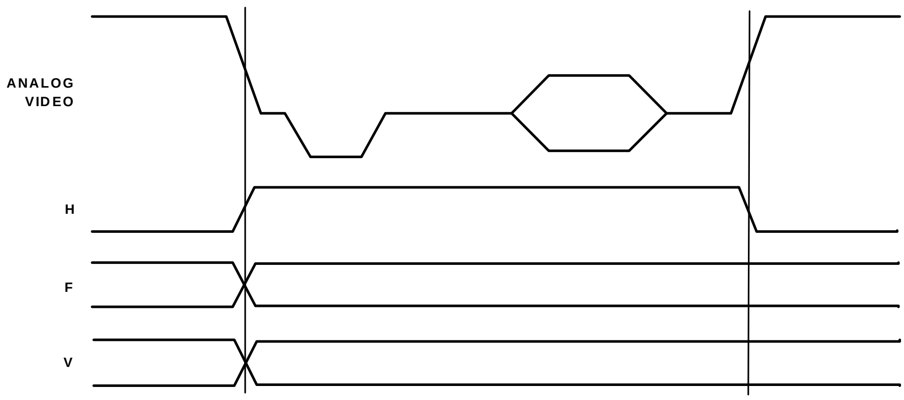


Figure 39. Timing Mode 0 Data Transitions (Master Mode)

Mode 1 :- Slave Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD
(Timing Register 0 TR0 = X X X X X 0 1 0)

In this mode the ADV7194 accepts Horizontal SYNC and Odd/ Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7194 automatically blanks all normally blank lines as per CCIR-624. Mode 1 is illustrated in Figure 40(NTSC) and Figure 41(PAL).

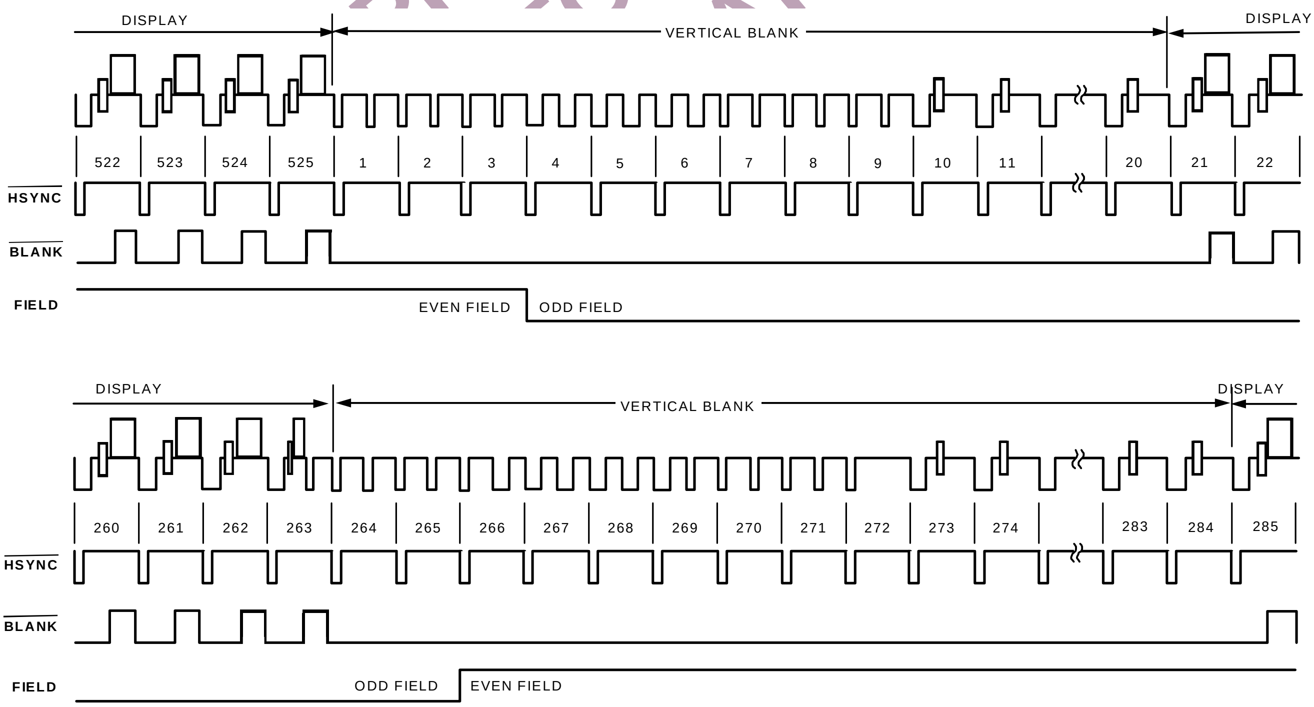


Figure 40. Timing Mode 1 (NTSC)

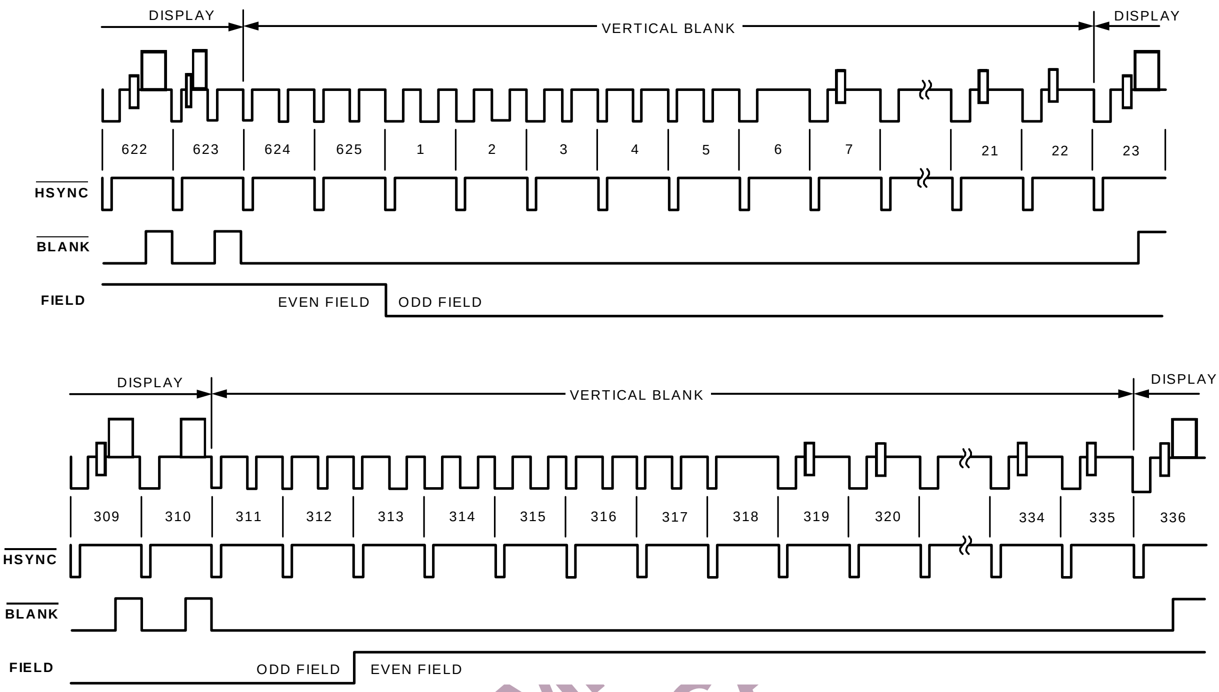


Figure 41 Timing Mode 1 (PAL)

Mode 1 :- Master Option. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 0 1 1)

In this mode the ADV7194 can generate Horizontal SYNC and Odd / Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is low indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7194 automatically blanks all normally blank lines as per CCIR-624 . Pixel data is latched on the rising clock edge following the timing signal transitions. Mode 1 is illustrated in Figure 43(NTSC) and Figure 44(PAL). Figure 42 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and FIELD for an odd or even field transition relative to the pixel data.

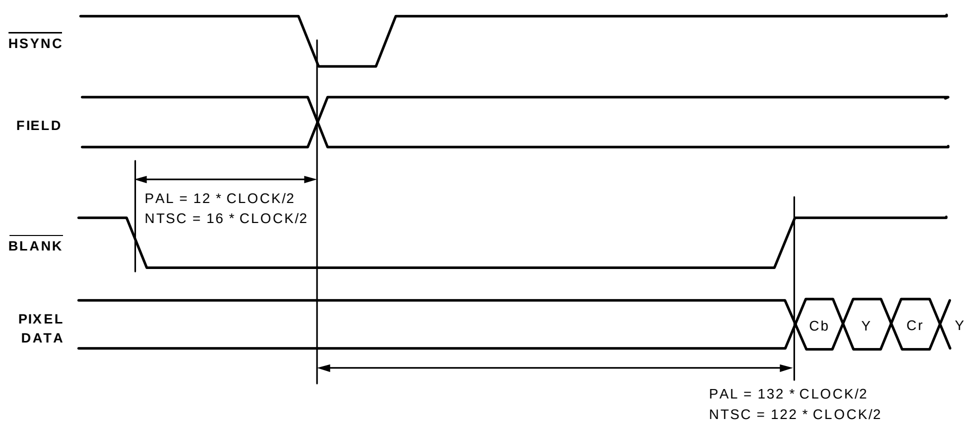


Figure 42. Timing Mode 1 Odd/Even Field Transitions Master/Slave

Mode 2 :- Slave Option HSYNC, VSYNC, BLANK.
(Timing Register 0 TR0 = X X X X X 1 0 0)

In this mode the ADV7194 accepts Horizontal and Vertical SYNC signals. A coincident low transition of both HSYNC and VSYNC inputs indicates the start of an Odd Field. A VSYNC low transition when HSYNC is high indicates the start of an Even Field. The BLANK signal is optional. When the BLANK input is disabled the ADV7192/93 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 46(NTSC) and Figure 47(PAL).

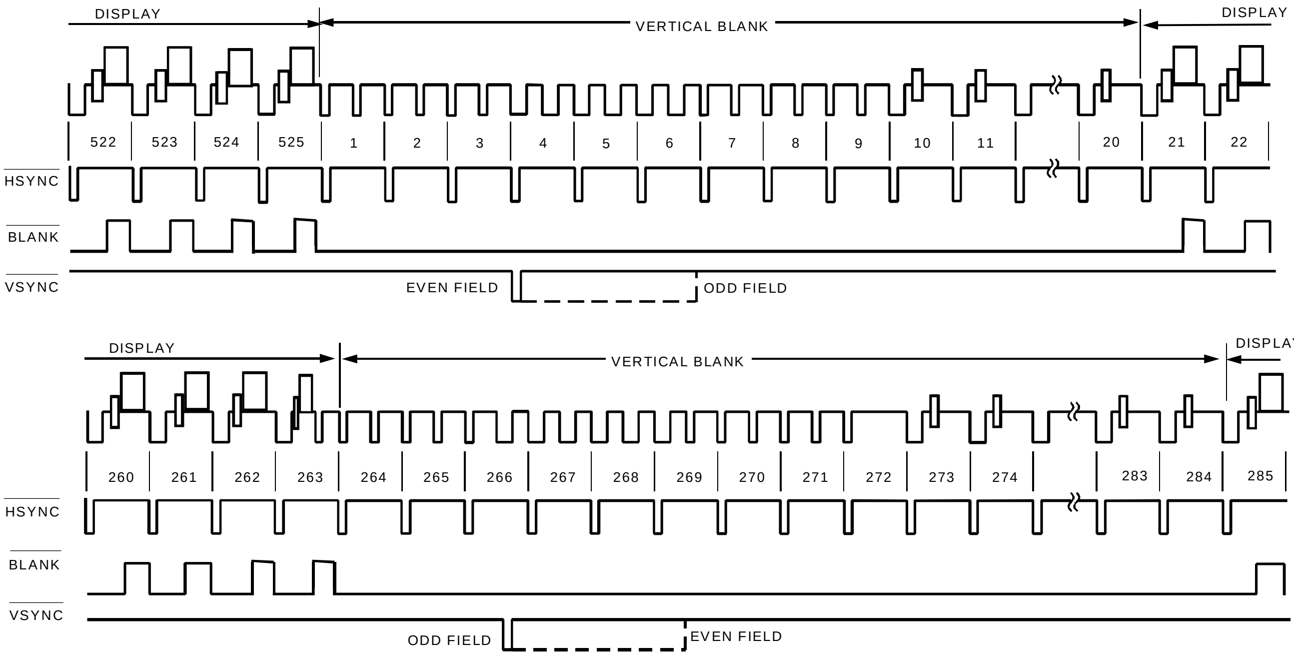


Figure 43 Timing Mode 2 (NTSC)

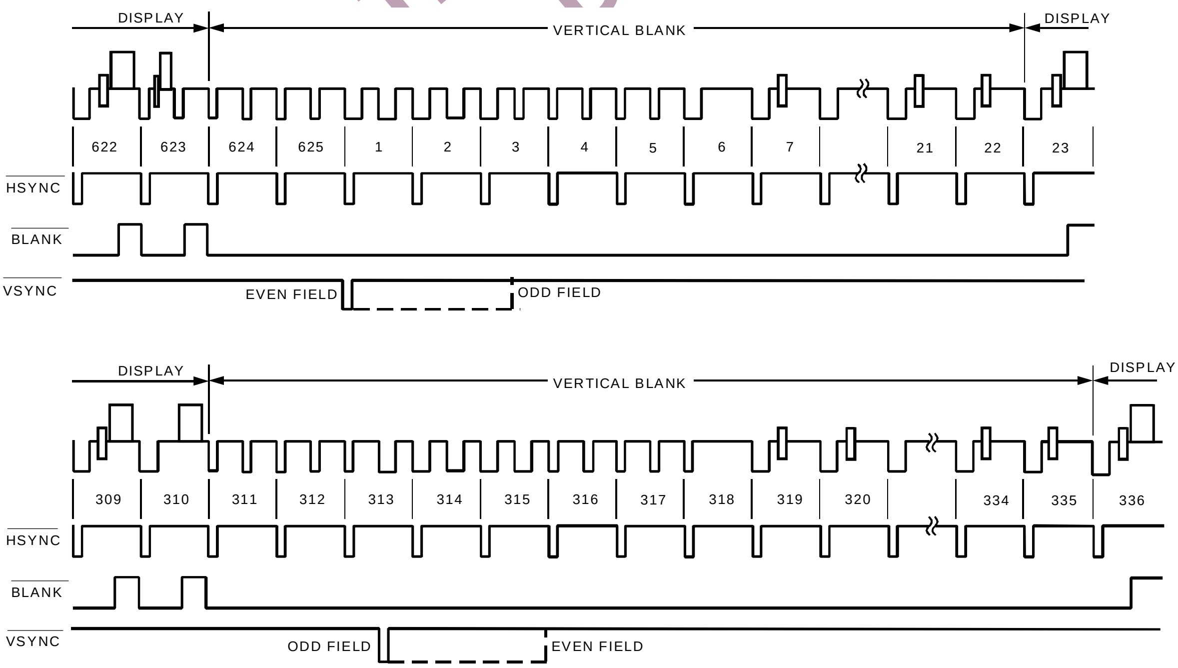


Figure 44. Timing Mode 2 (PAL)

Mode 2 :- Master Option $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{BLANK}}$.
(Timing Register 0 TR0 = X X X X X 1 0 1)

In this mode the ADV7194 can generate Horizontal and Vertical SYNC signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an Odd Field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an Even Field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7194 automatically blanks all normally blank lines as per CCIR-624. Mode 2 is illustrated in Figure 43 (NTSC) and Figure 44 (PAL). Figure 45 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and $\overline{\text{VSYNC}}$ for an even to odd field transition relative to the pixel data. Figure 46 illustrates the $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$ and $\overline{\text{VSYNC}}$ for an odd to even field transition relative to the pixel data.

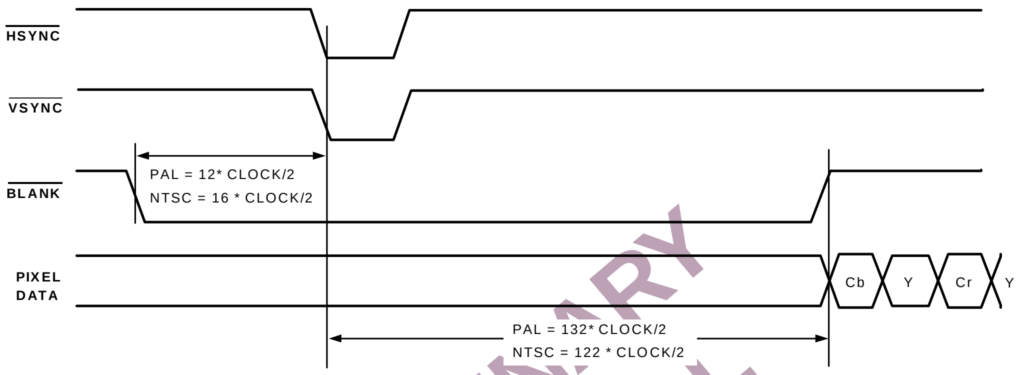


Figure 45. Timing Mode 2 Even to Odd Field Transistion Master/Slave

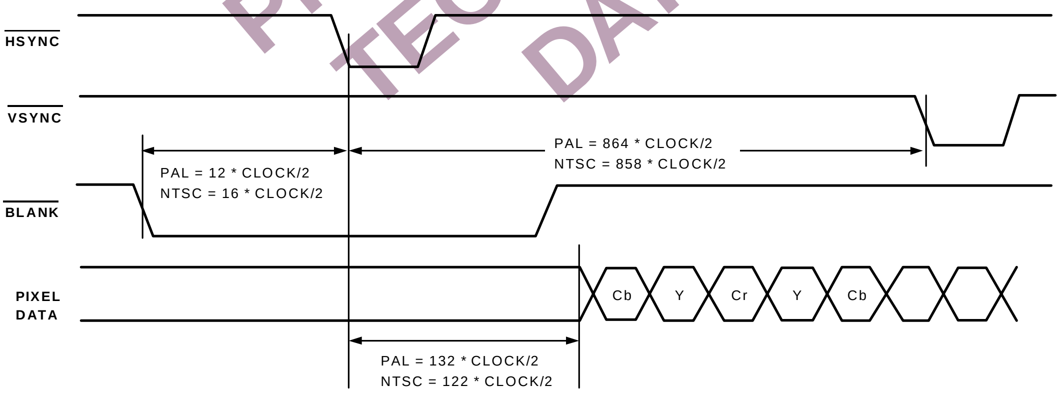


Figure 46. Timing Mode 2 Odd to Even Field Transistion Master/Slave

Mode 3 :- Master/Slave Option $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, FIELD.
(Timing Register 0 TR0 = X X X X X 1 1 0 or X X X X X 1 1 1)

In this mode the ADV7194 accepts or generates Horizontal SYNC and Odd / Even FIELD signals. A transition of the FIELD input when $\overline{\text{HSYNC}}$ is high indicates a new frame i.e. Vertical Retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled the ADV7194 automatically blanks all normally blank lines as per CCIR-624. Mode 3 is illustrated in Figure 47 (NTSC) and Figure 48 (PAL).

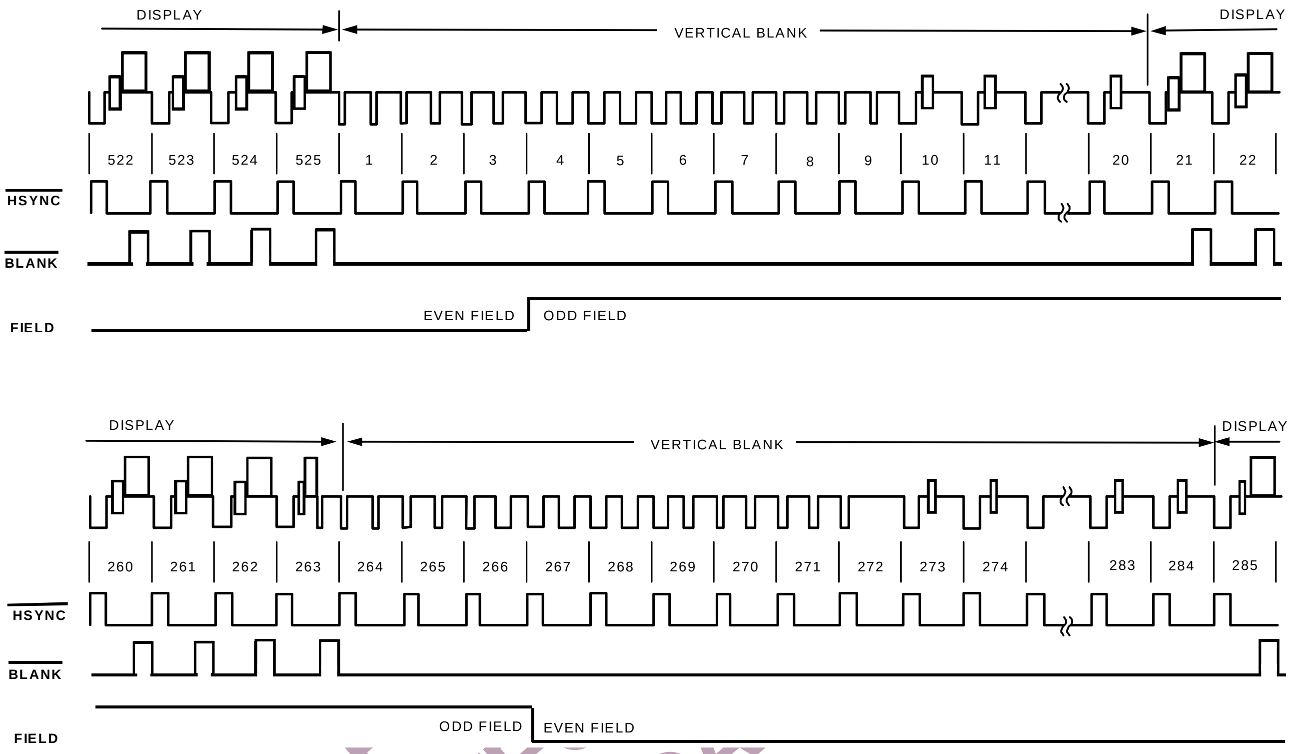


Figure 47. Timing Mode 3 (NTSC)

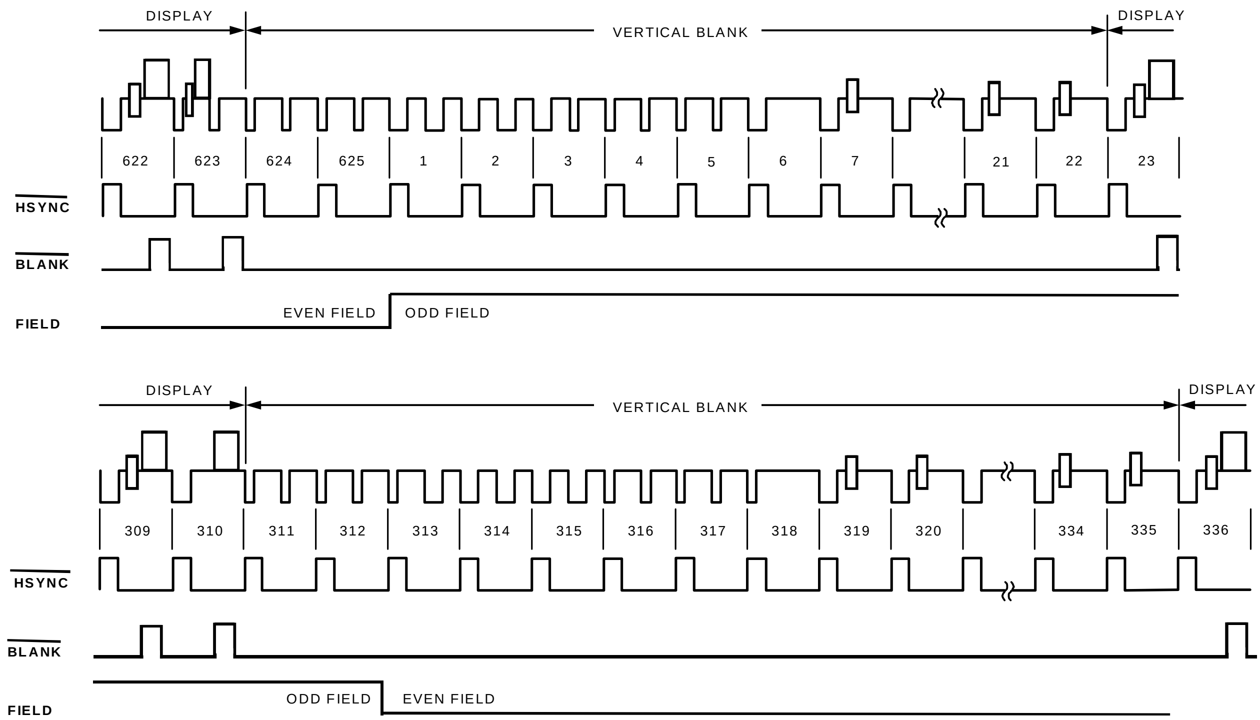


Figure 48. Timing Mode 3 (PAL)

MPU PORT DESCRIPTION.

The ADV7194 support a two wire serial (I^{2}C compatible) microprocessor bus driving multiple peripherals. Two inputs Serial Data (SDA) and Serial Clock (SCL) carry information between any device connected to the bus. Each slave device is recognized by a unique address. The ADV7194 has four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 49. The LSB sets either a read or write operation. Logic level "1" corresponds to a read operation while logic level "0" corresponds to a write operation. A1 is set by setting the ALSB pin of the ADV7194 to logic level "0" or logic level "1". When ALSB is set to "0", there is greater input bandwidth on the I2C lines, which allows high speed data transfers on this bus. When ALSB is set to "1", there is reduced input bandwidth on the I2C lines, which means that pulses of less than 50ns will not pass into the I2C internal controller. This mode is recommended for noisy systems.

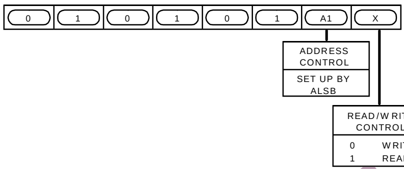


Fig 49. ADV7194 Slave Address

To control the various devices on the bus the following protocol must be followed. First the master initiates a data transfer by establishing a Start condition, defined by a high to low transistion on SDA whilst SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the Start condition and shift the next eight bits (7-Bit address + R/$\overline{W}$ bit). The bits are tranferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the Start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

A logic "0" on the LSB of the first byte means that the master will write information to the peripheral. A logic "1" on the LSB of the first byte means that the master will read information from the peripheral.

The ADV7194 acts as a standard slave device on the bus. The data on the SDA pin is 8 bits long supporting the 7-Bit addresses plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment allowing data to be written to or read from from the starting subaddress. A data transfer is always terminated by a Stop condition. The user can also access any unique subaddress register on a one by one basis without having to update all the registers. There is one exception. The Sub-Carrier Frequency Registers should be updated in sequence, starting with Sub-Carrier Frequency Register 0. The auto-increment function should be then used to increment and access Sub-Carrier Frequency Registers 1, 2 and 3. The Sub-Carrier Frequency Registers should not be accessed independently.

Stop and Start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, then these cause an immediate jump to the idle condition. During a given SCL high period the user should only issue one Start condition, one Stop condition or a single Stop condition followed by a single Start condition. If an invalid subaddress is issued by the user, the ADV7194 will not issue an acknowledge and will return to the idle condition. If in auto-increment mode, the user exceeds the highest subaddress then the following action will be taken:

1. In Read Mode, the highest subaddress register contents will continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no-acknowledge condition is where the SDA line is not pulled low on the ninth pulse.

2. In Write Mode, the data for the invalid byte will be not be loaded into any subaddress register, a no-acknowledge will be issued by the ADV7194 and the part will return to the idle condition.

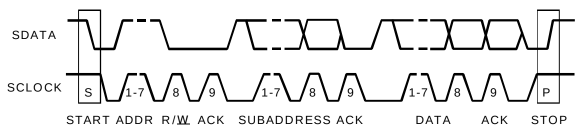


Figure 50. Bus Data Transfer

Figure 50 illustrates an example of data transfer for a read sequence and the Start and Stop conditions.

Figure 51 shows bus write and read sequences.

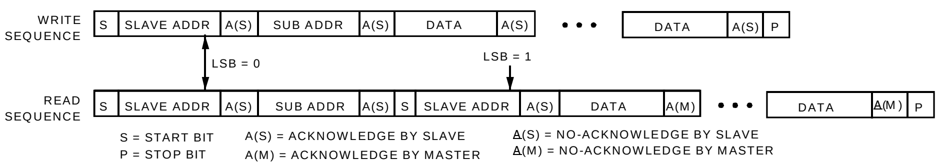


Figure 51 Write and Read Sequences

REGISTER ACCESSES

The MPU can write to or read from all of the registers of the ADV7194 except the Subaddress Registers which are write only registers. The Subaddress Register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the Subaddress Register. Then a read/write operation is performed from/to the target address which then increments to the next address until a Stop command on the bus is performed.

REGISTER PROGRAMMING

The following section describes each register. All registers can be read from as well as written to.

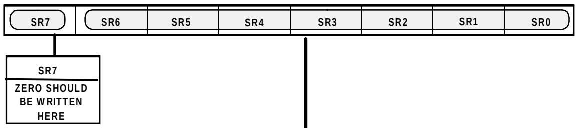
Subaddress Register (SR7-SR0)

The Communications Register is an eight bit write-only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The Subaddress Register determines to/from which register the operation takes place.

Figure 52 shows the various operations under the control of the Subaddress Register. "0" should always be written to SR7.

Register Select (SR6-SR0):

These bits are set up to point to the required starting address.



ADV7194 SUBADDRESS REGISTER

Address	SR6	SR5	SR4	SR3	SR2	SR1	SR0	
00h	0	0	0	0	0	0	0	MODE REGISTER 0
01h	0	0	0	0	0	0	1	MODE REGISTER 1
02h	0	0	0	0	0	1	0	MODE REGISTER 2
03h	0	0	0	0	0	1	1	MODE REGISTER 3
04h	0	0	0	0	1	0	0	MODE REGISTER 4
05h	0	0	0	0	1	0	1	MODE REGISTER 5
06h	0	0	0	0	1	1	0	MODE REGISTER 6
07h	0	0	0	0	1	1	1	MODE REGISTER 7
08h	0	0	0	1	0	0	0	MODE REGISTER 8
09h	0	0	0	1	0	0	1	MODE REGISTER 9
0Ah	0	0	0	1	0	1	0	TIMING REGISTER 0
0Bh	0	0	0	1	0	1	1	TIMING REGISTER 1
0Ch	0	0	0	1	1	0	0	SUB CARRIER FREQUENCY REGISTER 0
0Dh	0	0	0	1	1	0	1	SUB CARRIER FREQUENCY REGISTER 1
0Eh	0	0	0	1	1	1	0	SUB CARRIER FREQUENCY REGISTER 2
0Fh	0	0	0	1	1	1	1	SUB CARRIER FREQUENCY REGISTER 3
10h	0	0	1	0	0	0	0	SUB CARRIER PHASE REGISTER
11h	0	0	1	0	0	0	1	CLOSED CAPTIONING EXTENDED DATA BYTE 0
12h	0	0	1	0	0	1	0	CLOSED CAPTIONING EXTENDED DATA BYTE 1
13h	0	0	1	0	0	1	1	CLOSED CAPTIONING DATA BYTE 0
14h	0	0	1	0	1	0	0	CLOSED CAPTIONING DATA BYTE 1
15h	0	0	1	0	1	0	1	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 0
16h	0	0	1	0	1	1	0	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 1
17h	0	0	1	0	1	1	1	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 2
18h	0	0	1	1	0	0	0	NTSC PEDESTAL/TELETEXT CONTROL REGISTER 3
19h	0	0	1	1	0	0	1	CGMS/WSS 0
1Ah	0	0	1	1	0	1	0	CGMS/WSS 1
1Bh	0	0	1	1	0	1	1	CGMS/WSS 2
1Ch	0	0	1	1	1	0	0	TELETEXT CONTROL REGISTER
1Dh	0	0	1	1	1	0	1	CONTRAST CONTROL REGISTER
1Eh	0	0	1	1	1	1	0	U SCALE REGISTER
1Fh	0	0	1	1	1	1	1	V SCALE REGISTER
20h	0	1	0	0	0	0	0	HUE ADJUST REGISTER
21h	0	1	0	0	0	0	1	BRIGHTNESS CONTROL REGISTER
22h	0	1	0	0	0	1	0	SHARPNESS CONTROL REGISTER
23h	0	1	0	0	0	1	1	DNR REGISTER 0
24h	0	1	0	0	1	0	0	DNR REGISTER1
25h	0	1	0	0	1	0	1	DNR REGISTER 2
26h	0	1	0	0	1	1	0	GAMMA CORRECTION REGISTER 0
27h	0	1	0	0	1	1	1	GAMMA CORRECTION REGISTER 1
28h	0	1	0	1	0	0	0	GAMMA CORRECTION REGISTER 2
29h	0	1	0	1	0	0	1	GAMMA CORRECTION REGISTER 3
2Ah	0	1	0	1	0	1	0	GAMMA CORRECTION REGISTER 4
2Bh	0	1	0	1	0	1	1	GAMMA CORRECTION REGISTER 5
2Ch	0	1	0	1	1	0	0	GAMMA CORRECTION REGISTER 6
2Dh	0	1	0	1	1	0	1	GAMMA CORRECTION REGISTER 7
2Eh	0	1	0	1	1	1	0	GAMMA CORRECTION REGISTER 8
2Fh	0	1	0	1	1	1	1	GAMMA CORRECTION REGISTER 9
30h	0	1	1	0	0	0	0	GAMMA CORRECTION REGISTER 10
31h	0	1	1	0	0	0	1	GAMMA CORRECTION REGISTER 11
32h	0	1	1	0	0	1	0	GAMMA CORRECTION REGISTER 12
33h	0	1	1	0	0	1	1	GAMMA CORRECTION REGISTER 13
34h	0	1	1	0	1	0	0	BRIGHTNESS DETECT REGISTER
35h	0	1	1	0	1	0	1	OUTPUT CLOCK REGISTER
36h	0	1	1	0	1	1	0	RESERVED
37h	0	1	1	0	1	1	1	RESERVED
38h	0	1	1	1	0	0	0	RESERVED
39h	0	1	1	1	0	0	1	RESERVED
3Ah	0	1	1	1	0	1	0	RESERVED
3Bh	0	1	1	1	0	1	1	RESERVED
3Ch	0	1	1	1	1	0	0	RESERVED
3Dh	0	1	1	1	1	0	1	RESERVED
3Eh	0	1	1	1	1	1	0	RESERVED
3Fh	1	1	1	1	1	1	1	RESERVED
40h	1	0	0	0	0	0	0	RESERVED
41h	1	0	0	0	0	0	1	RESERVED
42h	1	0	0	0	0	1	0	RESERVED
43h	1	0	0	0	0	1	1	RESERVED
44h	1	0	0	0	1	0	0	RESERVED
45h	1	0	0	0	1	0	1	RESERVED
46h	1	0	0	0	1	1	0	RESERVED
47h	1	0	0	1	1	1	1	RESERVED
48h	1	0	0	1	0	1	0	RESERVED
49h	1	0	0	1	0	0	1	RESERVED
4Ah	1	0	0	1	0	0	0	RESERVED
4Bh	1	0	0	1	0	1	1	RESERVED

Figure 52 . Subaddress Register for the ADV7194

MODE REGISTER 0
MR0 (MR07-MR00)
(Address (SR4-SR0) = 00H)

Figure 53 shows the various operations under the control of Mode Register 0.

MR0 BIT DESCRIPTION

Output Video Standard Selection (MR00-MR01):
These bits are used to setup the encoder mode. The ADV7194 can be set up to output NTSC, PAL (B,D,G,H,I) or PAL N standard video.

Luma Filter Select (MR02-MR04):
These bits specify which luma filter is to be selected. The filter selection is made independent of whether PAL or NTSC is selected.

Chroma Filter Select (MR05-MR07):
These bits select the chrominance filter. A low pass filter can be selected with a choice of cut-off frequencies (0.65MHz, 1.0MHz, 1.3MHz , 2MHz or 3Mhz) along with a choice of CIF or QCIF filters.

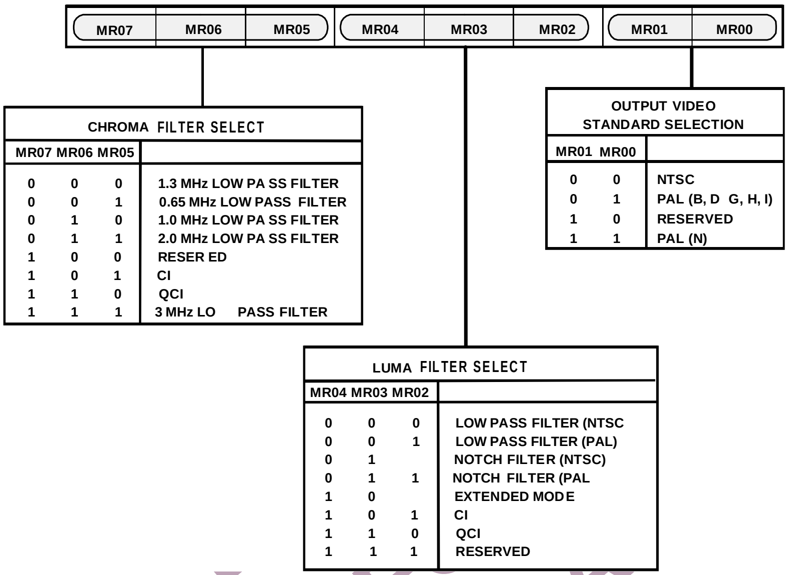


Figure 53. Mode Register 0 (MR0)

MODE REGISTER 1
MR1 (MR17-MR10)
(Address (SR4-SR0) = 01H)

Figure 54 shows the various operations under the control of Mode Register 1.

MR1 BIT DESCRIPTION

DAC Control (MR10-MR15):
Bits MR15-MR10 can be used to power down the DACs. This is in order to reduce the power consumption of the ADV7194 or if any of the DACs are not required in the application.

4XOversampling Control (MR16):
To enable 4xOversampling this bit has to be set to '1'. When enabled, the data is output at a frequency of 54 MHz. Note that 'PLL Enable' Control has to be enabled (MR61 = "0") in 4xOversampling mode. An external Vref can not be used in 4xOversampling Mode.

Reserved (MR17)
A logical " 0" must be written to this bit.

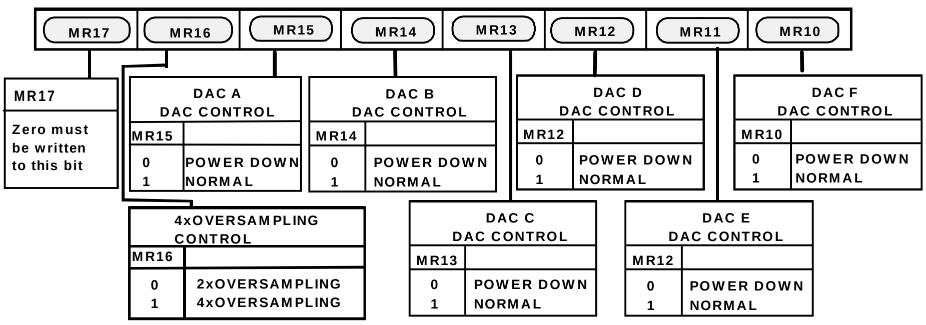


Figure 54. Mode Register 1 (MR1)

MODE REGISTER 2

MR2 (MR27-MR20)

(Address (SR4-SR0) = 02H)

Mode Register 2 is a 8-Bit wide register.

Figure 55 shows the various operations under the control of Mode Register 2.

MR2 BIT DESCRIPTION-

RGB/YUV Control (MR20):

This bit enables the output from the DACs to be set to YUV or RGB output video standard.

DAC Output Control (MR21):

This bit controls the output from DACs A,B, and C. When this bit is set to "1" Composite, Luma and Chroma Signals are output from DACs A, B and C (respectively).When this bit is set to "0", RGB or YUV may be output from these DACs.

SCART Enable Control (MR22):

This bit is used to switch the DAC outputs from SCART to a EUROSCART configuration. A complete table of all DAC output configurations is shown below.

Table II. DAC Output configuration

MR22 SCART	MR21 DAC O/P	MR20 RGB/ YUV	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
0	0	0	G (Y)	B (Pb)	R (Pr)	CVBS	LUMA	CHROMA
0	0	1	Y (Y)	U (Pb)	V (Pr)	CVBS	LUMA	CHROMA
0	1	0	CVBS	LUMA	CHROMA	G (Y)	B (Pb)	R (Pr)
0	1	1	CVBS	LUMA	CHROMA	Y (Y)	U (Pb)	V (Pr)
1	0	0	CVBS	B (Pb)	R (Pr)	G (Y)	LUMA	CHROMA
1	0	1	CVBS	U (Pb)	V (Pr)	Y (Y)	LUMA	CHROMA
1	1	0	CVBS	LUMA	CHROMA	G (Y)	B (Pb)	R (Pr)
1	1	1	CVBS	LUMA	CHROMA	Y (Y)	U (Pb)	V (Pr)

Note: In Progressive Scan Mode (MR80, '1') the DAC output configuration is stated in the brackets.

Pedestal Control (MR23):

This bit specifies whether a pedestal is to be generated on the NTSC composite video signal. This bit is invalid when the device is configured in PAL mode.

Square Pixel Control (MR24):

This bit is used to setup square pixel mode. This is available in Slave Mode only. For NTSC, a 24.5454MHz clock must be supplied. For PAL, a 29.5MHz clock must be supplied. Square pixel operation is not available in 4xOversampling mode.

Standard I²C Control (MR25):

This bit controls the video standard used by the ADV7194. When this bit is set to "1" the video standard is as programmed in Mode Register 0 ('Output Video Standard Selection'). When it is set to "0", the ADV7194 is forced into the standard selected by the NTSC_PAL pin. When NTSC_PAL is low the standard is NTSC, when the NTSC_PAL pin is high, the standard is PAL.

Pixel DataValid Control (MR26):

After resetting the device this bit has the value "0" and the pixel data input to the encoder is blanked such that a black screen is output from the DACs. The ADV7194 will be set to Master Mode timing. When this bit is set to "1" by the user (via the I2C), pixel data passes to the pins and the encoder reverts to the timing mode defined by Timing Register 0.

Sleep Mode Control (MR27):

When this bit is set ("1"), Sleep Mode is enabled. With this mode enabled the ADV7194 current consumption is reduced to typically 0.1 μA. The I²C registers can be written to and read from when the ADV7194 is in Sleep Mode.

When the device is in Sleep Mode and "0" is written to MR27, the ADV7194 will come out of Sleep Mode and resume normal operation. Also, if a $\overline{\text{RESET}}$ is applied during Sleep Mode the ADV7194 will come out of Sleep Mode and resume normal operation.

For this to operate, 'Power up in Sleep Mode' control has to be enabled (MR60 = "1"), otherwise Sleep Mode is controlled by the PAL_NTSC and SCRESET/RTC/TR pins.

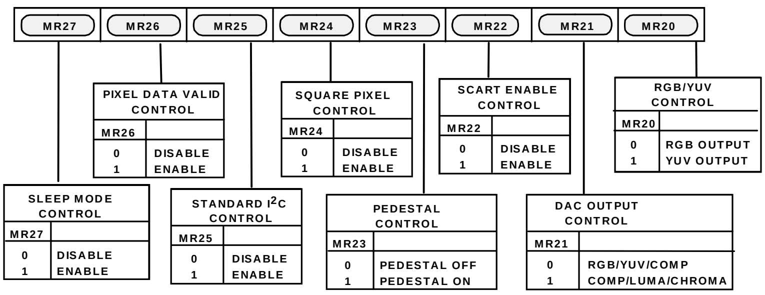


Figure 55. Mode Register 2 (MR2)

MODE REGISTER 3
MR3 (MR37-MR30)
(Address (SR4-SR0) = 03H)
Mode Register 3 is a 8-Bit wide register. Figure 56 shows the various operations under the control of Mode Register 3.

MR3 BIT DESCRIPTION
Revision Code (MR30 - MR31):
This bit is read only and indicates the revision of the device.

VBI Open (MR32):
This bit determines whether or not data in the Vertical Blanking Interval (VBI) is output to the analog outputs or blanked. Note that this condition is also valid in Timing Slave Mode 0. For further information see page 29.

Teletext Enable (MR33):
This bit must be set to "1" to enable teletext data insertion on the TTX pin. Note: TTX functionality is shared with VSO and CLAMP on pin 62. CLAMP/$\overline{\text{VSO}}$ Select (MR77) and TTX Input/CLAMP$\overline{\text{VSO}}$ Output Control (MR76) have to be set accordingly.

Teletext Bit Request Mode Control (MR34):
This bit enables switching of the teletext request signal from a continuous high signal (MR34 = "0") to a bitwise request signal (MR34 = "1").

Closed Captioning Field Selection (MR35-MR36)
These bits control the fields that closed captioning data is displayed on, closed captioning information can be displayed on an odd field, even field or both fields.

Reserved (MR37):
A logic '0' must be written to this bit.

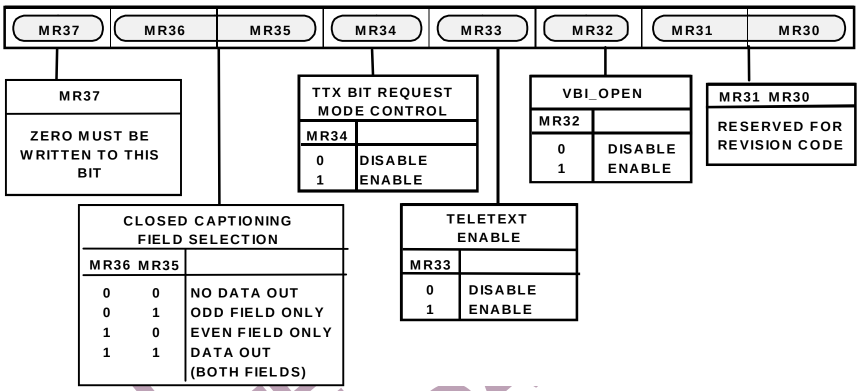


Figure 56. Mode Register 3 (MR3)

MODE REGISTER 4
MR4 (MR47-MR40)
(Address (SR4-SR0) = 04H)
Mode Register 4 is a 8-Bit wide register. Figure 57 shows the various operations under the control of Mode Register 4.

MR4 BIT DESCRIPTION
VSYNC_3H Control (MR40):
When this bit is enabled ("1") in Slave Mode , it is possible to drive the $\overline{\text{VSYNC}}$ input low for 2.5 lines in PAL mode and 3 lines in NTSC mode. When this bit is enabled in Master Mode the ADV7194 outputs an active low $\overline{\text{VSYNC}}$ signal for 3 lines in NTSC mode and 2.5 lines in PAL mode.

Genlock Selection (MR41-MR42)
These bits control the genlock feature and timing reset of the ADV7194. Setting MR41 and MR42 to logic "0" disables the SCRESET/RTC/TR pin and allows the ADV7194 to operate in normal mode.
(a) By setting MR41 to "0" and MR42 to "1" a timing reset is applied, resetting the horizontal and vertical counters. This has the effect of resetting the Field Count to Field 0. If the SCRESET/RTC/TR pin is held high, the counters will remain reset. Once the pin is released the counters will commence counting again. For correct counter reset, the SCRESET/RTC/TR pin has to remain high for at least 37ns (1clock cycle at 27MHz).
(b) If MR41 is set to "1" and MR42 is set to "0", the SCRESET/RTC/TR pin is configured as a subcarrier reset input and the subcarrier phase will reset to Field 0 whenever a low to high transition is detected on the SCRESET/RTC/TR pin (SCH phase resets at the start of the next Field).
(c) If MR41 is set to "1" and MR42 is set to "1", the SCRESET/RTC/TR pin is configured as a real time control input and the ADV7194 can be used to lock to an external video source working in RTC mode. See also page 28.

Active Video Line Duration (MR43)
This bit switches between two active video line durations. A "0" selects CCIR Rec.601 (720 pixels PAL/NTSC) and a "1" selects ITU-R BT.470 standard for active video duration (710 pixels NTSC, 702 pixels PAL).

Chrominance Control (MR44)
This bit enables the color information to be switched on and off the chroma, composite and color component outputs.

Burst Control (MR45)
This bit enables the color burst to be switched on and off the chroma and composite signals.

Color Bar Control (MR46):
This bit can be used to generate and output an internal color bar test pattern. The color bar configuration is 100/7.5/75/7.5 for NTSC and 100/0/75/0 for PAL. It is important to note that when color bars are enabled the ADV7194 is configured in a Master Timing mode. The output pins VSYNC, HSYNC and BLANK are tri-state during color bar mode.

Interlaced Mode Control (MR47):
This bit is used to setup the output to interlaced or non-interlaced mode.

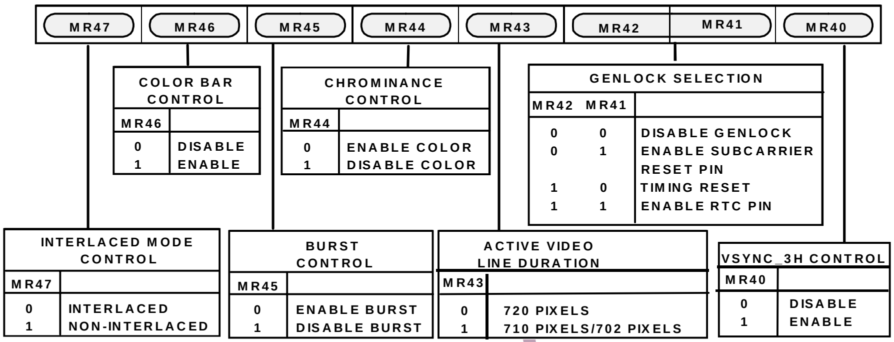


Figure 57. Mode Register 4 (MR4)

MODE REGISTER 5

MR5 (MR57-MR50)
(Address (SR4-SR0) = 05H)

Mode Register 5 is a 8-Bit wide register. Figure 58 shows the various operations under the control of Mode Register 5.

MR5 BIT DESCRIPTION

Y-Level Control (MR50):
This bit controls the component Y output level on the ADV7194. If this bit is set ("0"), the encoder outputs Betacam levels when configured in PAL or NTSC mode. If this bit is set ("1"), the encoder outputs SMPTE levels when configured in PAL or NTSC mode.

UV-Level Control (MR51-MR52):
These bits control the color component U and V output levels on the ADV7194. It is possible to have UV levels with a peak-peak amplitude of either 700mV (MR52+MR51 = "01") or 1000mV (MR52 + MR51 = "10") in NTSC and PAL. It is also possible to have default values of 934mV for NTSC and 700mV for PAL (MR52+ MR51 = "00").

RGB Sync (MR53):
This bit is used to set up the RGB outputs with the sync information encoded on all RGB outputs.

Clamp Delay (MR54-MR55):
These bits control the delay or advance of the CLAMP signal in the front or back porch of the ADV7194. It is possible to delay or advance the pulse by 0, 1, 2 or 3 clock cycles.

Note: TTX functionality is shared with VSO and CLAMP on pin 62. CLAMP/VSO Output Control (MR77) and TTX Input/CLAMPVSO Output Control (MR76) have to be set accordingly.

Clamp Delay Direction (MR56):
This bit controls a positive or negative delay in the CLAMP signal. If this bit is set ("1"), the delay is negative . If it is set ("0"), the delay is positive.

Clamp Position (MR57):
This bit controls the position of the CLAMP signal. If this bit is set ("1"), the CLAMP signal is located in the back porch position. If this bit is set ("0"), the CLAMP signal is located in the front porch position.

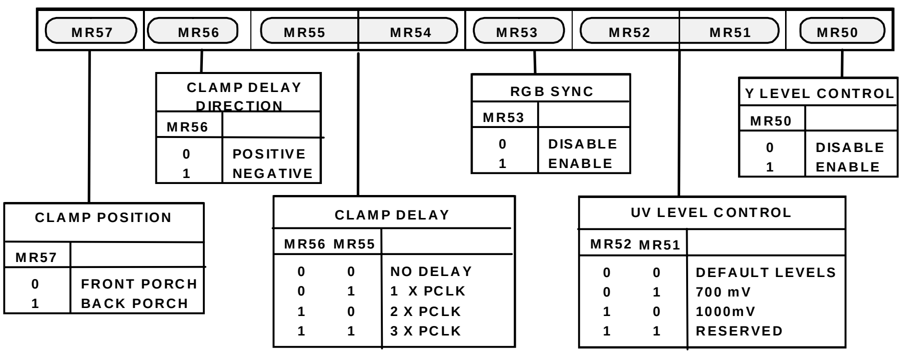


Figure 58. Mode Register 5 (MR5)

MODE REGISTER 6
MR6 (MR67-MR60)
(Address (SR4-SR0) = 06H)

Mode Register 6 is a 8-Bit wide register. Figure 59 shows the various operations under the control of Mode Register 6.

MR6 BIT DESCRIPTION

Power Up Sleep Mode Control (MR60):
After RESET is applied this control is enabled (MR60=0) if both
SCRESET/RTC/TR and NTSC_PAL pins are tied high. The ADV7194 will then power up in Sleep Mode to faciliate low power consumption before the I2C is initialised.
When this control is disabled (MR60=1, via the I2C) Sleep Mode control passes to 'Sleep Mode Control', MR27.

PPL Enable Control (MR61):
The PLL control should be enabled (MR61 = '0') when '4xOversampling' is enabled (MR16 = '1').

Reserved (MR62, MR63, MR64)
A logical "0" must be written to these bits.

Field Counter (MR65, MR66, MR67):
These three bits are read only bits. The Field count can be read back over the I2C interface. In NTSC mode the Field count goes from 0 - 3, in PAL mode from 0 - 7.

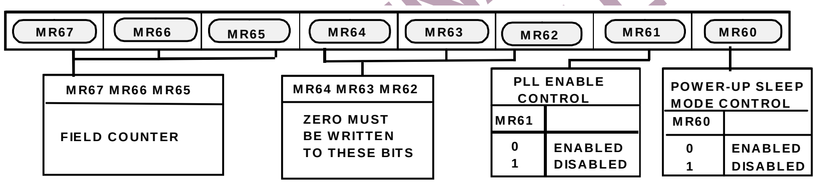


Figure 59. Mode Register 6 (MR6)

MODE REGISTER 7
MR7 (MR77-MR70)
(Address (SR4-SR0) = 07H)

Mode Register 7 is a 8-Bit wide register. Figure 60 shows the various operations under the control of Mode Register 7.

MR7 BIT DESCRIPTION

Color Control Enable (MR70):
This bit is used to enable control of contrast and saturation of color (Y-Scale, U-Scale, V-Scale). If this bit is set ("1") color controls are enabled. If this bit is set ("0"), the color control features are disabled.

Luma Saturation Control (MR71):
When this bit is set ("1"), the luma signal will be clipped if it reaches a limit that corresponds to an input luma value of 255 (after scaling by the Contrast Control Register). This prevents the chrominance component of the composite video signal being clipped if the amplitude of the luma is too high. When this bit is set ("0"), this control is disabled.

Hue Adjust Control (MR72):
This bit is used to enable hue adjustment on the composite and chroma output signals of the ADV7194. When this bit is set ("1"), the hue of the color is adjusted by the phase offset described in the Hue Adjust Control Register. When this bit is set ("0"), hue adjustment is disabled.

Brightness Enable Control (MR73):
This bit is used to enable brightness control on the ADV7194. The actual brightness level is programmed in the Brightness Control Register. This value or 'set up' level is added to the scaled Y data. When this bit is set ("1"), brightness control is enabled. When this bit is set ("0"), brightness control is disabled.

Sharpness Filter Enable (MR74):
This bit is used to enable the sharpness control of the luminance signal on the ADV7194 ('Luma Filter Select' has to be set to 'Extended', MR04-MR02 = "100"). The various responses of the filter are determined by the Sharpness Control Register. When this bit is set ("1") the luma response is altered by the amount described in the Sharpness Control Register. When this bit is set ("0"), the sharpness control is disabled. See figues 13, 14, 15 for luma signal responses.

CSO_HSO **Output Control (MR75):**
This bit is used to determine whether HSO or CSO TTL output signal is output at the CSO_HSO pin. If this bit is set ("1"), then the CSO TTL signal is output. If this bit is set ("0"), then the HSO TTL signal is output.

TTX Input/ CLAMP-VSO Output Control (MR76):
This bit controls whether pin 62 is configured as an output or as an input pin. A '1' selects pin 62 to be an output for CLAMP or VSO functionality. A '0' selects this pin as a TTX input pin.

CLAMP/VSO Output Control (MR77):
This bit is used to select the functionality of pin 62. Setting this bit to "1" selects CLAMP as the output signal. A "0" selects VSO as the output signal. Since this pin is also shared with the TTX functionality, 'TTX Input/ CLAMP-VSO Output' Control has to be set

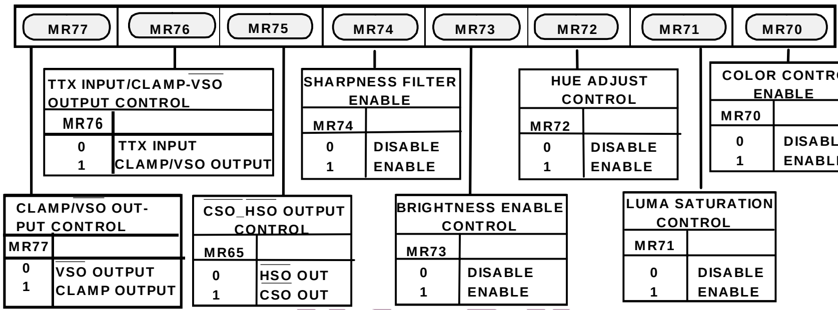


Figure 60. Mode Register 7 (MR7)

MODE REGISTER 8
MR8 (MR87-MR80)
(Address (SR4-SR0) = 08H)

Mode Register 8 is a 8-Bit wide register. Figure 61 shows the various operations under the control of Mode Register 8.

MR8 BIT DESCRIPTION

Progressive Scan Control (MR80):
This control enables the progressive scan inputs, Y0-9, Cb0-Cb9 and Cr0-Cr9. To enable this control MR80 has to be set to '1'. It is assumed that the incoming *Y* data contains all necessary sync information.
Note: Simultaneous progressive scan input and 20 or16-bit pixel input is not possible.

Reserved (MR 81):
A '0' must be written to this bit.

Double Buffer Control (MR82):
Double Buffering can be enabled or disabled on the Contrast Control Register, U Scale Register, V Scale Register, Hue Adjust Control Register, Closed Captioning Register, Brightness Control Register, Gamma Curve Select Bit. Double Buffering is not available in Master Mode.

20/16-Bit Pixel Port Control (MR83):
This bit controls whether the ADV7194 is operated in 16-bit mode ('10-Bit Pixel Port disabled, MR84='0', MR83='1') or 20-bit mode ('10-Bit Pixel Port enabled, MR84='1', MR83='1'). Unused input pins should be grounded.

10-Bit Pixel Port Control (MR84):
This bit selects 8-bit or 10-bit input format. In 8-bit mode the LSB of the pixel data is input on pin number 3, in 10-bit mode on pin number 1. Unused input pins should be grounded.

DNR Enable Control (MR85):
To enable the DNR process this bit has to be set to '1'. If this bit is set to '0' the DNR processing is bypassed. For further information on DNR controls see pages 55-57.

Gamma Enable Control (MR86):
To enable the programmable gamma correction this bit has to be set to enabled (MR86 = '1'). For further information on Gamma Correction controls see page58.

Gamma Curve Select Control (MR87):
This bit selects which of the two programmable gamma curves is to be used. When setting MR87 to '0' the gamma correction curve selected is curve A. Otherwise curve B is selected. Each curve will have to be programmed by the user. For further information on Gamma Correction controls see page 58.

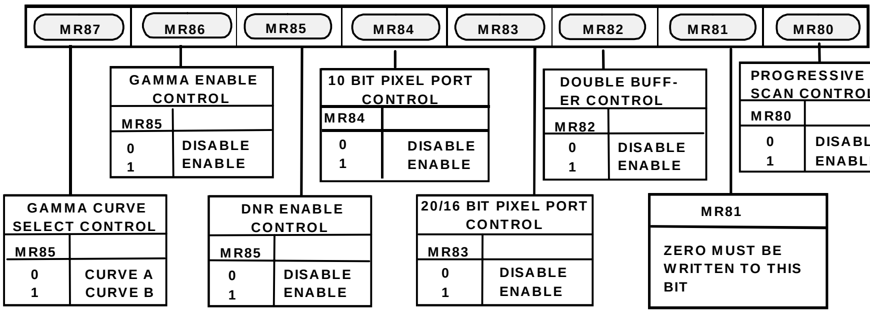


Figure 61. Mode Register 8 (MR8)

MODE REGISTER 9
MR9 (MR97-MR90)
(Address (SR4-SR0) = 09H)

Mode Register 9 is a 8-Bit wide register. Figure 63 shows the various operations under the control of Mode Register 9.

MR9 BIT DESCRIPTION

Undershoot Limiter (MR90 -MR91):
This control ensures that no luma video data will go below a programmable level. This prevents any synchronisation problems due to the luma signals going below the blanking level. Available limit levels are - 1.5 IRE, -6 IRE, -11 IRE.
Note that this facility is only available in 4xOversampling mode (MR16 = '1'). When the device is operated in 2xOversampling mode (MR16 = '0') or RGB outputs without RGB sync are selected in 4xOversampling, the minimum luma level is set in Timing Register 0, TR06 ('Min Luma' Control).

Black Burst Y-DAC (MR92):
It is possible to output a Black Burst signal from the DAC
which is selected to be the Luma DAC (MR22, MR21, MR20). This signal can be useful for locking two video sources together using professional video equipment. See also page 26.

Black Burst Luma-DAC (MR93):

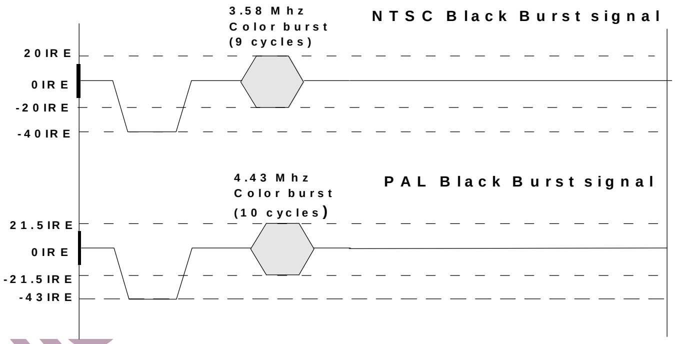


Figure 62 Black Burst signals for PAL and NTSC standards

It is possible to output a Black Burst signal from the DAC which is selected to be the Y-DAC (MR22, MR21, MR20). This signal can be useful for locking two video sources together using professional video equipment. See also page 26.

Chroma Delay Control (MR94-MR95):
The Chroma signal can be delayed by up to 8clock cycles at 27MHz using MR95-97. For further information see also page 26.

Reserved (MR96 - MR97):
A '0' must be written to these bits.

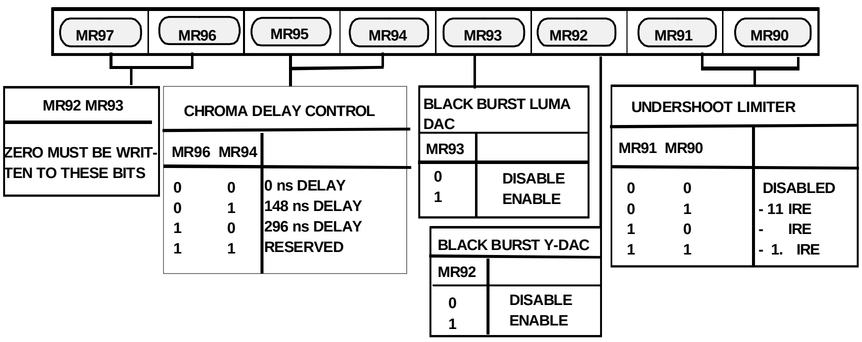


Figure 63. Mode Register 9 (MR9)

TIMING REGISTER 0 (TR07-TR00)
(Address (SR4-SR0) = 0AH)

Figure 64 shows the various operations under the control of Timing Register 0. This register can be read from as well as written to.

- TR0 BIT DESCRIPTION -

Master/Slave Control (TR00):
This bit controls whether the ADV7194 is in master or slave mode.

Timing Mode Selection (TR01-TR02):
These bits control the timing mode of the ADV7194. These modes are described in more detail on pages 31-37.

$\overline{\text{BLANK}}$ Input Control (TR03):
This bit controls whether the $\overline{\text{BLANK}}$ input is used to accept blank signals or whether blank signals are internally generated.
Note: When this input pin is is tied high (to +5V), the input is disabled regardless of the register setting. It therefore should be tied low (to Ground) to allow control over the I2C register.

Luma Delay (TR04-TR05):
The Luma signal can be delayed by up to 222ns (or 6 clock cycles at 27MHz) using TR04-05. For further information see page 26.

Min Luma Control (TR06):
This bit is used to control the minimum luma output value by the ADV7194. When this bit is set to a logic ("1"), the luma is limited to 7IRE below the blank level. When this bit is set to ("0"), the luma value can be as low as the sync bottom level. This minimum luma value is available in 2xOversampling and 4xOversampling.

Timing Register Reset (TR07):
Toggling TR07 from low to high and low again resets the internal timing counters. This bit should be toggled after power-up, reset or changing to a new timing mode.

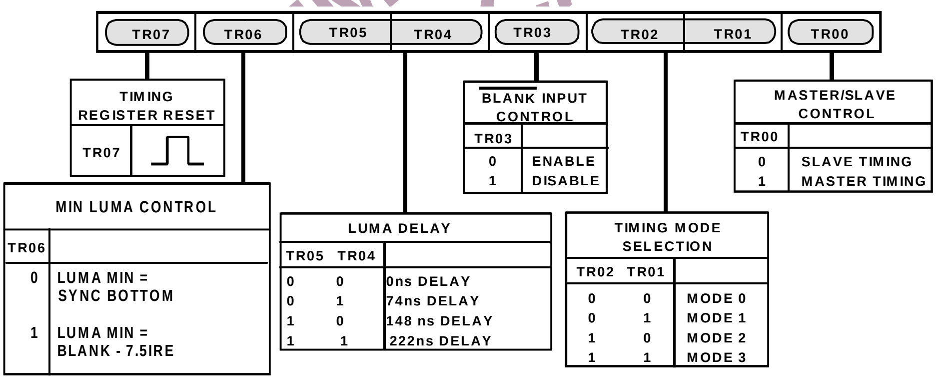


Figure 64. Timing Register 0

TIMING REGISTER 1
(TR17-TR10)
(Address (SR4-SR0) = 0BH)

Timing Register 1 is a 8-Bit wide register.

Figure 65 shows the various operations under the control of Timing Register 1. This register can be read from as well written to. This register can be used to adjust the width and position of the master mode timing signals.

TR1 BIT DESCRIPTION

HSYNC Width (TR10-TR11):
These bits adjust the HSYNC pulse width.
T_{PCLK} = one clock cycle at 27MHz.

HSYNC to VSYNC Delay (TR13-TR12):
These bits adjust the position of the HSYNC output relative to the VSYNC output.
T_{PCLK} = one clock cycle at 27MHz.

HSYNC to VSYN C Rising Edge Delay (TR14-TR15):
When the ADV7194 is in timing mode 1, these bits adjust the position of the HSYNC output relative to the VSYNC output rising edge.
T_{PCLK} = one clock cycle at 27MHz.

VSYNC Width (TR14-TR15):
When the ADV7194 is configured in timing mode 2, these bits adjust the VSYNC pulse width.
T_{PCLK} = one clock cycle at 27MHz.

HSYNC to Pixel Data Adjust (TR16-TR17):
This enables the HSYNC to be adjusted with respect to the pixel data. This allows the Cr and Cb components to be swapped. This adjustment is available in both master and slave timing modes.
T_{PCLK} = one clock cycle at 27MHz.

TR17	TR16	TR15	TR14	TR13	TR12	TR11	TR10

HSYNC TO PIXEL DATA ADJUST

TR17	TR16	
0	0	0 x T_{PCLK}
0	1	1 x T_{PCLK}
1	0	2 x T_{PCLK}
1	1	3 x T_{PCLK}

HSYNC TO VSYNC RISING EDGE DELAY (MODE 1 ONLY)

TR15	TR14	T_C
x	0	T_B
x	1	T_B + 32µs

VSYNC WIDTH (MODE 2 ONLY)

TR15	TR14	
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

HSYNC TO VSYNC DELAY

TR13	TR12	T_B
0	0	0 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	8 x T_{PCLK}
1	1	16 x T_{PCLK}

HSYNC WIDTH

TR11	TR10	T_A
0	0	1 x T_{PCLK}
0	1	4 x T_{PCLK}
1	0	16 x T_{PCLK}
1	1	128 x T_{PCLK}

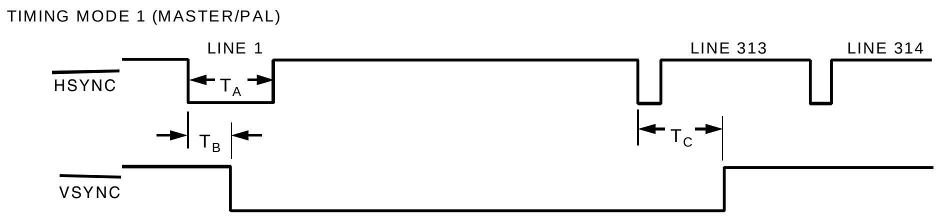


Figure 65. Timing Register 1

SUB-CARRIER FREQUENCY REGISTERS 3-0 (FSC3-FSC0)

(Address (SR4-SR0) = 0CH-0FH)

These 8-Bit wide registers are used to set up the Sub-Carrier Frequency. The value of these registers are calculated by using the following equation:

$$\text{Sub-Carrier Frequency Register} = \frac{(2^{32} - 1) * F_{SCF}}{F_{CLK}}$$

Example: NTSC Mode,
F_{CLK} = 27 MHz,
F_{SCF} = 3.5795454 MHz

$$\text{Sub-Carrier Frequency Value} = \frac{(2^{32}-1) \times 3.5795454\text{x}10^6}{27 \text{ x } 10^6}$$

Sub-Carrier Register Value = 21F07C16 HEX

Figure 66 shows how the frequency is set up by the four registers.

SUBCARRIER FREQUENCY REG 3	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
SUBCARRIER FREQUENCY REG 2	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
SUBCARRIER FREQUENCY REG 1	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC9	FSC8
SUBCARRIER FREQUENCY REG 0	FSC7	FSC6	FSC5	FSC4	FSC3	FSC2	FSC1	FSC0

Figure 66. Sub Carrier Frequency Registers

SUB-CARRIER PHASE REGISTER (FP7-FP0):

(Address (SR4-SR0) = 10H)

This 8-Bit wide register is used to set up the Sub-Carrier Phase. Each bit represents 1.41°. For normal operation this register is set to 00Hex.

SUBCARRIER PHASE REGISTER	FPH7	FPH6	FPH5	FPH4	FPH3	FPH2	FPH1	FPH0

Figure 67. Subcarrier Phase Register

CLOSED CAPTIONING EVEN FIELD DATA REGISTER 1-0 (CED15-CED00)

(Address (SR4-SR0) = 11-12H)

These 8-Bit wide registers are used to set up the closed captioning extended data bytes on Even Fields. Figure 68 shows how the high and low bytes are set up in the registers.

BYTE 1	CCD15	CCD14	CCD13	CCD12	CCD11	CCD10	CCD9	CCD8
BYTE 0	CCD7	CCD6	CCD5	CCD4	CCD3	CCD2	CCD1	CCD0

Figure 68. Closed Captioning Extended Data Register

CLOSED CAPTIONING ODD FIELD DATA REGISTER 1-0 (CCD15-CCD00)

(Subaddress (SR4-SR0) = 13-14H)

These 8-Bit wide registers are used to set up the closed captioning data bytes on Odd Fields. Figure 69 shows how the high and low bytes are set up in the registers.

BYTE 1	CED15	CED14	CED13	CED12	CED11	CED10	CED9	CED8
BYTE 0	CED7	CED6	CED5	CED4	CED3	CED2	CED1	CED0

Figure 69. Closed Captioning Data Register

NTSC PEDESTAL / PAL TELETEXT CONTROL REGISTERS 3-0 (PCE15-0, PCO15-0)/ (TXE15-0, TXO15-0)

(Subaddress (SR4-SR0) = 15-18H)

These 8-Bit wide registers are used to enable the NTSC pedestal/ PAL Teletext on a line by line basis in the vertical blanking interval for both odd and even fields. Figure 70/71 show the four control registers. A logic "1" in any of the bits of these registers has the effect of turning the Pedestal OFF on the equivalent line when used in NTSC. A logic "1" in any of the bits of these registers has the effect of turning Teletext ON on the equivalent line when used in PAL .

	LINE 17	LINE 16	LINE 15	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10
FIELD 1/3	PCO7	PCO6	PCO5	PCO4	PCO3	PCO2	PCO1	PCO0

	LINE 25	LINE 24	LINE 23	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18
FIELD 1/3	PCO15	PCO14	PCO13	PCO12	PCO11	PCO10	PCO9	PCO8

	LINE 17	LINE 16	LINE 15	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10
FIELD 2/4	PCE7	PCE6	PCE5	PCE4	PCE3	PCE2	PCE1	PCE0

	LINE 25	LINE 24	LINE 23	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18
FIELD 2/4	PCE15	PCE14	PCE13	PCE12	PCE11	PCE10	PCE9	PCE8

Figure 70. Pedestal Control Registers

	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10	LINE 9	LINE 8	LINE 7
FIELD 1/3	TXO7	TXO6	TXO5	TXO4	TXO3	TXO2	TXO1	TXO0

	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18	LINE 17	LINE 16	LINE 15
FIELD 1/3	TXO15	TXO14	TXO13	TXO12	TXO11	TXO10	TXO9	TXO8

	LINE 14	LINE 13	LINE 12	LINE 11	LINE 10	LINE 9	LINE 8	LINE 7
FIELD 2/4	TXE7	TXE6	TXE5	TXE4	TXE3	TXE2	TXE1	TXE0

	LINE 22	LINE 21	LINE 20	LINE 19	LINE 18	LINE 17	LINE 16	LINE 15
FIELD 2/4	TXE15	TXE14	TXE13	TXE12	TXE11	TXE10	TXE9	TXE8

Figure 71. Teletext Control Registers

TELETEXT REQUEST CONTROL REGISTER TC07 (TC07-TC00)

(Address (SR4-SR0) = 1CH)

Teletext Control Register is a 8-bit wide register. See Figure 72

TTXREQ FALLING EDGE CONTROL (TC00-TC03)

These bits control the position of the falling edge of TTXREQ. It can be programmed from zero clock cycles to a max of 15 clock cycles. This controls the active window for Teletext data. Increasing this value reduces the amount of Teletext bits below the default of 360. If Bits TC00-TC03 are 00Hex when Bits TC04-TC07 are changed then the falling egde of TTREQ will track that of the rising edge (i.e. the time between the falling and rising edge remains constant).

PCLK = clock cycle at 27MHz.

TTXREQ Rising Edge Control (TC04-TC07):

These bits control the position of the rising edge of TTXREQ. It can be programmed from zero clock cycles to a max of 15 clock cycles.

PCLK = clock cycle at 27MHz.

TC07	TC06	TC05	TC04	TC03	TC02	TC01	TC00

TTXREQ Rising Edge Control

TC07	TC06	TC05	TC04	
0	0	0	0	0 PCLK
0	0	0	1	1 PCLK
"	"	"	"	" PCLK
1	1	1	0	14 PCLK
1	1	1	1	15 PCLK

TTXREQ Falling Edge Control

TC03	TC02	TC01	TC00	
0	0	0	0	0 PCLK
0	0	0	1	1 PCLK
"	"	"	"	" PCLK
1	1	1	0	14 PCLK
1	1	1	1	15 PCLK

Figure 72 . Teletext Control Register

CGMS_WSS REGISTER 0 C/W0 (C/W07-C/W00)
(Address (SR4-SR0) = 19H)

CGMS_WSS register 0 is an 8-bit wide register. Figure 73 shows the operations under control of this register.

-C/W0 BIT DESCRIPTION-

CGMS Data (C/W00-C/W03) :
These four data bits are the final four bits of CGMS data output stream. Note it is CGMS data ONLY in these bit positions i.e. WSS data does not share this location.

CGMS CRC Check Control (C/W04) :
When this bit is enabled ("1"), the last six bits of the CGMS data i.e. the CRC check sequence is calculated internally by the ADV7194. If this bit is disabled ("0") the CRC values in the register are output to the CGMS data stream.

CGMS Odd Field Control (C/W05) :
When this bit is set ("1") CGMS is enabled for odd fields. Note this is only valid in NTSC mode.

CGMS Even Field Control (C/W06) :
When this bit is set ("1") CGMS is enabled for even fields. Note this is only valid in NTSC mode.

Wide Screen Signal Control (C/W07) :
When this bit is set ("1"), wide screen signalling is enabled. Note this is only valid in PAL mode.

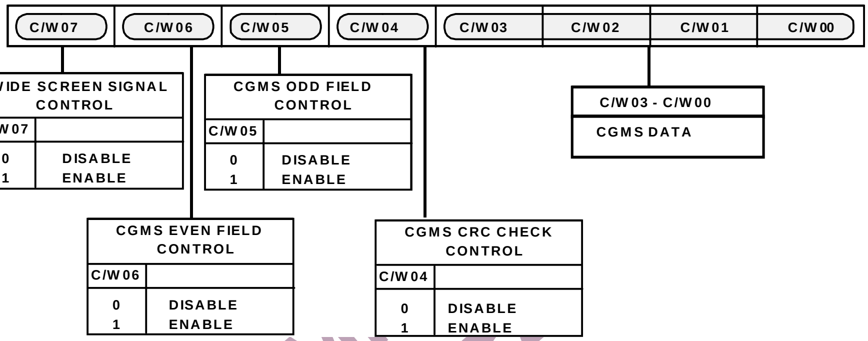


Figure 73. CGMS_WSS Register 0

CGMS_WSS REGISTER 1
C/W1 (C/W17-C/W10)
(Address (SR4-SR0) = 1AH)

CGMS_WSS register 1 is an 8-bit wide register. Figure 74 shows the operations under control of this register.

-C/W1 BIT DESCRIPTION-

CGMS/WSS Data (C/W10-C/W15) :
These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

CGMS Data (C/W16-C/W17) :
These bits are CGMS data bits only.

CGMS_WSS REGISTER 2
C/W1 (C/W27-C/W20)
(Address (SR4-SR0) = 1BH)

CGMS_WSS register 2 is an 8-bit wide register.Figure 75 shows the operations under control of this register.

-C/W2 BIT DESCRIPTION-

CGMS/WSS Data (C/W20-C/W27) :
These bit locations are shared by CGMS data and WSS data. In NTSC mode these bits are CGMS data. In PAL mode these bits are WSS data.

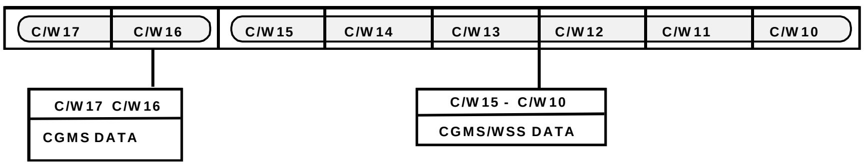


Figure 74. CGMS_WSS Register 1

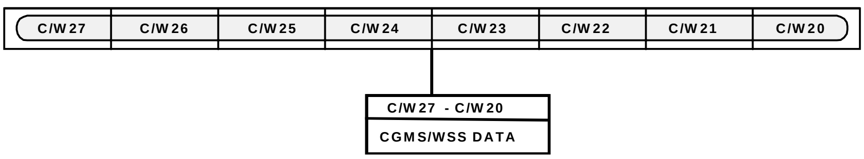


Figure 75. CGMS_WSS Register 2

CONTRAST CONTROL REGISTER
(CC00-CC07)
(Address (SR4-SR0) = 1DH)

The contrast control register is an 8-bit wide register used to scale the Y output levels. Figure 76 shows the operation under control of this register.

Y Scale Value (CC00-CC07) :

These eight bits represent the value required to scale the Y pixel data from 0.0 to 1.5 of its initial level. The value of these eight bits is calculated using the following equation:

Y Scale Value = Scale factor * 128

Example:

Scale factor = 1.18

Y Scale Value = 1.18 * 128 = 151.04
Y Scale Value= 151 (rounded to the nearest integer)
Y Scale Value = 10010111_b
Y Scale Value = 97_h

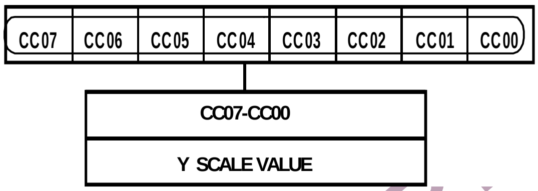


Figure 76. Contrast Control Register

COLOUR CONTROL REGISTERS 1-2
(CC1-CC2)
(Address (SR4-SR0) = 1EH-1FH)

The colour control registers are 8-bit wide registers used to scale the U and V output levels. Figure 77 shows the operations under control of these registers.

-CC1 BIT DESCRIPTION-

U Scale Value (CC10-CC17) :

These eight bits represent the value required to scale the U level from 0.0 to 2.0 of its initial level. The value of these eight bits is calculated using the following equation:

U Scalar Value = Scale factor * 128

Example:

Scale factor = 1.18

U Scale Value = 1.18 * 128 = 151.04
U Scale Value= 151 (rounded to the nearest integer)
U Scale Value = 10010111_b
U Scale Value = 97_h

-CC2 BIT DESCRIPTION-

V Scale Value (CC20-CC27) :

These eight bits represent the value required to scale the V pixel data from 0.0 to 2.0 of its initial level. The value of these eight bits is calculated using the following equation:

Example:

Scale factor = 1.18

V Scale Value = 1.18 * 128 = 151.04
V Scale Value= 151 (rounded to the nearest integer)
V Scale Value = 10010111_b
V Scale Value = 97_h

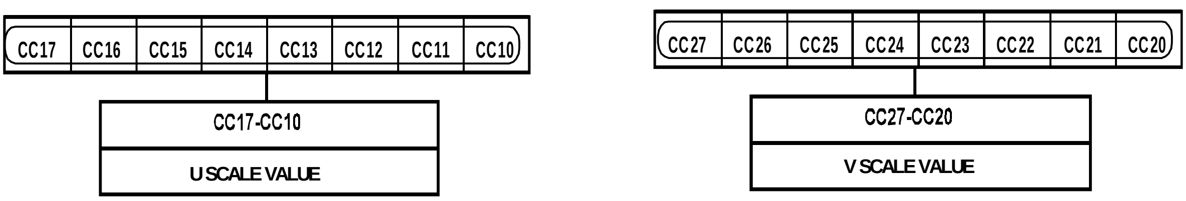


Figure 77. Color Control Registers

HUE ADJUST CONTROL REGISTER (HCR)

(Address (SR5-SR0) = 20H)

The hue control register is an 8-bit wide register used to adjust the hue on the composite and chroma outputs. Figure 78 shows the operation under control of this register.

-HCR BIT DESCRIPTION-

Hue Adjust Value (HCR0-HCR7) :

These eight bits represent the value required to vary the hue of the video data i.e. the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the colorburst. The ADV7194 provides a range of +/- 22.5° increments of 0.17578125°. For normal operation (zero adjustment) this register is set to 80Hex. FFHex and 00Hex represent the upper and lower limit (respectively) of adjustment attainable.

(Hue Adjust) [°] = 0.17578125° x(HCR_d -128) , for positive Hue Adjust Value.

EXAMPLE

To adjust the hue by +4° write 97_h to the Hue Control Register:

$(4 / 0.17578125) + 128 = 151_d^* = 97_h$

* rounded to the nearest integer

To adjust the hue by -4° write 69_h to the Hue Control Register:

$(-4 / 0.17578125) + 128 = 105_d^* = 69_h$

* rounded to the nearest integer

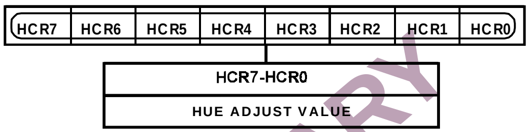


Figure 78. Hue Adjust Control Register

BRIGHTNESS CONTROL REGISTER (BCR)

(Address (SR5-SR0) = 21H)

The brightness control register is an 8-bit wide register which allows brightness control. Figure 79 shows the operation under control of this register.

-BCR BIT DESCRIPTION-

Brightness Value (BCR0-BCR6) :

Seven bits of this 8-bit wide register are used to control the brightness level. The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level can be a positive or negative value.
The programmable brightness levels in NTSC without Pedestal and PAL are maximum +15IRE and minimum -7.5IRE, in NTSC with Pedestal maximum 22.5 IRE and minimum 0IRE.

EXAMPLE:
Standard: NTSC with Pedestal.
To add +20IRE brightness level write 28_H into the Brightness Control Register:

[Brightness Control Register Value]$_H$ =
[IRE Value *2.015631]$_H$ =
[20 *2.015631]$_H$ = [40.31262]$_H$ = 28_H

Standard: PAL.
To add -7 IRE brightness level write 72_H into the Brightness Control Register:

[|IRE Value| *2.015631] =
[7 *2.015631] = [14.109417] = 0001110_B
[0001110] into 2's complement = [1110010]$_B$ = 72_H

SET-UP LEVEL IN NTSC WITH PEDESTAL	SET-UP LEVEL IN NTSC NO PEDESTAL	SET-UP LEVEL IN PAL	BRIGHTNESS CONTROL REGISTER VALUE
22.5 IRE	15 IRE	15 IRE	$1E_h$
15 IRE	7.5 IRE	7.5 IRE	$0F_h$
7.5 IRE	0 IRE	0 IRE	00_h
0 IRE	- 7.5 IRE	- 7.5 IRE	71_h

Figure 79. Possible output levels for given Brightness Control register values

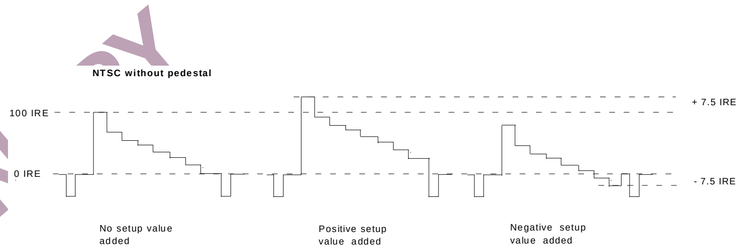


Figure 81. Adding a positve or negative Brightness Value to an unscaled Y signal

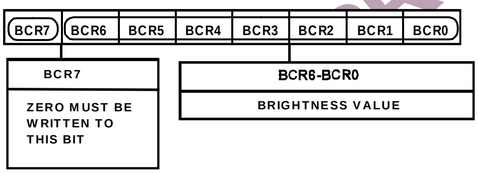


Figure 80. Brightness Control Register

SHARPNESS CONTROL REGISTER (PR)

(Address (SR5-SR0) = 22H)

The sharpness response register is an 8-bit wide register. The four MSBs are set to "0". The four LSBs are written to in order to select a desired filter response. Figure 82 shows the operation under control of this register.

-PR BIT DESCRIPTION-

Sharpness Response Value (PR3-PR0) :

These four bits are used to select the desired luma filter response. The option of twelve responses is given supporting a gain boost/attenuation in the range -4dB to +4dB. The value 12 (1100) written to these four bits corresponds to a boost of +4dB while the value 0 (0000) corresponds to -4dB. For normal operation these four bits are set to 6 (0110).Note: 'Luma Filter Select' has to be set to 'Extended Mode' and 'Sharpness Filter Enable' Control has to be enabled for settings in the Sharpness Control Register to take effect (MR02-04 = '100' ; MR74 = '1').
Refer to figures 12-15 for the filter responses.

Reserved (PR4-PR7) :

A logical "0" must be written to these bits.

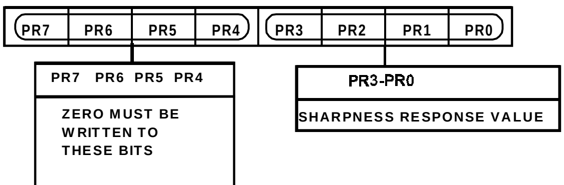


Figure 82. Sharpness Control Register

DNR REGISTERS 2 -0
(DNR 2 - DNR 0)
(Address (SR5-SR0) = 23H - 25H)

The Digital Noise Reduction Registers are three 8-bit wide register. They are used to control the DNR processing. See also page 27.

Coring Gain Border (DNR00-DNR03) :
These four bits are assigned to the gain factor applied to border areas .
In DNR Mode the range of gain values is 0 - 1, in increments of 1/8. This factor is applied to the DNR filter output which lies below the set threshold range. The result is then subtracted from the original signal.
In DNR Sharpness Mode the range of gain values is 0 - 0.5, in increments of 1/16. This factor is applied to the DNR filter output which lies above the threshold range.
The result is added to the original signal.

Coring Gain Data (DNR04-DNR07) :
These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block.
In DNR Mode the range of gain values is 0 - 1, in increments of 1/8. This factor is applied to the DNR filter output which lies below the set threshold range. The result is then subtracted from the original signal.
In DNR Sharpness Mode the range of gain values is 0 - 0.5, in increments of 1/16. This factor is applied to the DNR filter output which lies above the threshold range.
The result is added to the original signal.
Figure 83, 84 show the various operations under the control of DNR Register 0.

DNR07	DNR06	DNR05	DNR04	DNR03	DNR02	DNR01	DNR00

Coring Gain Data

DNR 07	DNR 06	DNR 05	DNR 04	
0	0	0	0	
0	0	0	1	+ 1/16
0	0	1	0	+ 2/16
0	0	1	1	+ 3/16
0	1	0	0	+ 4/16
0	1	0	1	+ 5/16
0	1	1	0	+ 6/16
0	1	1	1	+ 7/16
1	0	0	0	+ 8/16

Coring Gain Border

DNR 03	DNR 02	DNR 01	DNR 00	
0	0	0	0	
0	0	0	1	+ 1/16
0	0	1	0	+ 2/16
0	0	1	1	+ 3/16
0	1	0	0	+ 4/16
0	1	0	1	+ 5/16
0	1	1	0	+ 6/16
0	1	1	1	+ 7/16
1	0	0	0	+ 8/16

Figure 83. DNR Register 0 in DNR Sharpness Mode

DNR07	DNR06	DNR05	DNR04	DNR03	DNR02	DNR01	DNR00

Coring Gain Data

DNR 07	DNR 06	DNR 05	DNR 04	
0	0	0	0	0
0	0	0	1	- 1/8
0	0	1	0	- 2/8
0	0	1	1	- 3/8
0	1	0	0	- 4/8
0	1	0	1	- 5/8
0	1	1	0	- 6/8
0	1	1	1	- 7/8
1	0	0	0	- 1

Coring Gain Border

DNR 03	DNR 02	DNR 01	DNR 00	
0	0	0	0	0
0	0	0	1	- 1/8
0	0	1	0	- 2/8
0	0	1	1	- 3/8
0	1	0	0	- 4/8
0	1	0	1	- 5/8
0	1	1	0	- 6/8
0	1	1	1	- 7/8
1	0	0	0	- 1

Figure84. DNR Register 0 in DNR Mode

DNR1 BIT DESCRIPTION-
DNR Threshold (DNR10 - DNR 15):
These 6 bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.
Border Area (DNR16):
In setting DNR16 to a logic '1' the block transistion area can be defined to consist of 4 pixels. If this bit is set to a logic '0' the border transition area consists of 2 pixels, where 1 pixel refers to 2 clock cycles at 27MHz.
Block size control (DNR17):
This bit is used to select the size of the data blocks to be processed (see figure 82). Setting the block size control function to a logic '1' defines a 16x16 pixel data block, a logic '0' defines an 8x8 pixel data block, where 1 pixel refers to 2 clock cycles at 27 MHz.

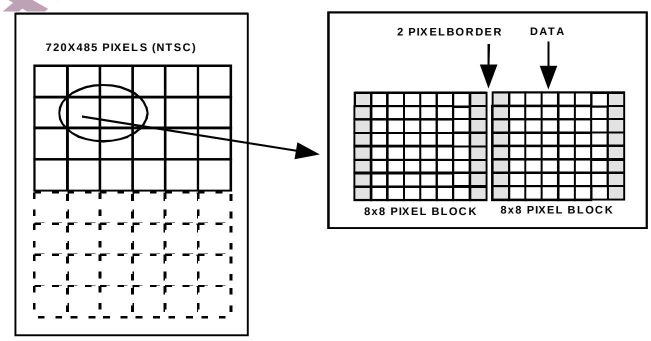


Figure 85. MPEG Block diagram

DNR17	DNR16	DNR15	DNR14	DNR13	DNR12	DNR11	DNR10

BLOCK SIZE CONTROL

DNR17	
0	8 PIXELS
1	16 PIXELS

BORDER AREA

DNR16	
0	2 PIXELS
1	4 PIXELS

DNR THRESHOLD

DNR 15	DNR 14	DNR 13	DNR 12	DNR 11	DNR 10	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Figure 86 DNR Register 1

DNR2 BIT DESCRIPTION-

DNR Input Select Control (DNR20-DNR22):
Three bits are assigned to select the filter which is applied to the incoming Y data.The signal which lies in the passband of the selected filter is the signal which will be DNR processed. The figure below show the filter responses selectable with this control.

DNR Mode Control (DNR23):
This bit controls the DNR mode selected. A logic '0' selects DNR mode, a logic '1' selects DNR Sharpness mode.

DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR mode, it is possible to subtract a fraction of the signal which lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR Sharpness mode is enabled it is possible to add a fraction of the signal which lies above the set threshold to the original signal, since this data is assumed to be valid data and not noise. The overall effect being that the signal will be boosted (similar to using Extended SSAF™ filter) .

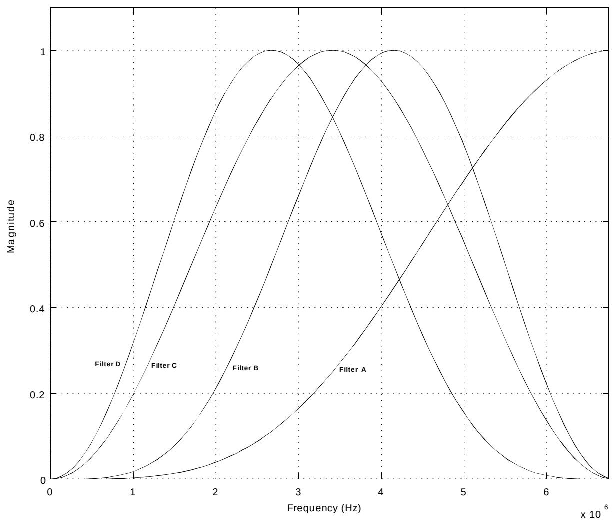


Figure 87. Filter Response of filters selectable

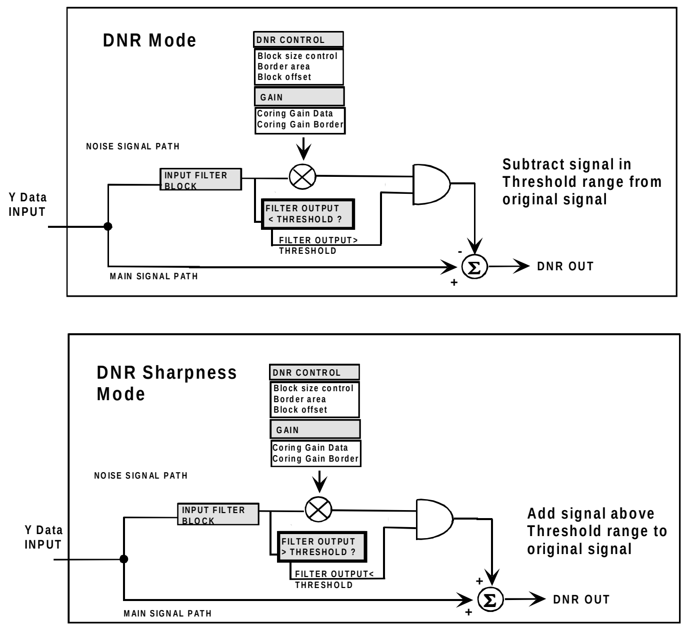


Figure 88 Block diagram for DNR Mode and DNR Sharpness Mode

Block Offset Control (DNR24- DNR27):
Four bits are assigned to this control which allows a shift of the data block of 15 pixels maximum. Consider the coring gain positions fixed. The block offset 'shifts' the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

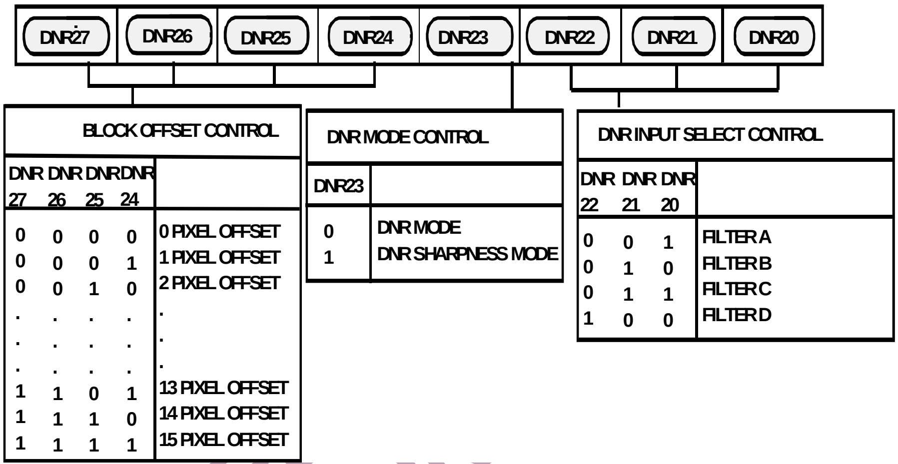


Figure 89. DNR Register 2

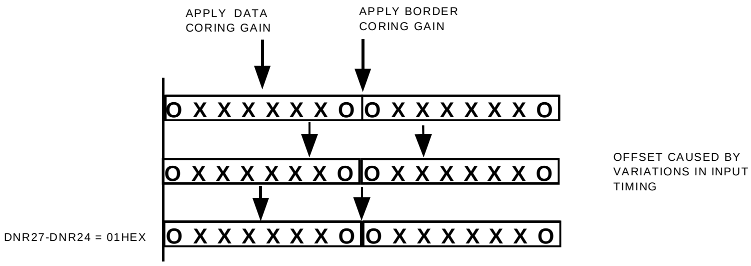


FIGURE 90 DNR 27-24, BLOCK OFFSET CONTROL

GAMMA CORRECTION REGISTERS 0- 13
(GAMMA 0-13)
(Address (SR5-SR0) = 26H -33H)

The Gamma Correction Registers are fourteen 8-bit wide register. They are used to program the gamma correction curves A and B.

Generally gamma correction is applied to compensate for the non linear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever non-linear processing is used.

Gamma correction uses the function :

$$Signal_{OUT} = (Signal_{IN})^{\gamma}$$

where δ = gamma power factor

Gamma correction is performed on the luma data only. The user has the choice to use two different curves, curve A or curve B. At any one time only one of these curves can be used.

The response of the curve is programmed at 7 pre-defined locations. In changing the values at these locations the gamma curve can be modified. Between these points linear interpolation is used to generate intermediate values. Considering the curve to have a total length of 256 points, the seven locations are at: 32, 64, 96, 128, 160, 192, 224.

Location 0, 16, 240 and 255 are fixed and can not be changed.

For the length of 16 to 240 the gamma correction curve has to be calculated as below:

$$y = x^{\gamma}$$

where y = gamma corrected output

x = linear input signal

γ = gamma power factor

To program the gamma correction registers, the 7 values for y have to be calculated using the following formulare:

$$y_n = [\, x_{(n-16)} / (240 - 16)\,]^{\gamma} \times (240-16) + 16$$

where

$x_{(n-16)}$ = Value for x along x-axis at points n = 32, 64, 96, 128, 160, 192 or 224

y_n = Value for y along the y-axis, which has to be written into the gamma correction register .

EXAMPLE:

y_{32} = [(16 / 224)$^{0.5}$ x 224] + 16 = 76*
y_{64} = [(48 / 224)$^{0.5}$ x 224] + 16 =120*
y_{96} = [(80 / 224)$^{0.5}$ x 224] + 16 = 150*
y_{128} = [(112 / 224)$^{0.5}$ x 224] + 16 = 174*
* rounded to the nearest integer

The above will result in a gamma curve shown below, assuming a ramp signal as an input.

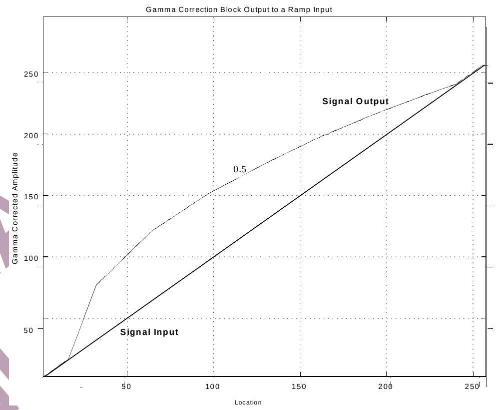


Figure 91 Signal Input (Ramp) and Signal Output for Gamma 0.5

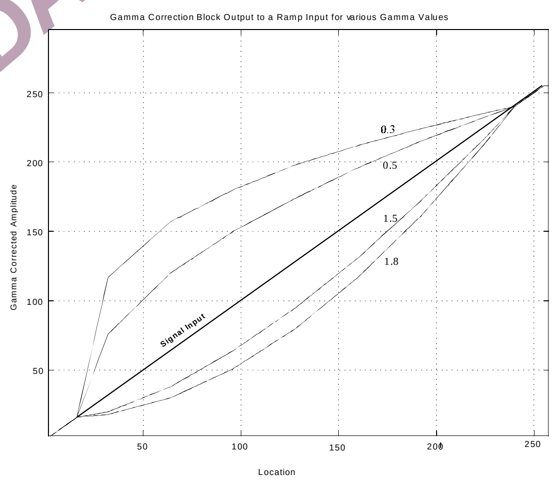


Figure 92 Signal Input (Ramp) and selectable Gamma Output curves

The gamma curves shown above are examples only, any user defined curve is acceptable in the range of 16 - 240.

BRIGHTNESS DETECT REGISTER
(Address (SR5-SR0) = 34H)

The Brightness Detect Register is a 8-bit wide register used only to read back data in order to monitor the brightness/darkness of the incoming video data on a field-by-field basis. The brightness information is read from the I2C and based on this information, the color controls or the gamma correction controls may be adjusted.

The luma data is monitored in the active video area only. The average brightness I2C register is updated on the fallling edge of every VSYNC signal.

OUTPUT CLOCK REGISTER (OCR 9-0)
(Address (SR4-SR0) = 35H)

The Output Clock Register is a 8-Bit wide register. Figure 93 shows the various operations under the control of this register.

OCR BIT DESCRIPTION

Reserved (OCR00):
A logic '0' must be written to this bit.

CLKOUT pin Control (OCR01):
This bit enables the CLKOUT pin when set to '1' and therefore outputs a 54MHz clock generated by the internal PLL. The PLL and 4xOversampling have to be enabled for this control to take effect, (MR61 = ' 0' ; MR16 = '1').

Reserved (OCR02):
A logic '0' must be written to this bit.

Reserved (OCR03-06):
A logic '1' must be written to these bits.

Reserved (OCR07):
A logic '0' must be written to this bit.

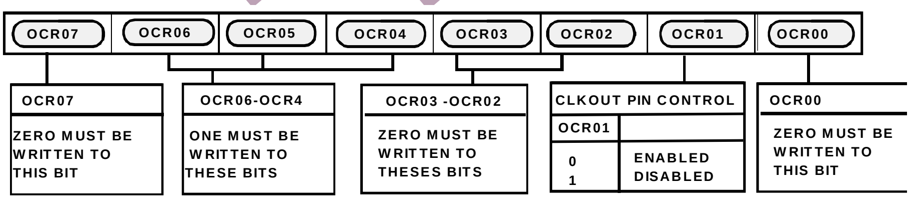


Figure 93. Output Clock Register

APPENDIX 1

BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7194 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7194 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7194 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7194, the analog output traces, and all the digital signal traces leading up to the ADV7194.
This should be as substantial as possible to maximize heat spreading and power dissipation on the board.

Power Planes

The ADV7194 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7194.
The metallization gap separating device power plane and board power plane should be as narrow as possible to minimise the obstruction to the flow of heat from the device into the general board.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7194 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common-mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7194 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7194 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three- terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7194 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7194 should be avoided to reduce noise pickup.
Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7194 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital inputs, especially pixel data inputs and clocking signals should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the outputs should each have a 300ohm load resistor connected to GND. These resistors should be placed as close as possible to the ADV7194 so as to minimize reflections.

The ADV7194 should have no inputs left floating. Any inputs that are not required should be tied to ground.

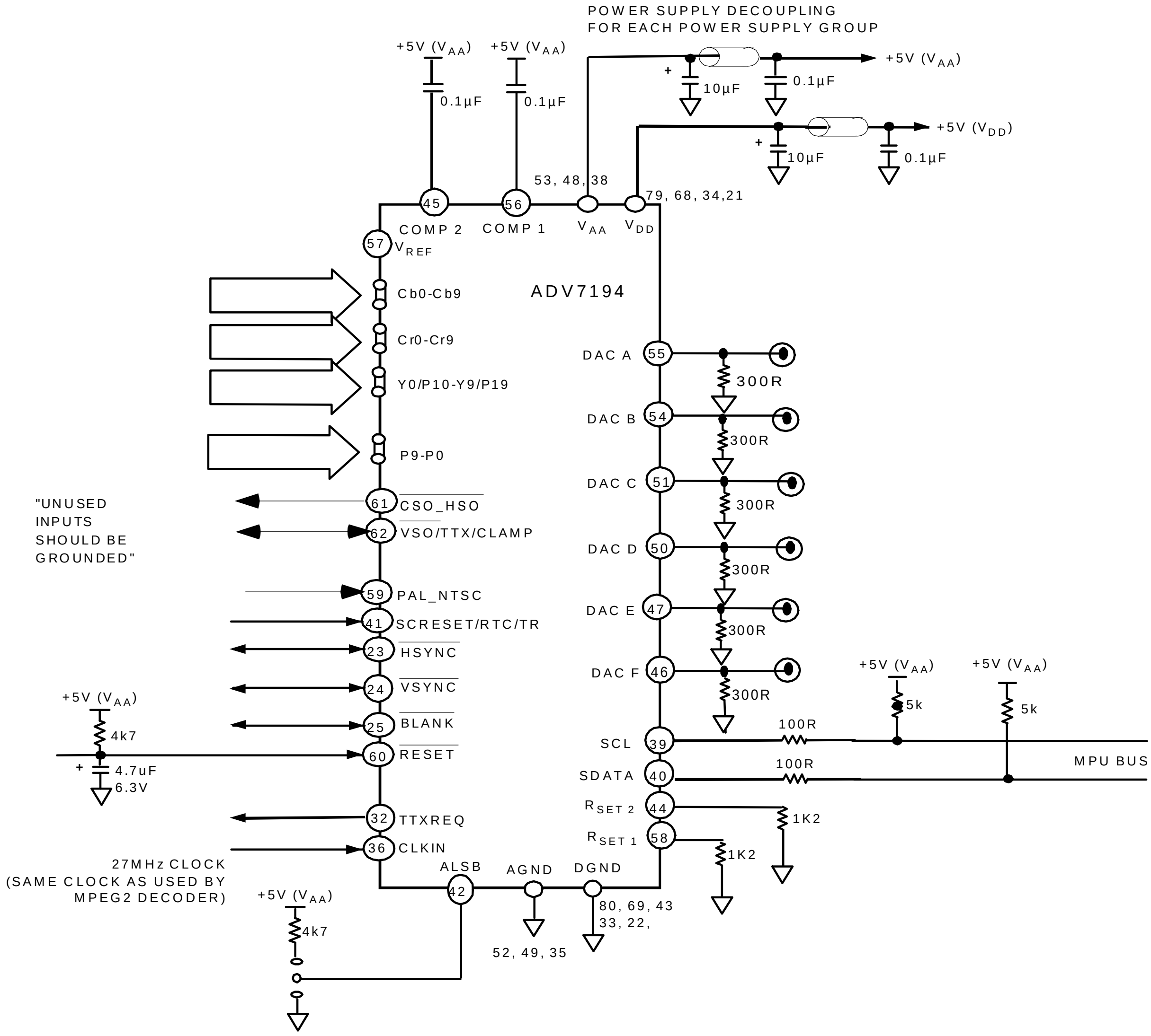


Figure 94. Recommended Analog Circuit Layout

APPENDIX 2

CLOSED CAPTIONING

The ADV7194 supports closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency and phase locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a logic level "1" start bit. 16 bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits and one odd parity bit. The data for these bytes is stored in Closed Captioning Data Registers 0 and 1.

The ADV7194 also supports the extended closed captioning operation which is active during even fields and is encoded on Scan Line 284. The data for this operation is stored in Closed Captioning Extended Data Registers 0 and 1.

All clock run-in signals and timing to support Closed Captioning on Lines 21 and 284 are generated automatically by the ADV7194. All pixels inputs are ignored during Lines 21 and 284 if closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA608 describe the closed captioning information for Lines 21 and 284.

The ADV7194 uses a single buffering method. This means that the closed captioning buffer is only one byte deep, therefore there will be no frame delay in outputting the closed captioning data unlike other two byte deep buffering systems. The data must be loaded one line before (Line 20 or Line 283) it is outputted on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn will load the new data (two bytes) every field. If no new data is required for transmission, "0"es must be inserted in both data registers, this is called NULLING. It is also important to load 'control codes' all of which are double bytes on Line 21 or a TV will not recognize them. If there is a message like "Hello World" which has an odd number of characters, it is important to pad it out to even in order to get "end of caption" 2-byte control code to land in the same field.

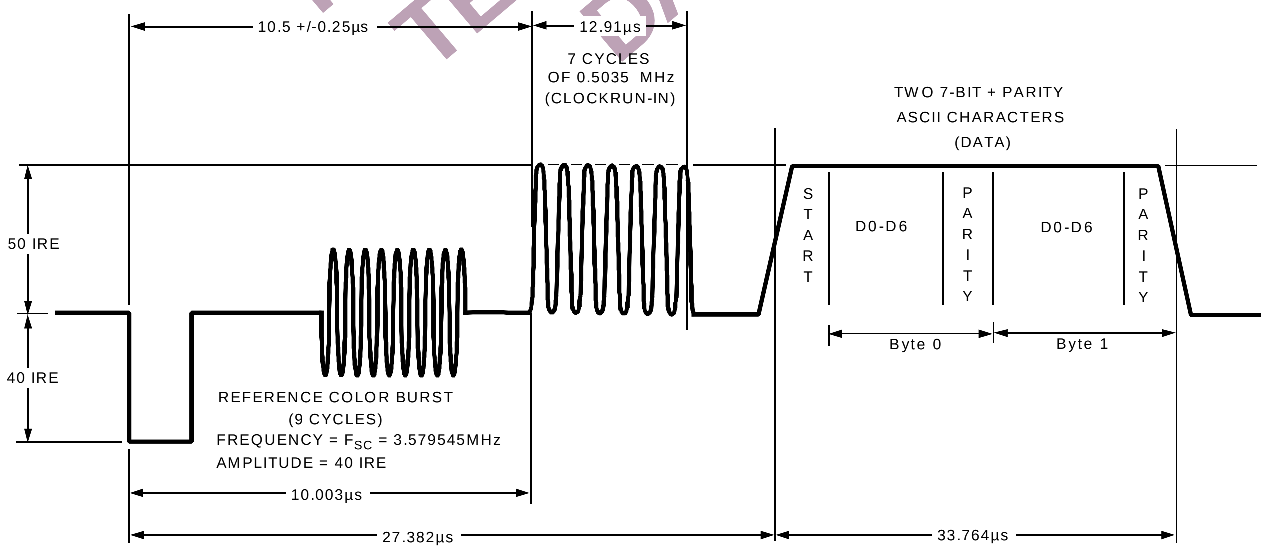


Figure 95. Closed Captioning Waveform (NTSC)

APPENDIX 3

COPY GENERATION MANAGEMENT SYSTEM (CGMS)

The ADV7194 supports Copy Generation Management System (CGMS) conforming to the standard. CGMS data is transmitted on Line 20 of the odd fields and Line 283 of even fields. Bits C/W05 and C/W06 control whether or not CGMS data is outputed on ODD and EVEN fields. CGMS data can only be transmitted when the ADV7194 is configured in NTSC mode. The CGMS data is 20 bits long, the function of each of these bits is as shown below. The CGMS data is preceeded by a reference pulse of the same amplitude and duration as a CGMS bit, see figure below. These bits are outputed from the configuration registers in the following order: C/W00 = C16, C/W01= C17, C/W02 = C18, C/W03 = C19, C/W10 = C8 , C/W11 = C9, C/W12 = C10, C/W13 = C11, C/W14 = C12, C/W15 = C13, C/W16 = C14 , C/W17 = C15 , C/W20 = C0 , C/W21 = C1, C/W22 = C2, C/W23 = C3, C/W24 = C4, C/W25 = C5, C/W26 = C6, C/W27= C7. If the bit C/W04 is set to a logic "1", the last six bits C19-C14 which comprise the 6-bit CRC check sequence are calculated automatically on the ADV7194 based on the lower 14 bits (C0-C13) of the data in the data registers and output with the remaining 14-bits to form the complete 20-bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $X^6 + X + 1$ with a preset value of 111111. If C/W04 is set to a logic "0" then all 20-bits (C0-C19) are output directly from the CGMS registers (no CRC calculated, must be calculated by the user).

Function of CGMS bits:

WORD 0 - 6 BITS
WORD 1 - 4 BITS
WORD 2 - 6 BITS
CRC - 6 BITS CRC polynomial = $X^6 + X + 1$ (preset to 111111)

WORD 0		1	0
B1	Aspect ratio	16:9	4:3
B2	Display format	Letterbox	Normal
B3	Undefined		

WORD 0
B4,B5,B6 Identification information about video and other signals (e.g. audio)

WORD 1
B7,B8,B9,B10 Identification signal incidental to Word 0

WORD 2
B11,B12,B13,B14 Identification signal and information incidental to Word 0

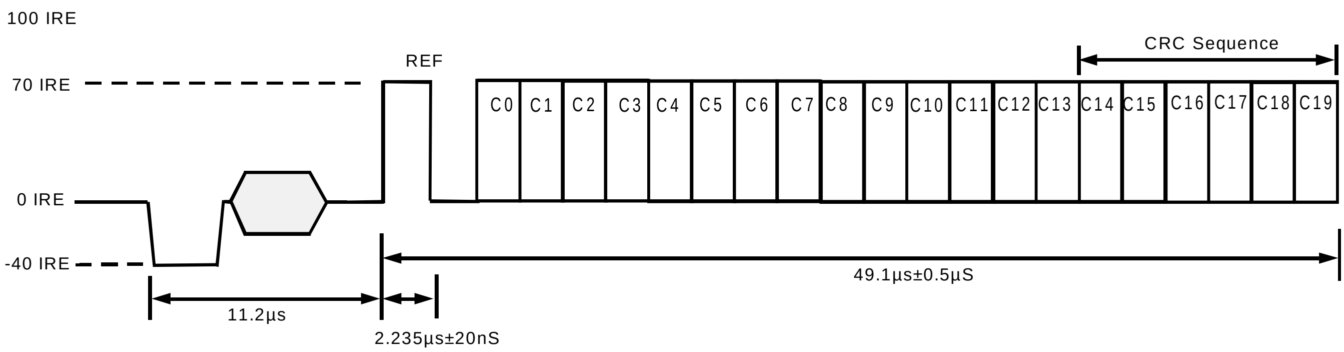


Figure 96. CGMS Waveform diagram

APPENDIX 4

WIDE SCREEN SIGNALLING

The ADV7194 supports Wide Screen Signalling (WSS) conforming to the standard. WSS data is transmitted on line 23. WSS data can only be transmitted when the ADV7194 is configured in PAL mode. The WSS data is 14-bits long, the function of each of these bits is as shown below. The WSS data is preceeded by a run-in sequence and a Start Code, see figure below. The bits are output from the configuration registers in the following order: C/W20 = W0, C/W21= W1, C/W22 = W2, C/W23 = W3, C/W24 = W4 , C/W25 = W5, C/W26 = W6, C/W27 = W7, C/W10 = W8, C/W11 = W9, C/W12 = W10 , C/W13 = W11 , C/W14 = W12 , C/W15 = W13 . If the bit C/W07 is set to a logic "1" it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5µs from the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video.

Function of CGMS bits:

Bit 0 - Bit 2 Aspect Ratio / Format / Position
Bit 3 is odd parity check of Bit 0 -Bit 2

B0, B1, B2,B3	Aspect Ratio	Format	Position
0 0 0 1	4:3	Full Format	non-applicable
1 0 0 0	14:9	Letterbox	centre
0 1 0 0	14:9	Letterbox	top
1 1 0 1	16:9	Letterbox	centre
0 0 1 0	16:9	Letterbox	top
1 0 1 1	>16:9	Letterbox	centre
0 1 1 1	14:9	Full Format	centre
1 1 1 0	16:9	non-applicable	non-applicable

B4
0 Camera Mode
1 Film Mode

B5
0 Standard coding
1 Motion Adaptive Colour Plus

B6
0 No Helper
1 Modulated Helper

B7 RESERVED

B9	B10	
0	0	No open subtitles
1	0	Subtitles in active image area
0	1	Subtitles out of active image area
1	1	Reserved

B11
0 No surround sound information
1 Surround sound mode

B12 RESERVED
B13 RESERVED

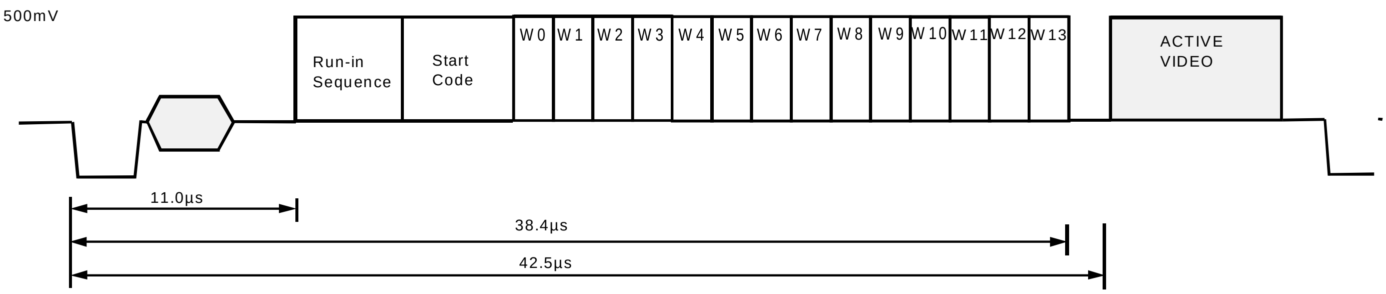


Figure 97. WSS Waveform diagram

APPENDIX 5

Teletext Insertion

Time T_{PD} is the time needed by the ADV7194 to interpolate input data on TTX and insert it onto the CVBS or Y outputs, such that it appears $T_{synTxtOut}$ = 10.2µs after the leading edge of the horizontal signal. Time Txt_{Del} is the pipeline delay time by the source that is gated by the TTREQ signal in order to deliver TTX data.

With the programability that is offered with TTXREQ signal on the Rising/Falling edges, the TTX data is always inserted at the correct position of 10.2µs after the leading edge of Horizontal Sync pulse, thus this enables a source interface with variable pipeline delays.

The width of the TTXREQ signal must always be maintained such that it allows the insertion of 360 (in order to comply with the Teletext Standard "PAL-WST") teletext bits at a text data rate of 6.9375Mbits/s, this is achieved by setting TC03-TC00 to "0". The insertion window is not open if the Teletext Enable bit (MR34) is set to "0".

Teletext Protocol

The relationship between the TTX bit clock (6.9375MHz) and the system CLOCK (27MHz) for 50Hz is given as follows:

$$(27MHz / 4) = 6.75MHz$$
$$(6.9375 \times 10^6 / 6.75 \times 10^6 = 1.027777$$

Thus 37 TTX bits correspond to 144 clocks (27MHz), each bit has a width of almost 4 clock cycles. The ADV7192/93 uses an internal sequencer and variable phase interpolation filter to minimize the phase jitter and thus generate a bandlimited signal which can be output on the CVBS and Y outputs.

At the TTX input the bit duration scheme repeats after every 37 TTX bits or 144 clock cycles. The protocol requires that TTX Bits 10, 19, 28, 37 are carried by three clock cycles, all other bits by four clock cycles. After 37 TTX bits, the next bits with three clock cycles are Bits 47, 56, 65 and 74. This scheme holds for all following cycles of 37 TTX bits, until all 360 TTX bits are completed. All teletext lines are implemented in the same way. Individual control of teletext lines are controlled by Teletext Setup Registers.

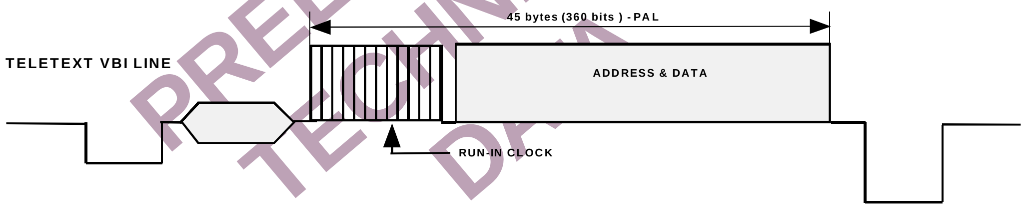
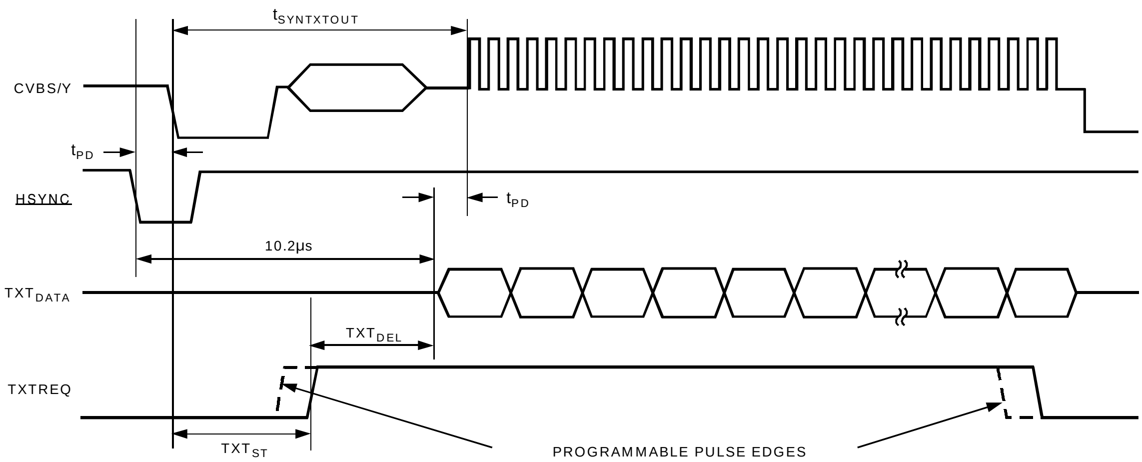


Figure 98. Teletext VBI Line



$t_{SYNTXTOUT}$ = 10.2µs
t_{PD} = PIPELINE DELAY THROUGH ADV7194
TXT_{DEL} = TTXREQ TO TTX (PROGRAMMABLE RANGE = 4 BITS [0-15 CLOCK CYCLES])

Figure 99. Teletext Functionality Diagram

APPENDIX 6

OPTIONAL OUTPUT FILTER

If an output filter is required for the CVBS, Y, UV, Chroma and RGB outputs of the ADV7194, the filter in Figure 100 can be used in 2xOversampling Mode. In4xOversampling Mode the filter in Figure 101 is recommended. The plot of the filter characteristics are shown in Figure 102 and 103. An output filter is not required if the outputs of the ADV7194 are connected to most analog monitors or TVs, however if the output signals are applied to a system where sampling is used (eg. Digital TVs) then a filter is required to prevent aliasing.

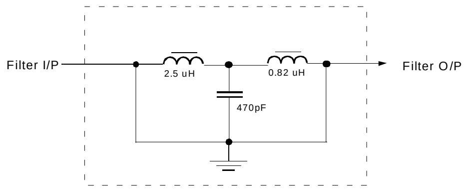


Figure 100. Output Filter for 2xOversampling Mode

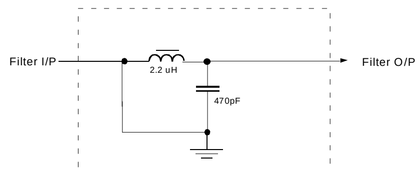


Figure 101. Output Filter for 4xOversampling Mode

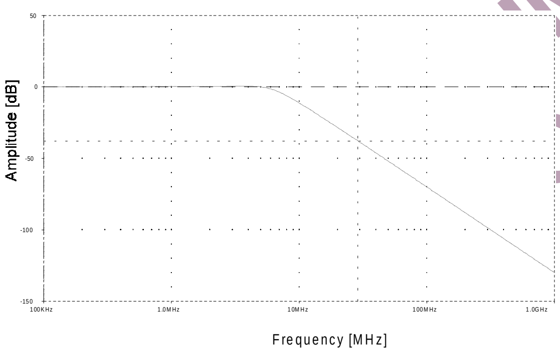


Figure 102. Output Filter Plot for 2xOversampling filter

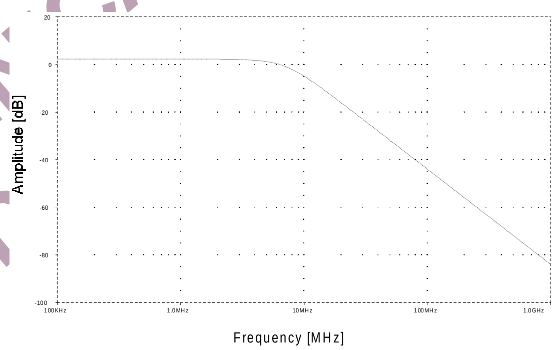


Figure 103 Output Filter Plot for 4xOversampling filter

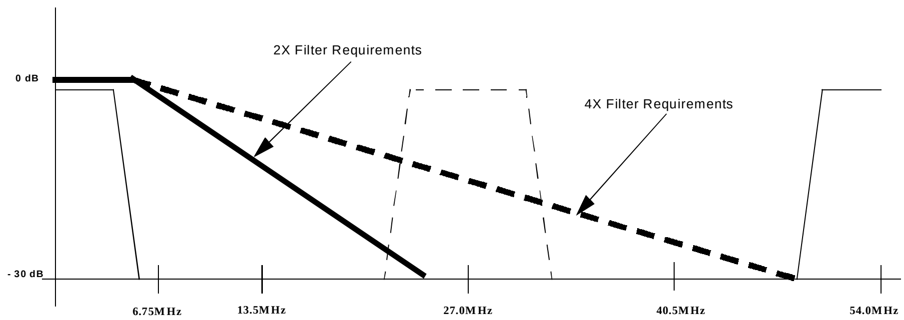


Figure 104. Output Filter Requirements in 4xOversampling Mode

APPENDIX 7

DAC BUFFERING

External buffering is needed on the ADV7194 DAC outputs. The configuration in Figure 105/106 is recommended. .

When calculating absolute output full scale current and voltage use the following equations:

$V_{OUT} = I_{OUT} * R_{LOAD}$

$I_{OUT} = (V_{REF} * K)/ R_{SET}$

K= 4.2146 constant, V_{REF} = 1.235V

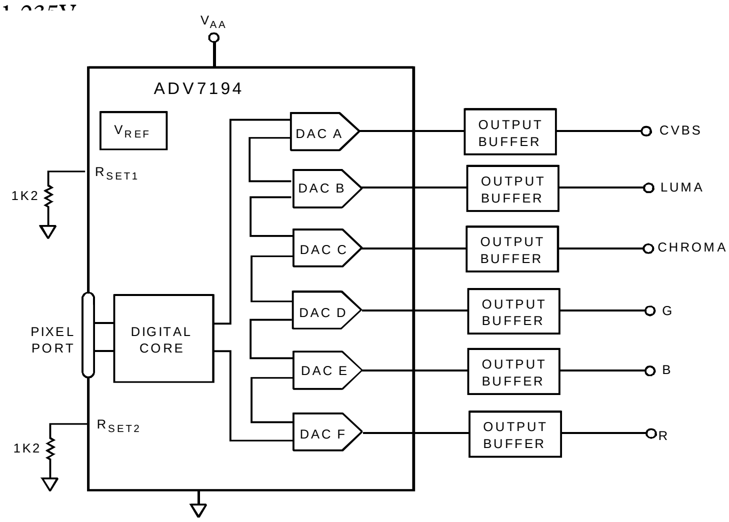


Figure 105. Output DAC Buffering Configuration

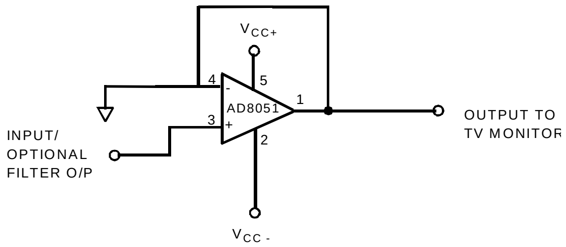


Figure 106. Recommended DAC Output Buffer using an OP-amp

APPENDIX 8

RECOMMENDED REGISTER VALUES

The ADV7194 registers can be set depending on the user standard required.
The following examples give the various register formats for several video standards.

NTSC (Fsc = 3.5795454MHz)

Address		Data
00Hex	Mode Register 0	10Hex
01Hex	Mode Register 1	3FHex
02Hex	Mode Register 2	62Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	04Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	16Hex
0DHex	Subcarrier Frequency Register 1	7CHex
0EHex	Subcarrier Frequency Register 2	F0Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR 0	44Hex
24Hex	DNR 1	20Hex
25Hex	DNR 2	00Hex
35Hex	Output Clock Register	70Hex

PAL B, D, G, H, I (Fsc = 4.43361875MHz)

Address		Data
00Hex	Mode Register 0	11Hex
01Hex	Mode Register 1	3FHex
02Hex	Mode Register 2	62Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	04Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR0	44Hex
24Hex	DNR1	20Hex
25Hex	DNR2	00Hex
35Hex	Output Clock Register	70Hex

PAL N (Fsc = 4.43361875MHz)

Address		Data
00Hex	Mode Register 0	13Hex
01Hex	Mode Register 1	3FHex
02Hex	Mode Register 2	62Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	04Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR0	44Hex
24Hex	DNR1	20Hex
25Hex	DNR2	00Hex
35Hex	Output Clock Register	70Hex

PAL 60 (Fsc = 4.43361875MHz)

Address		Data
00Hex	Mode Register 0	12Hex
01Hex	Mode Register 1	3FHex
02Hex	Mode Register 2	62Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	04Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR0	44Hex
24Hex	DNR1	20Hex
25Hex	DNR2	00Hex
35Hex	Output Clock Register	70Hex

POWER ON RESET REG VALUES
(PAL_NTSC=0, NTSC selected

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	00Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	16Hex
0DHex	Subcarrier Frequency Register 1	7CHex
0EHex	Subcarrier Frequency Register 2	F0Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR0	00Hex
24Hex	DNR1	00Hex
25Hex	DNR2	00Hex
26Hex	Gamma 0	xxHex
27Hex	Gamma 1	xxHex
28Hex	Gamma 2	xxHex
29Hex	Gamma 3	xxHex
2AHex	Gamma 4	xxHex
2BHex	Gamma 5	xxHex
2CHex	Gamma 6	xxHex
2DHex	Gamma 7	xxHex
2EHex	Gamma 8	xxHex
2FHex	Gamma 9	xxHex
30Hex	Gamma 10	xxHex
31Hex	Gamma 11	xxHex
32Hex	Gamma 12	xxHex
33Hex	Gamma 13	xxHex
34Hex	Brightness Detect Register	xxHex
35Hex	Output Clock Register	72Hex

POWER ON RESET REG VALUES
(PAL_NTSC=1, PAL selected

Address		Data
00Hex	Mode Register 0	01Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	00Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR0	00Hex
24Hex	DNR1	00Hex
25Hex	DNR2	00Hex
26Hex	Gamma 0	xxHex
27Hex	Gamma 1	xxHex
28Hex	Gamma 2	xxHex
29Hex	Gamma 3	xxHex
2AHex	Gamma 4	xxHex
2BHex	Gamma 5	xxHex
2CHex	Gamma 6	xxHex
2DHex	Gamma 7	xxHex
2EHex	Gamma 8	xxHex
2FHex	Gamma 9	xxHex
30Hex	Gamma 10	xxHex
31Hex	Gamma 11	xxHex
32Hex	Gamma 12	xxHex
33Hex	Gamma 13	xxHex
34Hex	Brightness Detect Register	xxHex
35Hex	Output Clock Register	72Hex

POWER ON RESET REG VALUES

(PAL_NTSC = 0, NTSC selected)

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	00Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	16Hex
0DHex	Subcarrier Frequency Register 1	7CHex
0EHex	Subcarrier Frequency Register 2	F0Hex
0FHex	Subcarrier Frequency Register 3	21Hex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR 0	00Hex
24Hex	DNR 1	00Hex
25Hex	DNR 2	00Hex
26Hex	Gamma 0	xxHex
27Hex	Gamma 1	xxHex
28Hex	Gamma 2	xxHex
29Hex	Gamma 3	xxHex
2AHex	Gamma 4	xxHex
2BHex	Gamma 5	xxHex
2CHex	Gamma 6	xxHex
2DHex	Gamma 7	xxHex
2EHex	Gamma 8	xxHex
2FHex	Gamma 9	xxHex
30Hex	Gamma 10	xxHex
31Hex	Gamma 11	xxHex
32Hex	Gamma 12	xxHex
33Hex	Gamma 13	xxHex
34Hex	Brightness Detect Register	xxHex
35Hex	Output Clock Register	72Hex

POWER ON RESET REG VALUES

(PAL_NTSC = 1, PAL selected)

Address		Data
00Hex	Mode Register 0	00Hex
01Hex	Mode Register 1	07Hex
02Hex	Mode Register 2	08Hex
03Hex	Mode Register 3	00Hex
04Hex	Mode Register 4	00Hex
05Hex	Mode Register 5	00Hex
06Hex	Mode Register 6	00Hex
07Hex	Mode Register 7	00Hex
08Hex	Mode Register 8	00Hex
09Hex	Mode Register 9	00Hex
0AHex	Timing Register 0	08Hex
0BHex	Timing Register 1	00Hex
0CHex	Subcarrier Frequency Register 0	CBHex
0DHex	Subcarrier Frequency Register 1	8AHex
0EHex	Subcarrier Frequency Register 2	09Hex
0FHex	Subcarrier Frequency Register 3	2AHex
10Hex	Subcarrier Phase Register	00Hex
11Hex	Closed Captioning Ext Register 0	00Hex
12Hex	Closed Captioning Ext Register 1	00Hex
13Hex	Closed Captioning Register 0	00Hex
14Hex	Closed Captioning Register 1	00Hex
15Hex	Pedestal Control Register 0	00Hex
16Hex	Pedestal Control Register 1	00Hex
17Hex	Pedestal Control Register 2	00Hex
18Hex	Pedestal Control Register 3	00Hex
19Hex	CGMS_WSS Reg 0	00Hex
1AHex	CGMS_WSS Reg 1	00Hex
1BHex	CGMS_WSS Reg 2	00Hex
1CHex	Teletext Control Register	00Hex
1DHex	Contrast Control Register	00Hex
1EHex	Color Control Register 1	00Hex
1FHex	Color Control Register 2	00Hex
20Hex	Hue Control Register	00Hex
21Hex	Brightness Control Register	00Hex
22Hex	Sharpness Response Register	00Hex
23Hex	DNR 0	00Hex
24Hex	DNR 1	00Hex
25Hex	DNR 2	00Hex
26Hex	Gamma 0	xxHex
27Hex	Gamma 1	xxHex
28Hex	Gamma 2	xxHex
29Hex	Gamma 3	xxHex
2AHex	Gamma 4	xxHex
2BHex	Gamma 5	xxHex
2CHex	Gamma 6	xxHex
2DHex	Gamma 7	xxHex
2EHex	Gamma 8	xxHex
2FHex	Gamma 9	xxHex
30Hex	Gamma 10	xxHex
31Hex	Gamma 11	xxHex
32Hex	Gamma 12	xxHex
33Hex	Gamma 13	xxHex
34Hex	Brightness Detect Register	xxHex
35Hex	Output Clock Register	72Hex

APPENDIX 9

NTSC WAVEFORMS (WITH PEDESTAL)

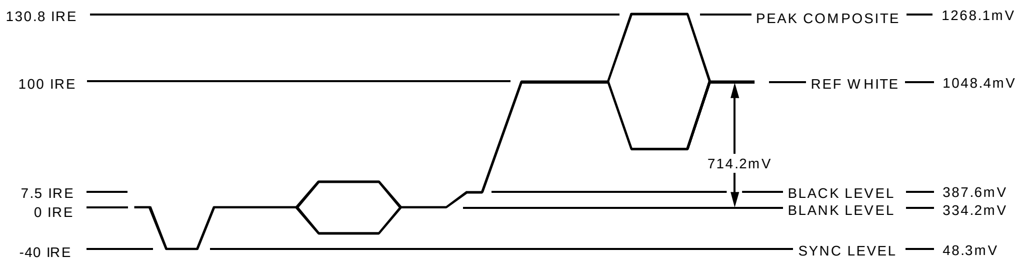


Figure 107. NTSC Composite Video Levels

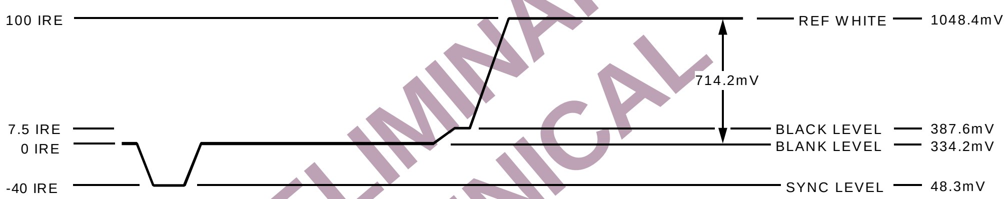


Figure 108. NTSC Luma Video Levels

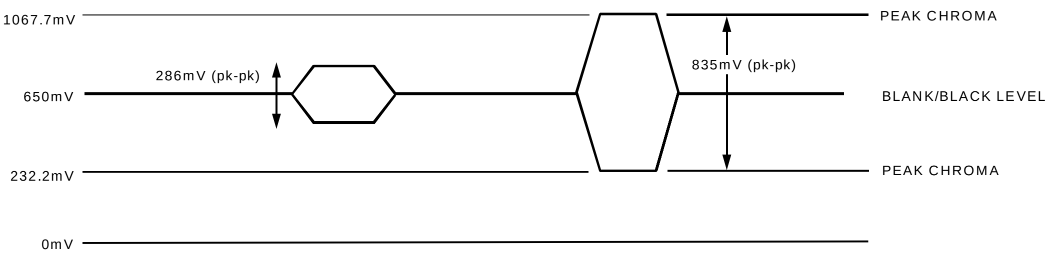


Figure 109. NTSC Chroma Video Levels

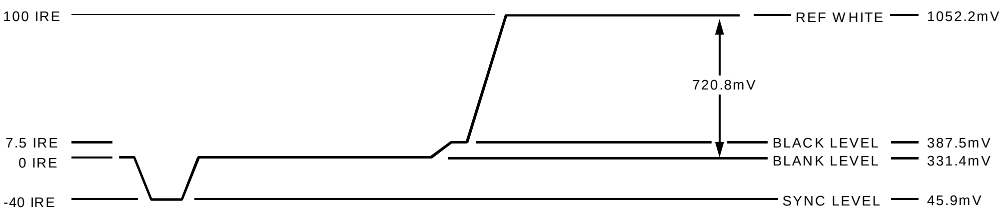


Figure 110. NTSC RGB Video Levels

NTSC WAVEFORMS (WITHOUT PEDESTAL)

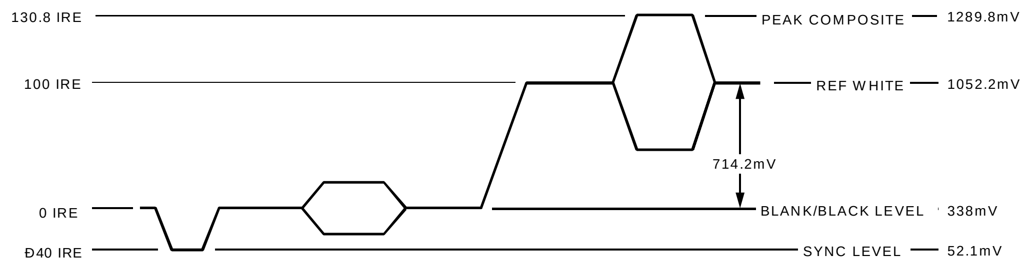


Figure 111. NTSC Composite Video Levels

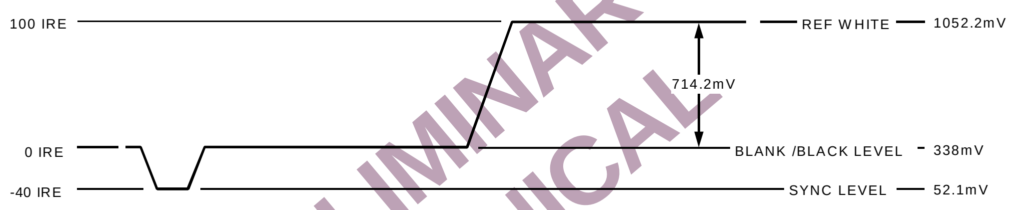


Figure 112. NTSC Luma Video Levels

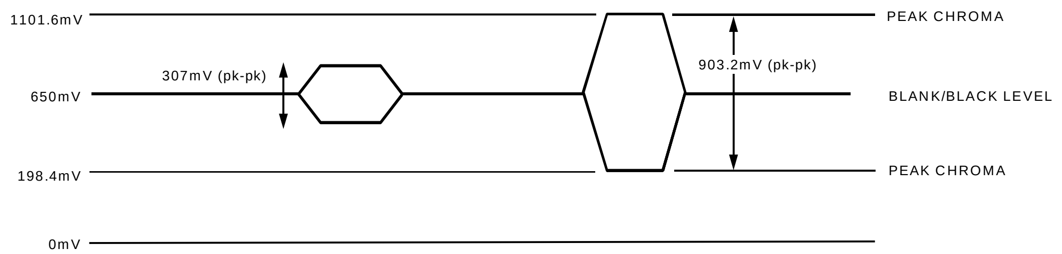


Figure 113. NTSC Chroma Video Levels

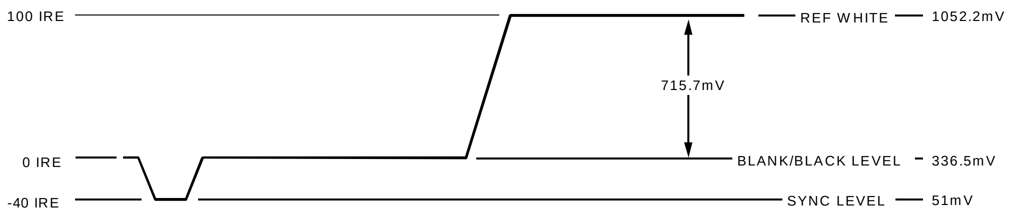


Figure 114. NTSC RGB Video Levels

PAL WAVEFORMS

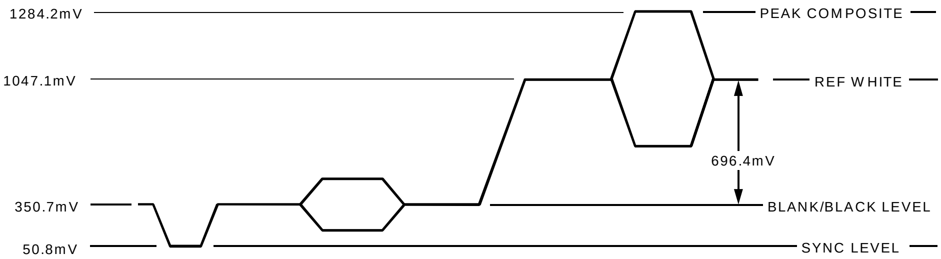


Figure 115. PAL Composite Video Levels

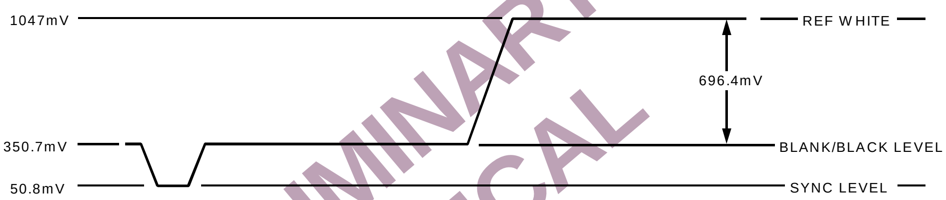


Figure 116. PAL Luma Video Levels

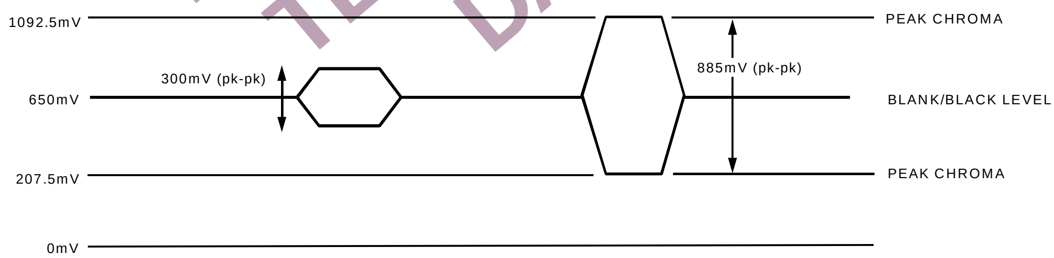


Figure 117. PAL Chroma Video Levels

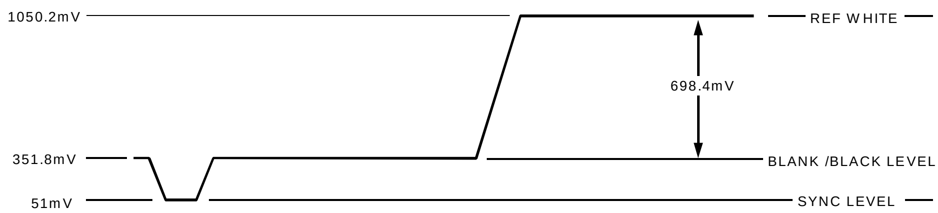


Figure 118. PAL RGB Video Levels

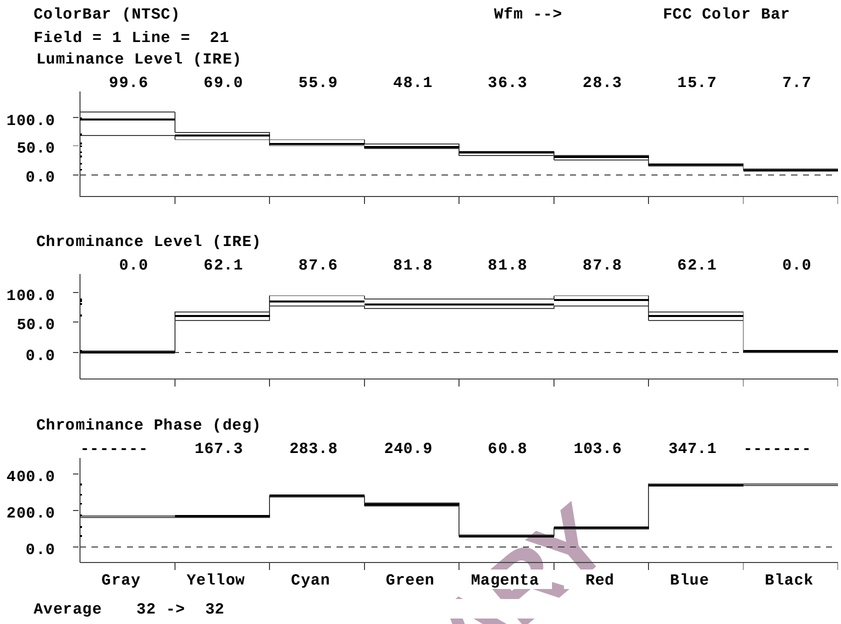


Figure 119. NTSC Color Bars Measurement

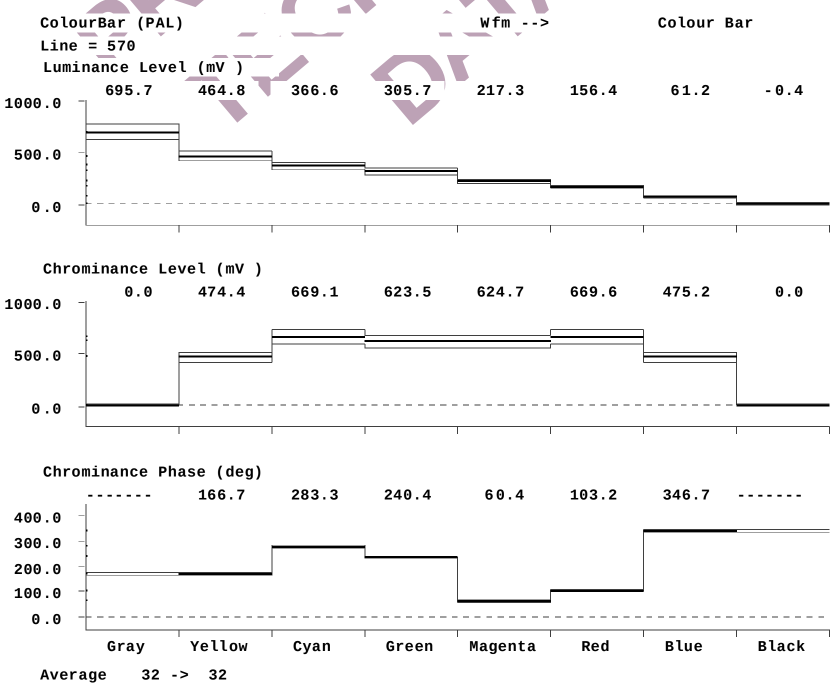


Figure 120. PAL Color Bars Measurement

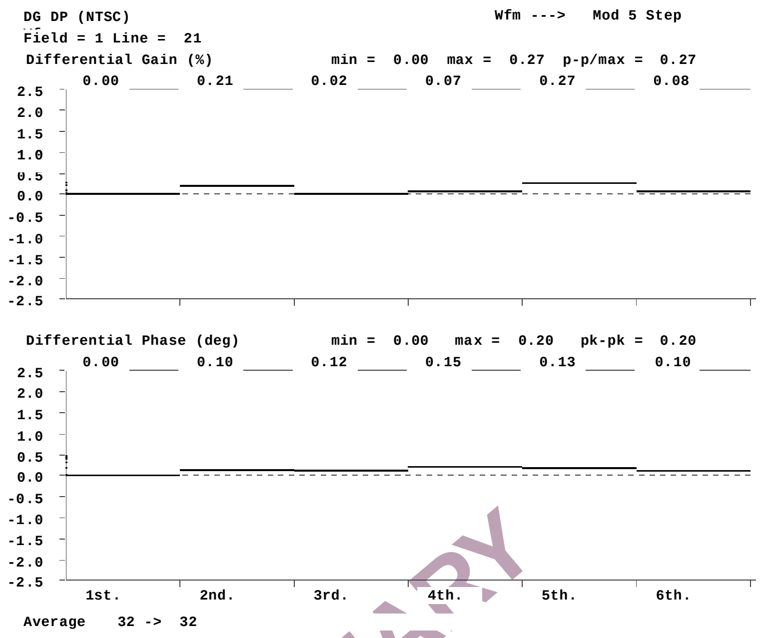


Figure 121. NTSC Differential Gain and Phase Measurement

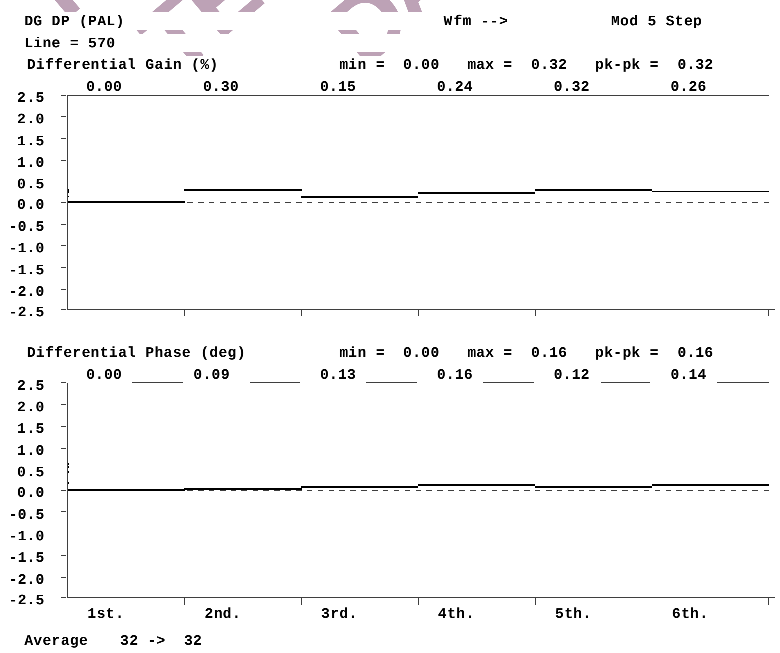


Figure 122. PAL Differential Gain and Phase Measurement

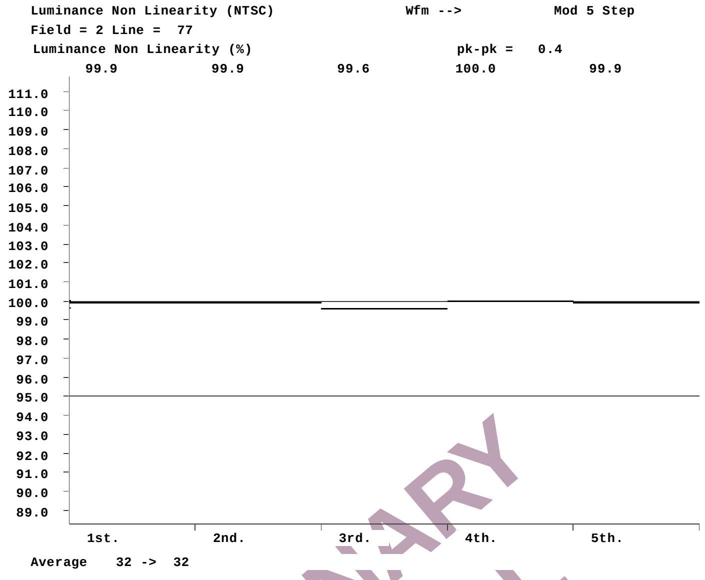


Figure 123. NTSC Luminance Non-Linearity

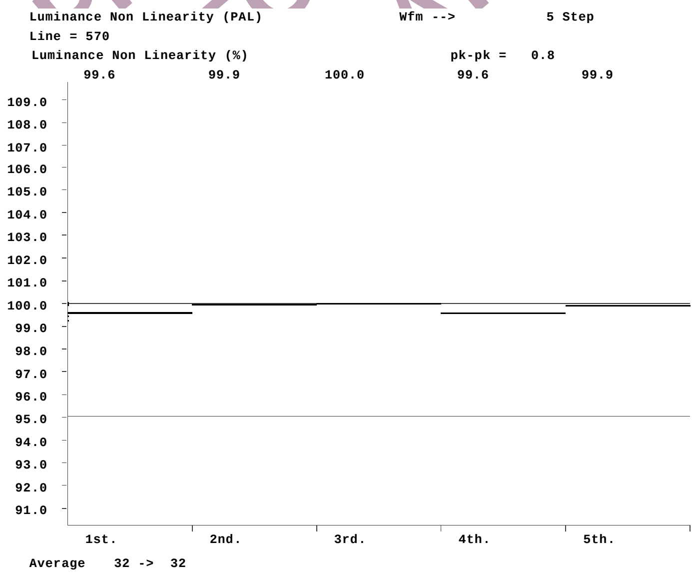


Figure 124. PAL Luminance Non-Linearity

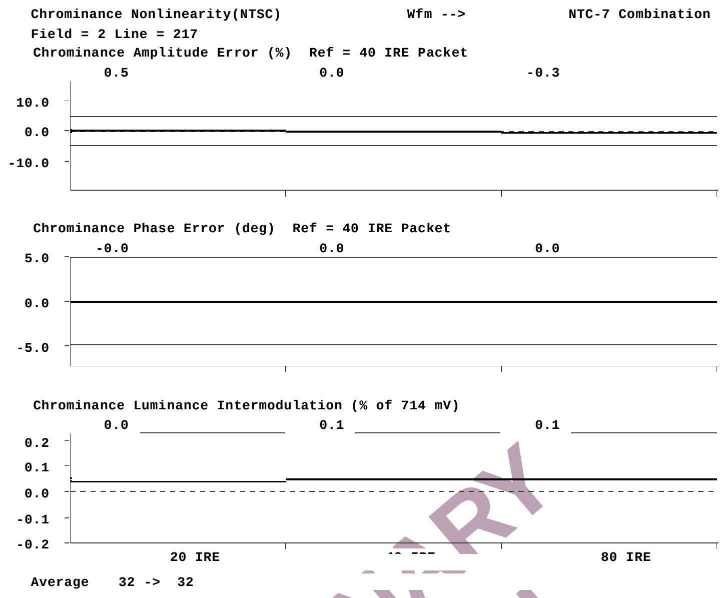


Figure 125. NTSC Chrominance Non-Linearity

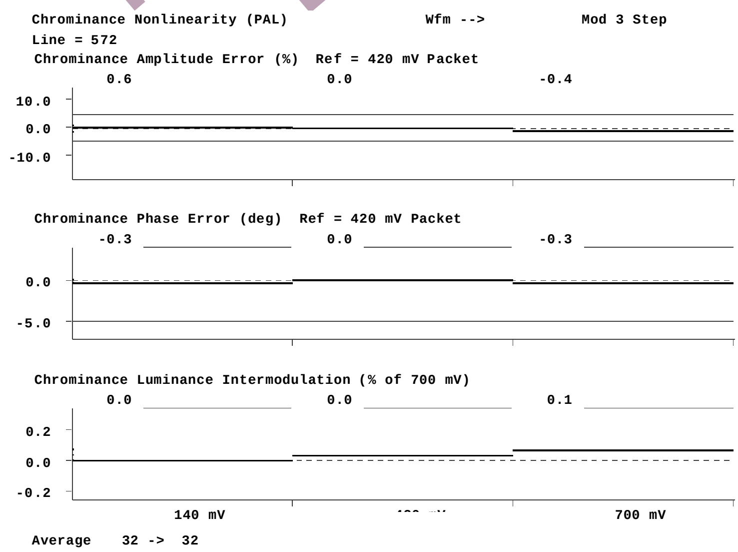


Figure 126. PAL Chrominance Non-Linearity

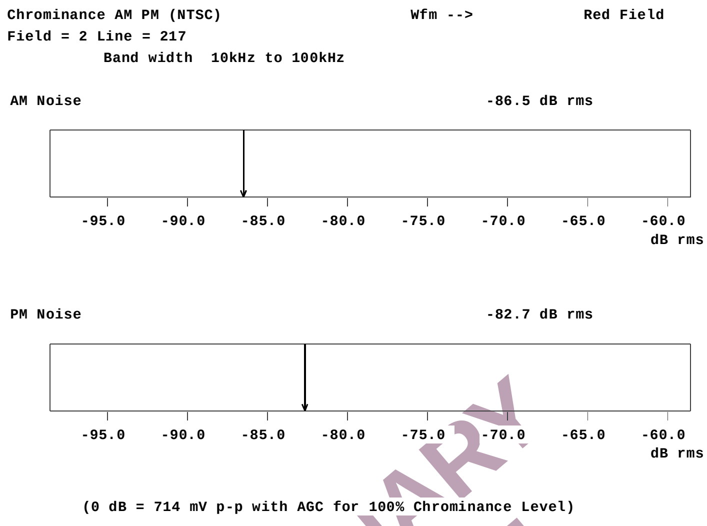


Figure 127. NTSC Chrominance AMPM

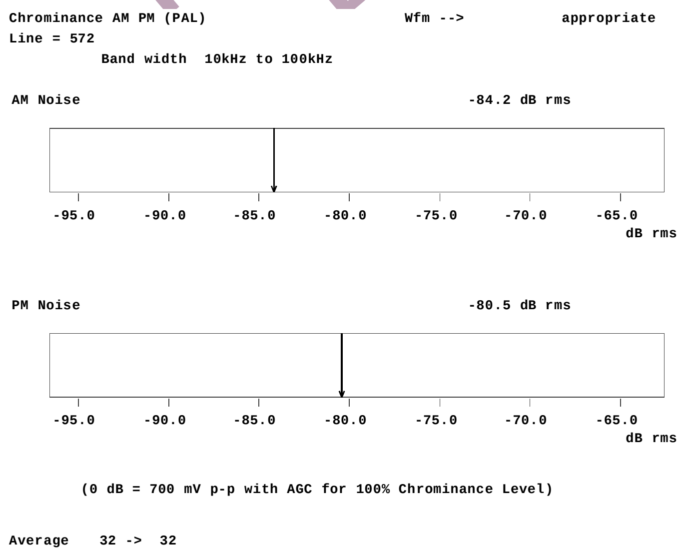


Figure 128. PAL Chrominance AMPM

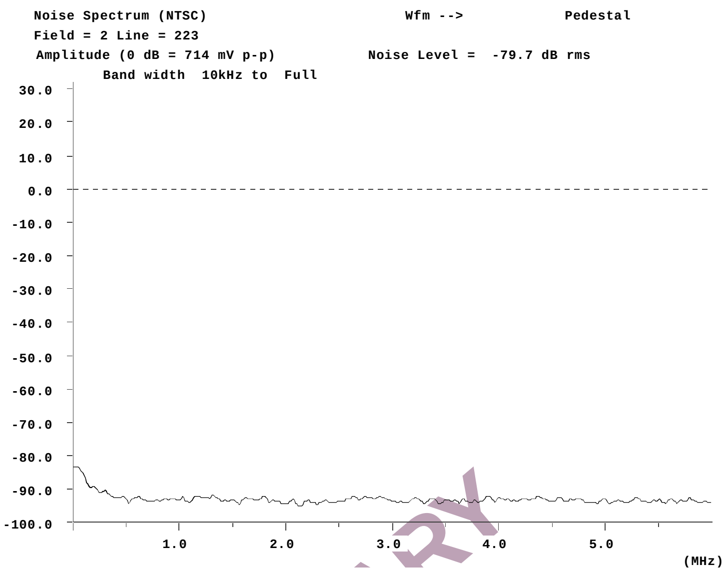


Figure 129. NTSC Noise Spectrum - Pedestal

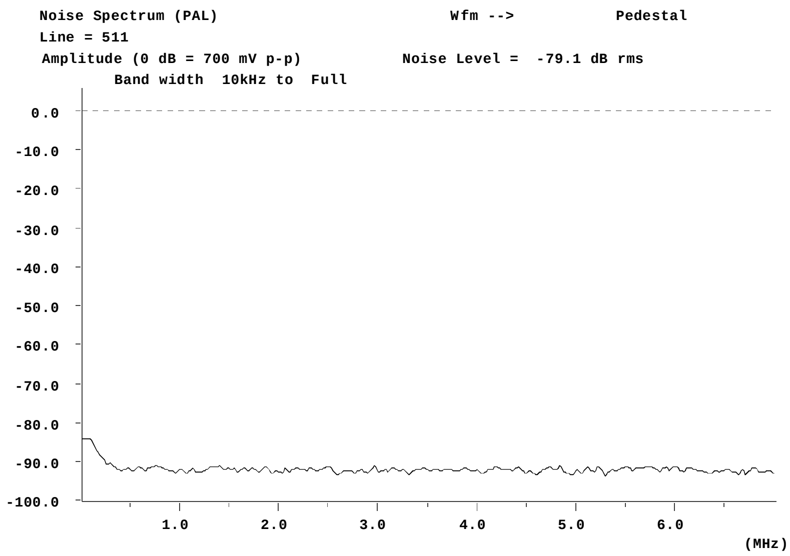


Figure 130. PAL Noise Spectrum - Pedestal

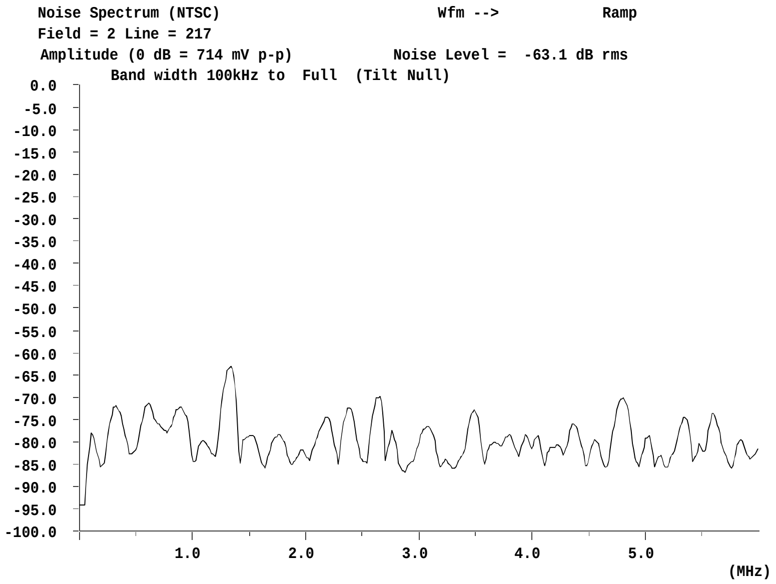


Figure 131. NTSC Noise Spectrum - Ramp

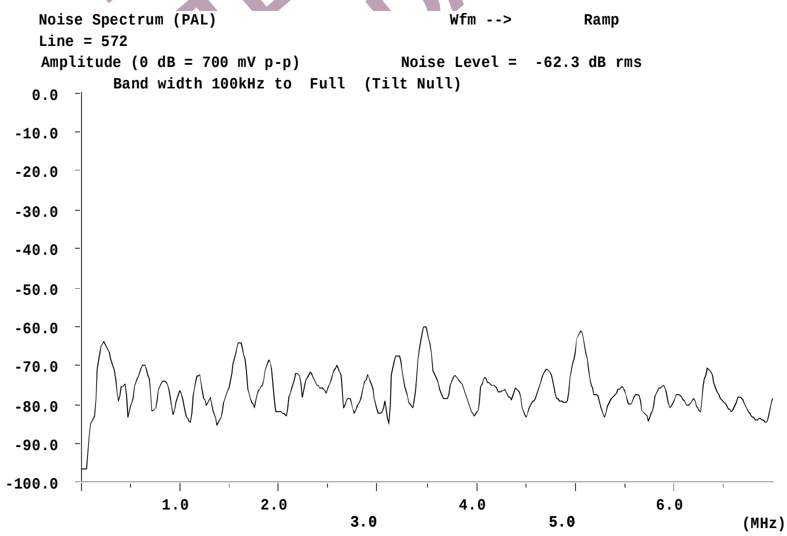


Figure 132. PAL Noise Spectrym - Ramp

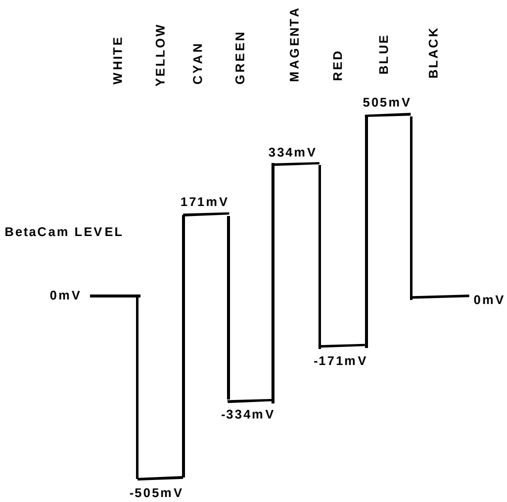


Figure 133. NTSC 100% Color Bars No Pedestal U Levels

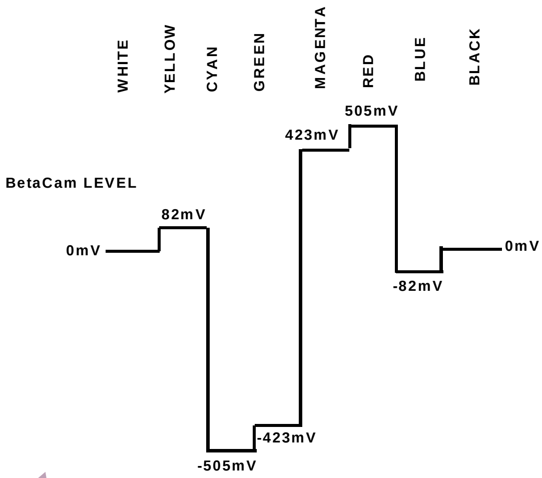


Figure 134. NTSC 100% Color Bars No Pedestal V Levels

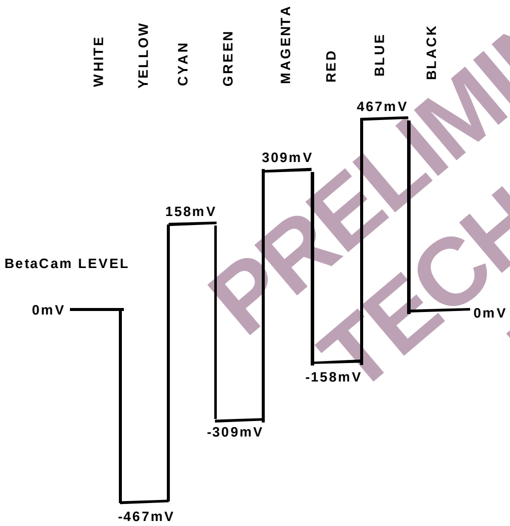


Figure 135. NTSC 100% Color Bars with Pedestal U Levels

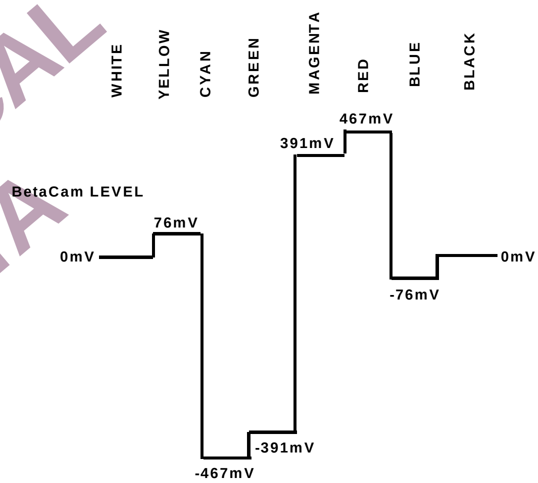


Figure 136. NTSC 100% Color Bars with Pedestal V Levels

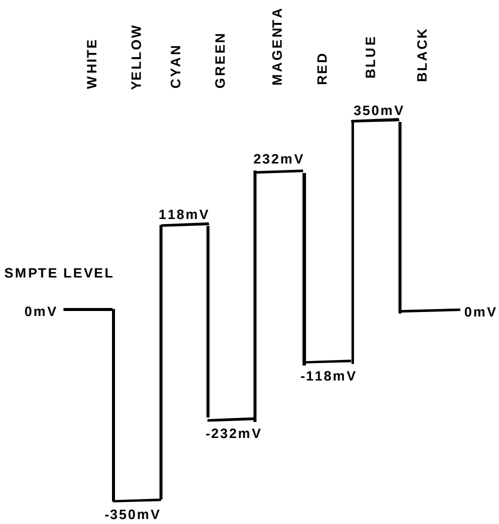


Figure 137. PAL 100% Color Bars U Levels

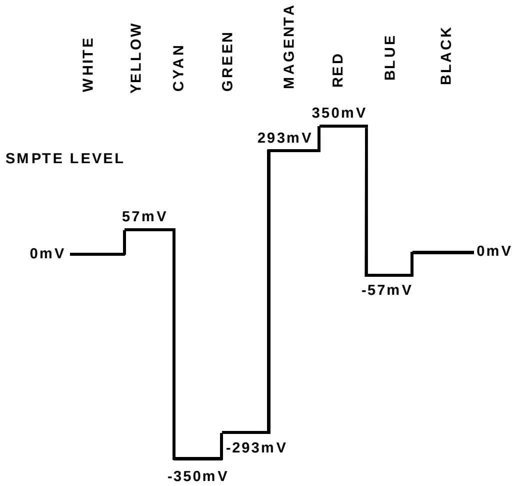


Figure 138-. PAL 100% Color Bars V Levels

OUTPUT WAVEFORMS

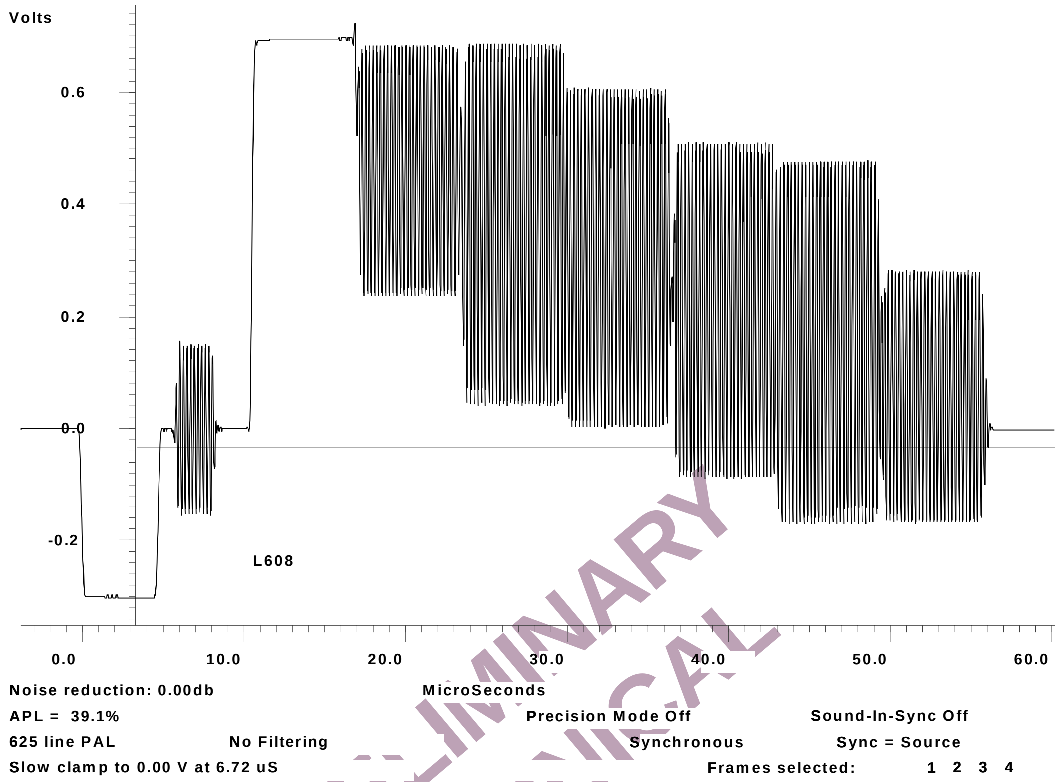


Figure 139.100/75% PAL Color Bars

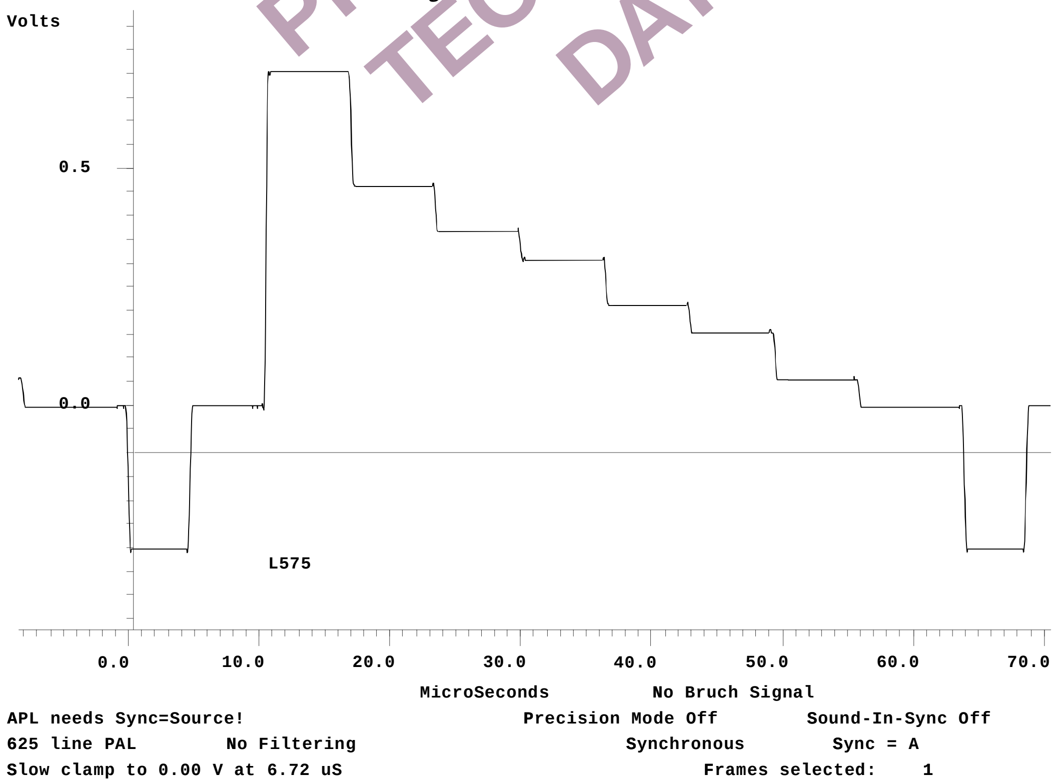


Figure 140. 100/75% PAL Color Bars Luminance

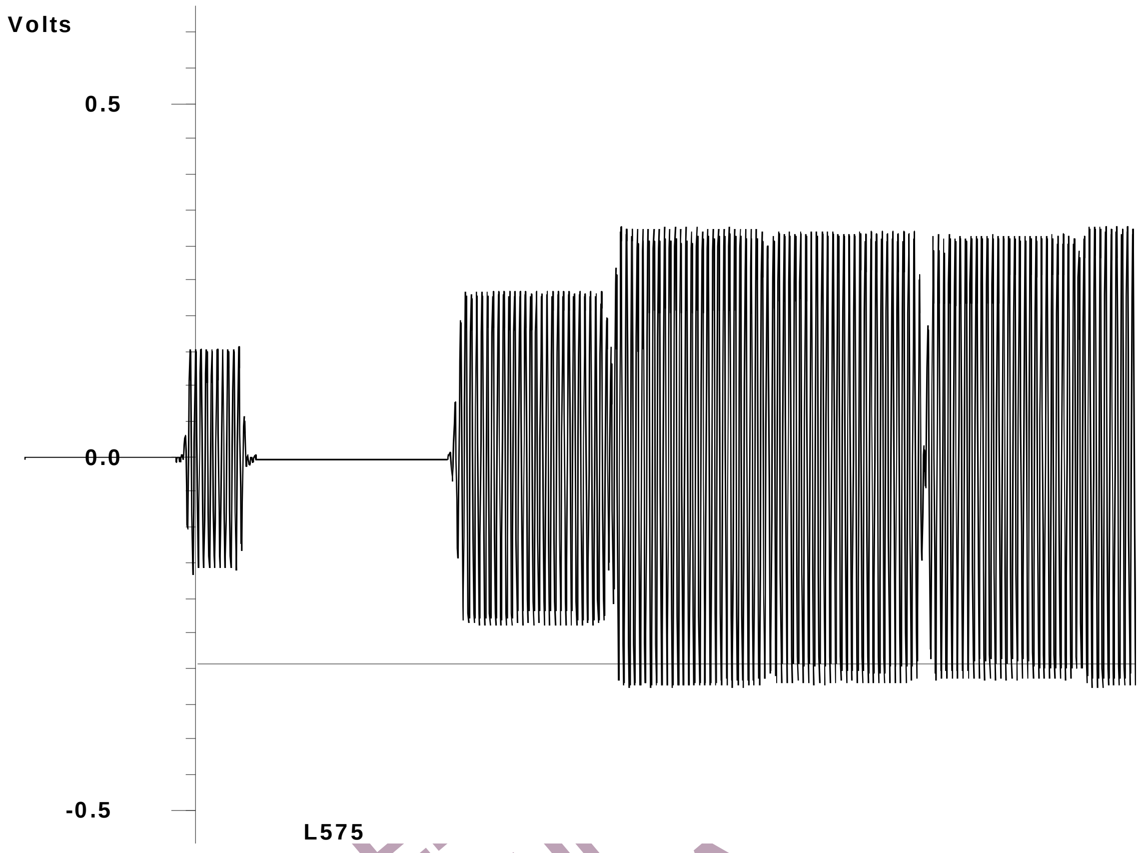


Figure 141 100/75% PAL Color Bars Chrominance

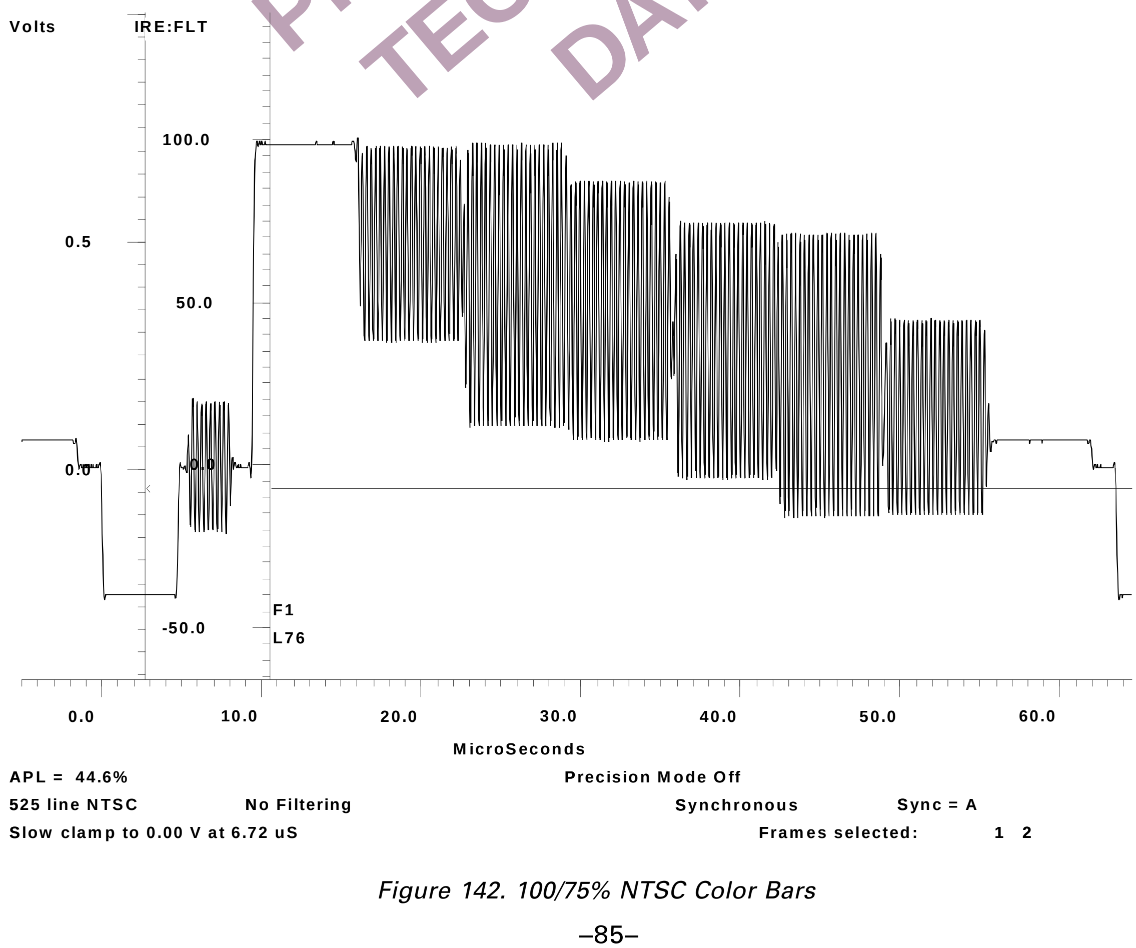


Figure 142. 100/75% NTSC Color Bars

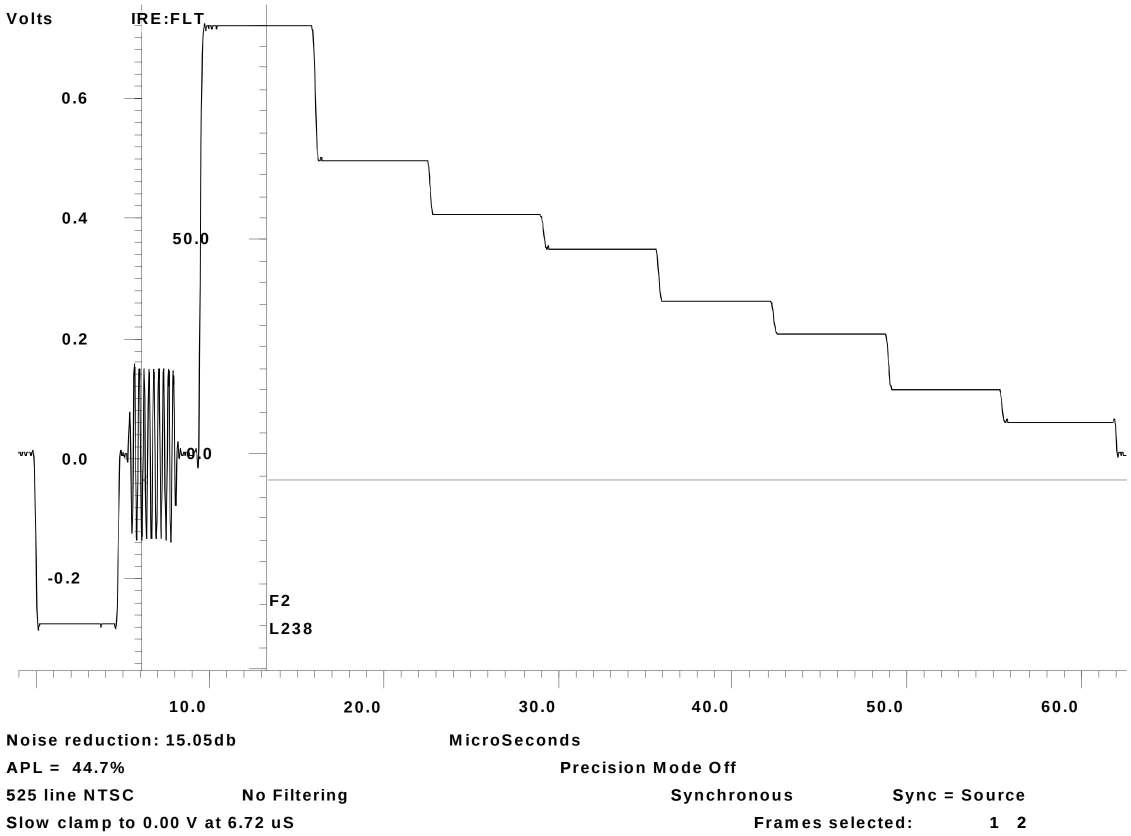


Figure 143. 100/75% NTSC Color Bars Luminance

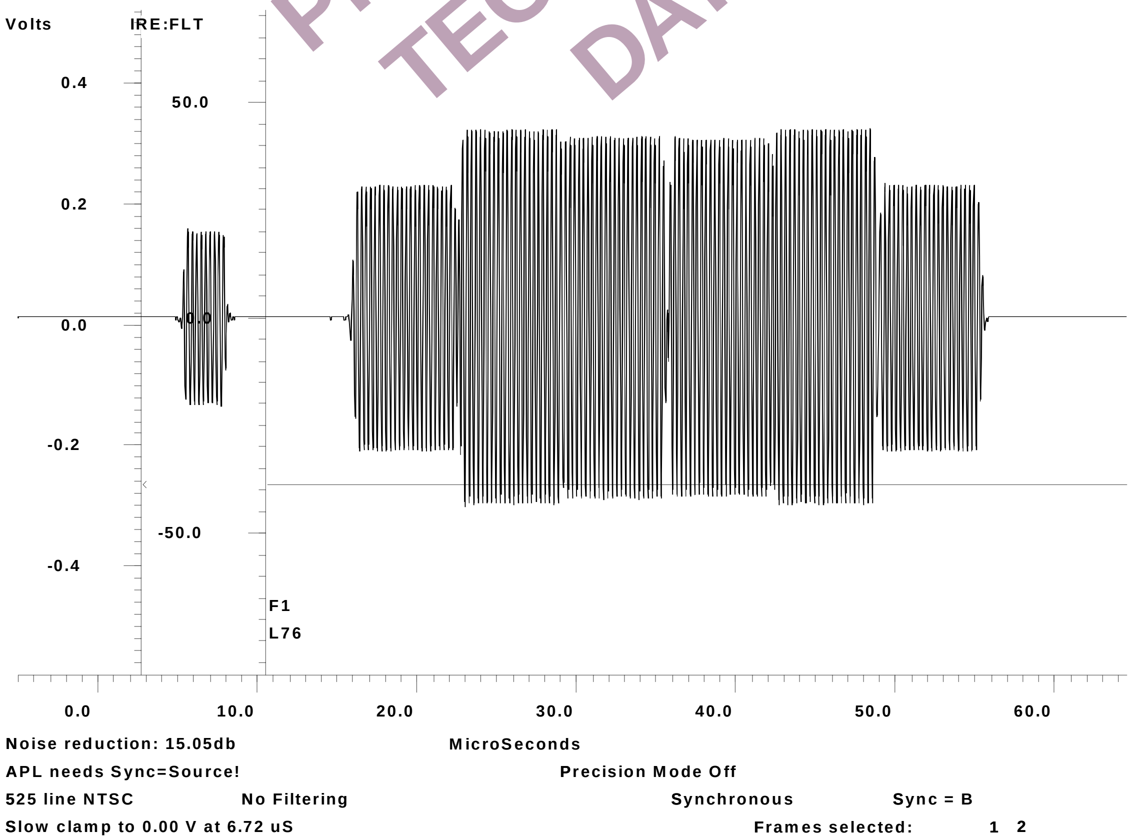


Figure 144.100/75% NTSC Color Bars Chrominance

APPENDIX 10

VECTOR PLOTS

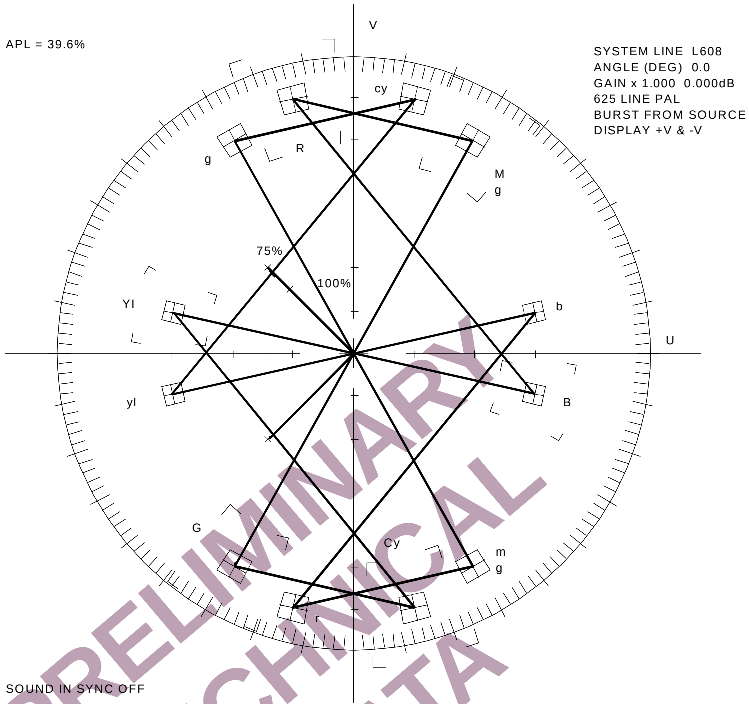


Figure 145. PAL Vector Plot

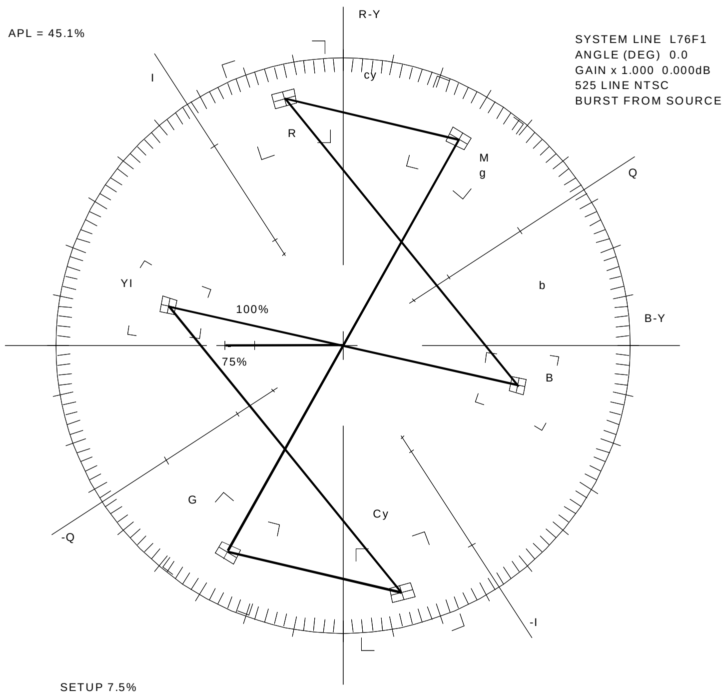


Figure 146. NTSC Vector Plot

APPENDIX 11

PACKAGE OUTLINE DIMENSIONS

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

80-Lead LQFP
(ST-80)