

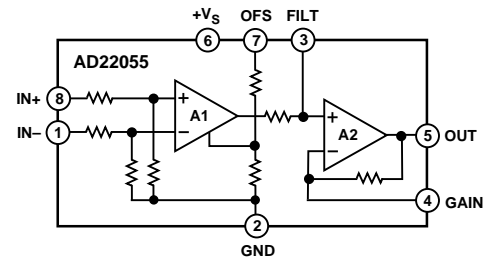
FEATURES

- Gain of 400. Alterable from 40 to 1000
- Output Span 20 mV to ($V_S - 0.25$) V
- 1 Pole Low-Pass Filtering Available
- Offset Capability
- Differential Input Resistance 230 k Ω
- Drives 1 k Ω Load to +4 V Using $V_S = +5$ V
- Supply Voltage: +3 V to +36 V
- Transient Spike Protection and RFI Filters Included
- Peak Input Voltage (40 ms): 60 V
- Reversed Supply Protection: -34 V
- Operating Temperature Range: -40°C to +125°C

APPLICATIONS

- Interface for Pressure Transducers, Position Indicator, Strain Gages, and Other Low Level Signal Sources

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD22055 accepts a differential signal from a bridge transducer whose common-mode signal can be anywhere between the power supplies.

The extended temperature range allows for local signal conditioning for oil and hydraulic pressure sensors as well as other automotive sensors.

*Patents pending.

The use of an external gain resistor allows the user to compensate transducer gain error and temperature drift.

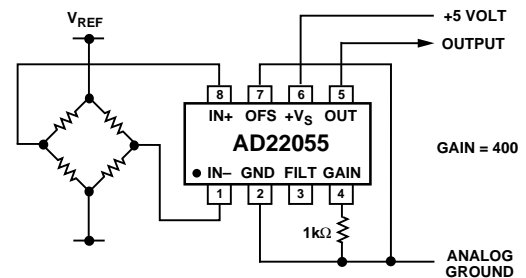


Figure 1. Typical Application Circuit for a Pressure Sensor Interface

REV. 0

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

© Analog Devices, Inc., 1995

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD22055—SPECIFICATIONS (@ $T_A = +25^\circ\text{C}$, $V_S = +5\text{ V}$, $V_{CM} = 0$, unless otherwise noted)

Parameter	Comments	Test Conditions	Min	Typ	Max	Units
INPUTS (PINS 1 AND 8)						
V_{CM}	Common-Mode Range		0		5	V
$CMRR_{LF}$	Common-Mode Rejection Ratio	$f \leq 10\text{ Hz}$	-80	-90		dB
$CMRR_{HF}$	Common-Mode Rejection Ratio	$f = 10\text{ kHz}$	-60	-75		dB
R_{INCM}	Common-Mode Input Resistance	Pin 1 or Pin 8 to Pin 2	180	230		k Ω
R_{MATCH}	Matching of Input Resistances			± 05		%
R_{INDIFF}	Differential Input Resistance	Pin 1 to Pin 8	180	230	300	k Ω
PREAMPLIFIER						
G_{CL}	Closed-Loop Gain ¹			40		V/V
V_O	Output Voltage Range (Pin 3)		+0.02		+4.75	V
R_O	Output Resistance ²		77.6	80	82.4	k Ω
OUTPUT BUFFER						
G_{CL}	Closed-Loop Gain ¹	$R_{LOAD} \geq 10\text{ k}\Omega$	9.95	10	10.05	V/V
V_O	Output Voltage Range		+0.02		+4.75	V
R_O	Output Resistance (Pin 5)	$V_O \geq 0.1\text{ V dc}$		2.0		Ω
OVERALL SYSTEM						
G_{CL}	Gain ¹	$V_O \geq 0.1\text{ V dc}$	398	400	402	V/V
	Gain Drift	$-40^\circ\text{C to } +125^\circ\text{C}$		-60		ppm/ $^\circ\text{C}$
	Gain Drift	$-125^\circ\text{C to } +150^\circ\text{C}$		-500		ppm/ $^\circ\text{C}$
V_{OS}	Initial Offset Voltage ³		-1	0.05	1	mV
	Offset Drift	$-40^\circ\text{C to } +125^\circ\text{C}$		1		$\mu\text{V}/^\circ\text{C}$
	Offset Drift	$-125^\circ\text{C to } +150^\circ\text{C}$		-10		$\mu\text{V}/^\circ\text{C}$
	Input Resistance	Pin 7 to Pin 2	2.5	3.0		k Ω
I_{OSC}	Short-Circuit Output Current		7	11	25	mA
$BW_{-3\text{ dB}}$	-3 dB Bandwidth	$V_O = +1\text{ V dc}$	20	30		kHz
SR	Slew Rate			0.2		V/ μs
N_{SD}	Noise Spectral Density ³	$f = 100\text{ Hz to } 10\text{ kHz}$		0.2		$\mu\text{V}/\sqrt{\text{Hz}}$
POWER SUPPLY						
V_S	Operating Range	$T_A = T_{MIN} \text{ to } T_{MAX}$	3	5	36	V
I_S	Quiescent Supply Current ⁴			200	500	μA
TEMPERATURE RANGE						
T_{OP}	Operating Temperature Range		-40		+125	$^\circ\text{C}$
PACKAGE	Plastic SOIC (R-8)			AD22055R		

NOTES

¹A2 gain is trimmed to $\pm 0.5\%$ with a 0.01% 1 k Ω resistor to ground from Pin 4. The overall gain is trimmed to a gain of $400 \pm 0.5\%$ with the same 1 k Ω resistor. The gain of A1 (the ratio of overall gain to A2 gain) is used to adjust the overall gain and, therefore, is not trimmed explicitly to 40. Note that the actual gain to a particular application can be modified by the use of an external resistor at Pin 4.

²The actual output resistance of A1 is only a few ohms, but access to this output, via Pin 3, is always through an 80 k Ω resistor, which is trimmed to $\pm 3\%$.

³Referred to the input (Pins 1 and 8).

⁴With $V_{DM} = 0\text{ V}$. Differential mode signals are referred to as V_{DM} , while V_{CM} refers to common-mode voltages.

All min and max specifications are guaranteed, although only those marked in **boldface** are tested on all production units at final test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

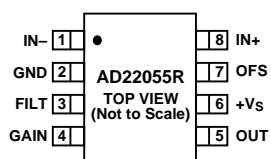
Supply Voltage	+3 V to +36 V
Peak Input Voltage (40 ms)	60 V
Reversed Continuous Supply Voltage	-34 V
Operating Temperature	-40°C to +125°C
Storage Temperature	-65°C to +150°C
Output Short Circuit Duration	Indefinite
Lead Temperature (Soldering, 60 sec)	+300°C

¹Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD22055R	-40°C to +125°C	Plastic SOIC	R-8

PIN CONNECTION



PIN DESCRIPTION

8-Pin SOIC	
Pin	Function
1	IN-
2	Ground
3	Filter
4	Gain
5	Out
6	Out
6	+V _S
7	OFS
8	IN+

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD22057 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PRODUCT DESCRIPTION

The AD22055 is a single supply difference amplifier consisting of a precision balanced attenuator, a very low drift preamplifier and an output buffer amplifier (A1 and A2, respectively in the functional block diagram). It has been designed so that small differential signals V_{DM} can be accurately amplified and filtered in the presence of large common-mode voltages V_{CM} without the use of any other active components.

The common-mode range resistors in this network are trimmed to match better than one part in 10,000. The resistive attenuator network is situated at the input to the AD22055 (Pins 1 and 8) allowing the common-mode voltage at Pins 1 and 8 to be two times greater than that which can be tolerated by the actual input of A1. As a result, the input common-mode range extends from ground to the power supply voltage.

Two small filter capacitors (not shown) have been included at the inputs to A1 to minimize the effects of any spurious RF signals present in the signal.

Internal feedback around A1 sets the closed-loop gain of the preamplifier to 40 V/V from the input pins, and the output of A1 is connected to Pin 3 via a 80 kΩ resistor which is trimmed to ±3%, to facilitate the low-pass filtering of the signal. The output buffer A2 has a gain of 10 V/V (using a precise 1 kΩ resistor from Pin 4 to ground) setting the precalibrated, overall gain of the AD22055, to 400 mV. This gain is easily user-configurable.

Overall gain is programmed using the following equation:

$$Gain = 40 \left(1 + \frac{9 \text{ k}\Omega}{R_{GAIN}} \right) V/V \quad (1)$$

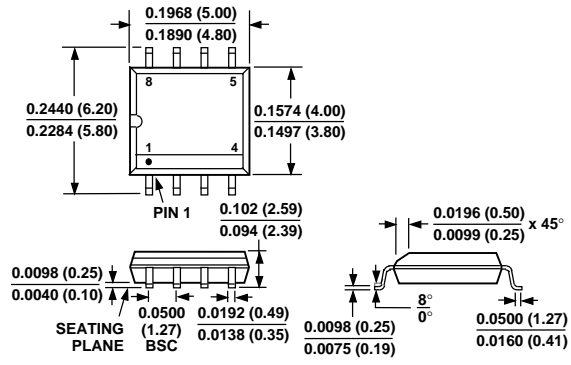
The dynamic properties of the AD22055 are optimized for interfacing to transducers, in particular those with a Wheatstone Bridge configuration. Its rejection of large, high frequency, common-mode signals makes it superior to that of many alternative approaches. This is due to the very careful design of the input attenuator and the dose integration of this highly balanced, high impedance system with the preamplifier.



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic SOIC Package (R-8)



000000000

PRINTED IN U.S.A.