ANALOG DEVICES

Monolithic 16-Bit Serial/Byte DACPORT

SMD/883B AD660

Scope

This specification covers the detail requirement for a complete, monolithic 16-bit digital-to-analog converter (DACPORT®) with an on-board reference, output amplifier and double buffered latches. The electrical specifications match the Standard Military Drawing (SMD) 5962-94633 in effect at the release of this data sheet. For a copy of the latest official SMD, contact DESC-ELDS.

Part Number/Case Outline

For case outline dimensions, see Package Information Appendix of General Specification ADI-M-1000. The complete part numbers of these SMD and 883 devices are as follows:

Device Type	SMD Part Number	ADI 883 Part Number	Package Description	Package Designation ADI	Package Designation MIL-STD-1835
01	5962-9463301MLA	AD660SQ/883B	24-Pin Cerdip	Q-24	GDIP3-T24

Absolute Maximum Ratings.[1] (T_A = +25°C unless otherwise noted)

V_{LL} to DGND ..... −0.3 V to +7 V
V_{CC} to AGND ..... −0.3 V to +17.0 V
V_{EE} to AGND ..... +0.3 V to −17.0 V
AGND to DGND ..... ±1 V
Digital Inputs (Pins 5–12 and 14–19) to DGND ..... −1.0 V to +7.0 V
REF IN to AGND ..... ±10.5 V
Span/Bipolar Offset to AGND ..... +10.5 V
Ref Out, V_{OUT} ..... Indefinite Short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation
  To +60°C ..... 1000 mW
  Derates above +60°C ..... 8.7 mW/°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Recommended Operating Conditions

V_{LL} max ..... +5 V
V_{CC}/V_{EE} ..... ±15 V
Ambient Temperature Range ..... −55°C to +125°C

Thermal Characteristics

Thermal Resistance, Junction-to-Case (θ_{JC}) max ..... 28°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA}) max ..... 80°C/W

DACPORT is a registered trademark of Analog Devices, Inc.

NOTE
[1]Permanent damage may occur if any absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher-than-recommneded voltages for extended periods of time.

REV. B

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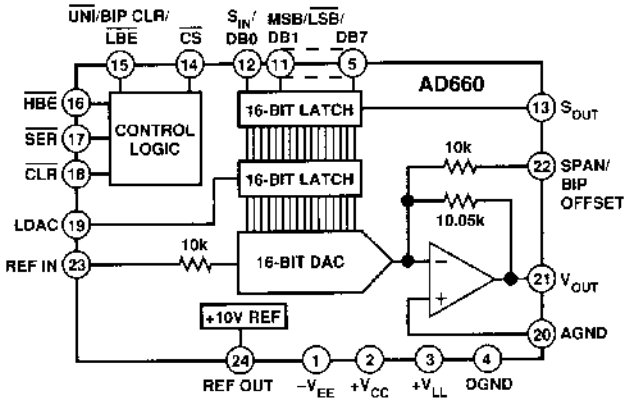
AD660—SPECIFICATIONS

Table I. Electrical Performance Characteristics

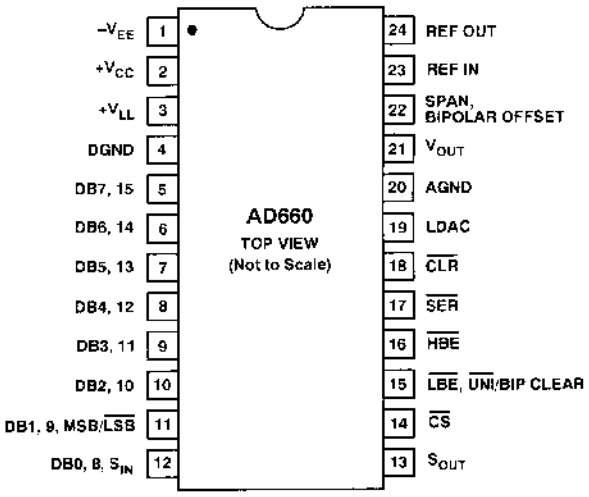
Test	Symbol	Conditions[1] V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V unless otherwise specified	Group A Subgroup	Device Type	Limits Min	Limits Max	Units
Resolution[2]	RES		1	01	16		Bits
Relative Accuracy	RA		1	01		2	±LSB
			2, 3			4	
Differential Nonlinearity	DNL	Major Carry Errors	1	01		2	±LSB
			2, 3			4	
Gain Error[3, 4]	A_E	All Bits On	1	01		0.10	±% of FSR
Gain Drift[3]	TCA_E	All Bits On	2, 3	01		25	ppm/°C
Unipolar Offset Error	V_{OS}	All Bits Off	1	01		2.5	±mV
Unipolar Offset Tempco	TCV_{OS}	All Bits Off	2, 3	01		3	ppm/°C
Bipolar Zero Error	B_{PZE}	MSB On, All Others Off	1	01		7.5	±mV
Bipolar Zero Tempco	TCB_{PZE}	MSB On, All Others Off	2, 3	01		5	ppm/°C
Reference Output Voltage	V_{REF}		1	01	9.99	10.01	V
Reference Output Drift	TCV_{REF}		2, 3	01		25	ppm/°C
Reference Output External Current[2, 5]	IV_{REF}		1	01	2		mA
Reference Output Capacitive Load[2]	CLV_{REF}		1	01		1000	pF
Reference Input Resistance[2]	R_{IN}		1	01	7	13	kΩ
Bipolar Offset Input Resistance[2]	$R_{IN}BPO$		1	01	7	13	kΩ
Output Voltage Range[2]	V_{OUT}	Unipolar Range	1	01	0	+10	V
		Bipolar Range			−10	+10	
Output Current[2]	I_{OUT}		1	01	5		mA
Capacitive Load[2]	C_L		1	01		1000	pF
Output Voltage Settling Time	t_{SL}	20 V Step, T_A = +25°C[2]	1	01		13	µs
		20 V Step, T_A = −55°C, +125°C	—		10 typ		
		10 V Step, T_A = +25°C	—		6 typ		
		10 V Step, T_A = −55°C, +125°C	—		8 typ		
		LSB Step, T_A = −55°C, +125°C, +25°C	—		2.5 typ		
Digital Input High Voltage	V_{IH}		1, 2, 3	01	2		V
Digital Input Low Voltage	V_{IL}		1, 2, 3	01		0.8	V
Digital Input High Current	I_{IH}	V_{IH} = +5.5 V	1, 2, 3	01		10	±µA
Digital Input Low Current	I_{IL}	V_{IL} = 0 V	1, 2, 3	01		10	±µA
Power Supply Current	I_{LL}	V_{IH} = +5.5 V, V_{IL} = 0.0	1	01		2	mA
		V_{IH} = 2.4, V_{IL} = 0.4				7.5	
	I_{CC}					18	
	I_{EE}					−18	
Power Supply Rejection Ratio	PSRR	−14.25 V ≥ V_{CC} ≥ +15.75 V	1	01		2	±ppm/%
		−14.25 V ≥ V_{EE} ≥ −15.75 V				2	
		−4.5 V ≥ V_{LL} ≥ +5.5 V				2	
Total Harmonic Distortion + Noise	THD+N	0 dB, 990.5 Hz; Sample Rate = 96 kHz −20 dB, 990.5 Hz; Sample Rate= 96 kHz −60 dB, 990.5 Hz; Sample Rate = 96 kHz	1	01		0.009 0.056 5.6	%
Signal-to-Noise Ratio	SNR		1	01	83		dB

NOTES
[1]For 16-bit resolution, 1 LSB = 0.0015% or FSR = 15 ppm of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR = 30 ppm of FSR. For 14-bit resolution 1 LSB = 0.006% of FSR = 60 ppm of FSR. FSR stands for Full-Scale Range and is 10 V in Unipolar Mode and 20 V in Bipolar Mode.
[2]Guaranteed, not tested parameter.
[3]Gain error and gain drift are measured using the internal reference.
[4]Measured with fixed 50 Ω resistors. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar Mode) or 0.50% of FSR (Bipolar Mode).
[5]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET.

Functional Block Diagram and Terminal Assignments



Q-24 Package

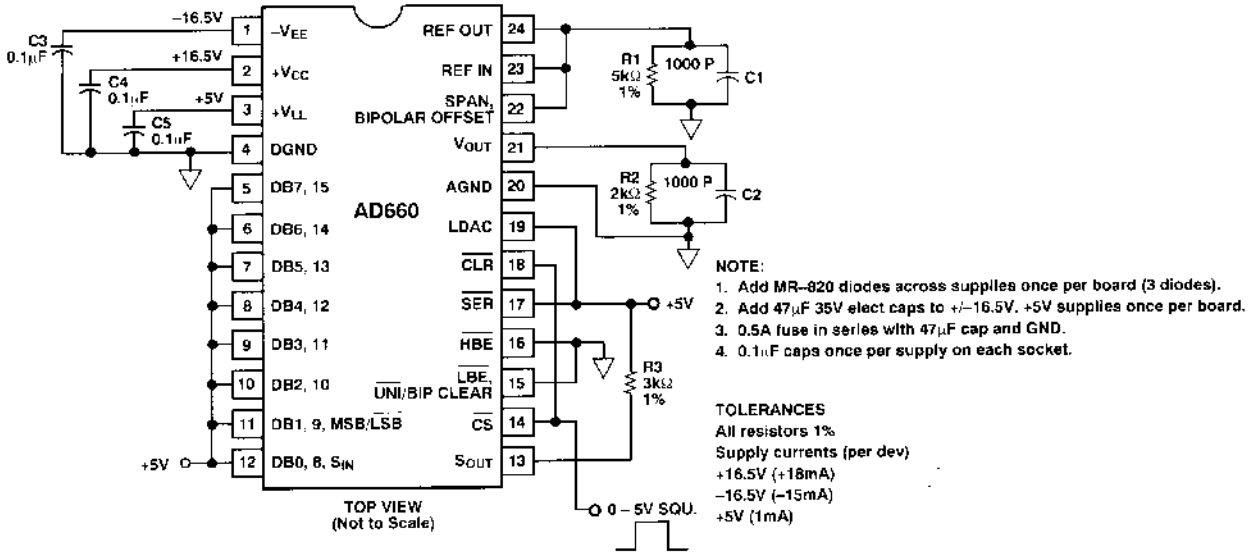


Microcircuit Technology Group

This microcircuit is covered by technology group (56).

Life Test/Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



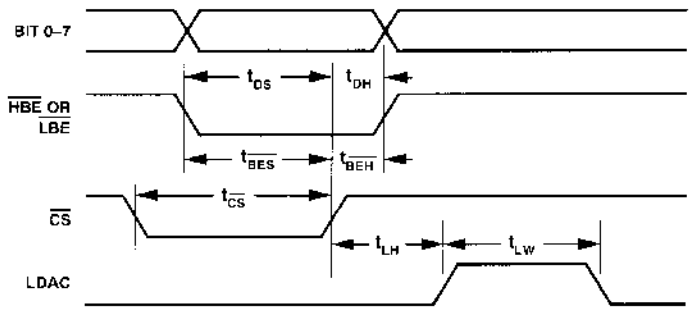


Figure 1a. AD660 Byte Load Timing

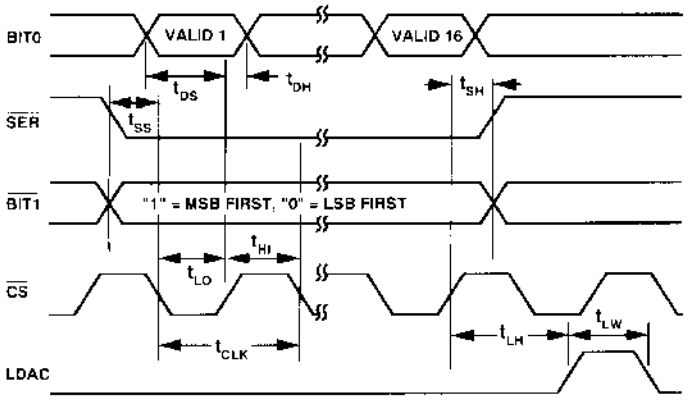


Figure 1b. AD660 Serial Load Timing

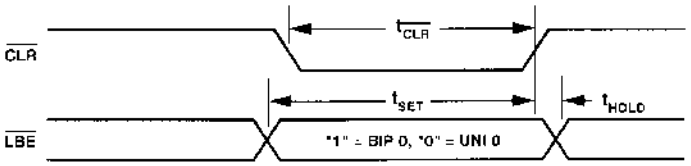


Figure 1c. Asynchronous Clear to Bipolar or Unipolar Zero

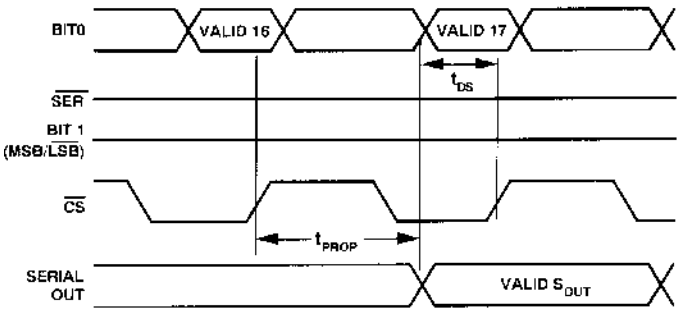


Figure 1d. Serial Out Timing

TIMING CHARACTERISTICS V_{CC} = +15 V, V_{EE} = −15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V, timing parameters are guaranteed not tested.

Parameter	Subgroup 9	Subgroups 10, 11	Units
(Figure 1a)			
$t_{\overline{CS}}$	40	50	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{BES}	40	50	ns min
t_{BEH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure 1b)			
t_{CLK}	80	100	ns min
t_{LO}	30	50	ns min
t_{HI}	30	50	ns min
t_{SS}	0	10	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{SH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure 1c)			
$t_{\overline{CLR}}$	80	110	ns min
t_{SET}	80	110	ns min
t_{HOLD}	0	10	ns min
(Figure 1d)			
t_{PROP}	50	100	ns min
t_{DS}	50	80	ns min

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