LC²MOS Quad 14-Bit DAC

AD7834/AD7835

FEATURES

Four 14-Bit DACs in One Package
- **AD7834—Serial Loading**
- **AD7835—Parallel 8-/14-Bit Loading**

Voltage Outputs
Power-On Reset Function
Max/Min Output Voltage Range of +/–8.192 V
Maximum Output Voltage Span of 14 V
Common Voltage Reference Inputs
User Assigned Device Addressing
Clear Function to User-Defined Voltage
Surface Mount Packages
- **AD7834—28-Pin SO, DIP and Cerdip**
- **AD7835—44-Pin PQFP and PLCC**

APPLICATIONS

Process Control
Automatic Test Equipment
General Purpose Instrumentation

GENERAL DESCRIPTION

The AD7834 and AD7835 contain four 14-bit DACs on one monolithic chip. The AD7834 and AD7835 have output voltages in the range of ±8.192 V with a maximum span of 14 V.

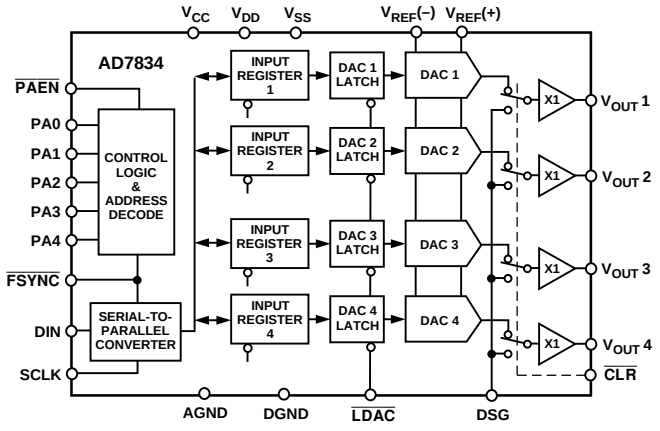
The AD7834 is a serial input device. Data is loaded in 16-bit format from the external serial bus, MSB first after two leading 0s, into one of the input latches via DIN, SCLK and $\overline{\text{FSYNC}}$. The AD7834 has five dedicated package address pins, PA0–PA4, that can be wired to AGND or V_{CC} to permit up to 32 AD7834s to be individually addressed in a multipackage application.

The AD7835 can accept either 14-bit parallel loading or double-byte loading, where right-justified data is loaded in one 8-bit and one 6-bit byte. Data is loaded from the external bus into one of the input latches under the control of the $\overline{\text{WR}}$, $\overline{\text{CS}}$, $\overline{\text{BYSHF}}$ and DAC channel address pins, A0–A2.

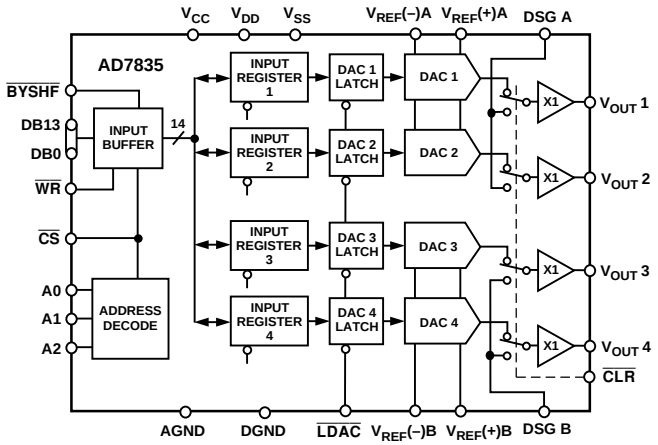
With either device, the $\overline{\text{LDAC}}$ signal can be used to update either all four DAC outputs simultaneously or individually, on reception of new data. In addition, for either device, the asynchronous $\overline{\text{CLR}}$ input can be used to set all signal outputs, $V_{OUT}1$–$V_{OUT}4$, to the user-defined voltage level on the Device Sense Ground pin, DSG. On power-on, before the power supplies have stabilized, internal circuitry holds the DAC output voltage levels to within ±2 V of the DSG potential. As the supplies stabilize, the DAC output levels move to the exact DSG potential (assuming $\overline{\text{CLR}}$ is exercised).

The AD7834 is available in 28-pin 0.3" SO and 0.6" DIP packages, and the AD7835 is available in a 44-pin PQFP package and a 44-pin PLCC package.

AD7834 FUNCTIONAL BLOCK DIAGRAM



AD7835 FUNCTIONAL BLOCK DIAGRAM



REV. A

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Tel: 617/329-4700 **Fax: 617/326-8703**

AD7834/AD7835–SPECIFICATIONS

(V_{CC} = +5 V ± 5%; V_{DD} = +15 V ± 5%; V_{SS} = –15 V ± 5%; AGND = DGND = 0 V; T_A[1] = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	A	B	S	Units	Test Conditions/Comments
ACCURACY					
Resolution	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	LSB max	Guaranteed Monotonic Over Temperature
Full-Scale Error					$V_{REF}(+)$ = +7 V, $V_{REF}(–)$ = –7 V
T_{MIN} to T_{MAX}	±5	±5	±8	mV max	
Zero-Scale Error	±4	±4	±5	mV max	$V_{REF}(+)$ = +7 V, $V_{REF}(–)$ = –7 V
Gain Error	±0.5	±0.5	±0.5	mV typ	$V_{REF}(+)$ = +7 V, $V_{REF}(–)$ = –7 V
Gain Temperature Coefficient[2]	4	4	4	ppm FSR/°C typ	
	20	20	20	ppm FSR/°C max	
DC Crosstalk[2]	50	50	50	µV max	See Terminology. R_L = 10 kΩ
REFERENCE INPUTS					
DC Input Resistance	30	30	30	MΩ typ	
Input Current	±1	±1	±1	µA max	Per Input
$V_{REF}(+)$ Range	0/+8.192	+7/+8.192	0/+8.192	V min/max	
$V_{REF}(–)$ Range	–8.192/0	–8.192/0	–8.192/0	V min/max	
$[V_{REF}(+)–V_{REF}(–)]$	5/14	7/14	5/14	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
DEVICE SENSE GROUND INPUTS					
Input Current	±2	±2	±2	µA max	Per Input. V_{DSG} = –2 V to +2 V
DIGITAL INPUTS					
V_{INH}, Input High Voltage	2.4	2.4	2.4	V min	
V_{INL}, Input Low Voltage	0.8	0.8	0.8	V max	
I_{INH}, Input Current	±10	±10	±10	µA max	
C_{IN}, Input Capacitance	10	10	10	pF max	
POWER REQUIREMENTS					
V_{CC}	5.0	5.0	5.0	V nom	±5% for Specified Performance
V_{DD}	15.0	15.0	15.0	V nom	±5% for Specified Performance
V_{SS}	–15.0	–15.0	–15.0	V nom	±5% for Specified Performance
Power Supply Sensitivity					
ΔFull Scale/ΔV_{DD}	110	110	110	dB typ	
ΔFull Scale/ΔV_{SS}	100	100	100	dB typ	
I_{CC}	0.2	0.2	0.5	mA max	V_{INH} = V_{CC}, V_{INL} = DGND
	3	3	3	mA max	AD7834. V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
	6	6	6	mA max	AD7835. V_{INH} = 2.4 V min, V_{INL} = 0.8 V max
I_{DD}	10	10	15	mA max	AD7834. Outputs Unloaded
	15	15	15	mA max	AD7835. Outputs Unloaded
I_{SS}	10	10	15	mA max	Outputs Unloaded

AC PERFORMANCE CHARACTERISTICS

(These characteristics are included for Design Guidance and are not subject to production testing.)

Parameter	A	B	S	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time	10	10	10	µs typ	Full-Scale Change to ±1/2 LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Digital-to-Analog Glitch Impulse	120	120	120	nV-s typ	Measured with $V_{REF}(+)$ = $V_{REF}(–)$ = 0 V. DAC Latch Alternately Loaded with All 0s and All 1s
DC Output Impedance	0.5	0.5	0.5	Ω typ	See Terminology
Channel-to-Channel Isolation	100	100	100	dB typ	See Terminology; Applies to the AD7835 Only
DAC to DAC Crosstalk	25	25	25	nV-s typ	See Terminology
Digital Crosstalk	3	3	3	nV-s typ	Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter
Digital Feedthrough – AD7834	0.2	0.2	0.2	nV-s typ	Effect of Input Bus Activity on DAC Output Under Test
– AD7834	0.1	0.1	0.1	nV-s typ	
Output Noise Spectral Density					
@ 1 kHz	40	40	40	nV/√Hz typ	All 1s Loaded to DAC. $V_{REF}(+)$ = $V_{REF}(–)$ = 0 V

NOTES

[1]Temperature range is as follows: A Version: –40°C to +85°C; B Version: –40°C to +85°C; S Version: –55°C to +125°C.

[2]Guaranteed by design.

Specifications subject to change without notice

TIMING SPECIFICATIONS[1] (V_{CC} = +5 V ± 5%; V_{DD} = +15 V ± 5%; V_{SS} = –15 V ± 5%; AGND = DGND = 0 V)

Parameter	Limit at T_{MIN}, T_{MAX}	Units	Description
AD7834 Specific			
t_1[2]	100	ns min	SCLK Cycle Time
t_2[2]	50	ns min	SCLK Low Time @ +25°C
	60	ns min	SCLK Low Time –40°C to +85°C
	66	ns min	SCLK Low Time –55°C to +125°C
t_3[2]	30	ns min	SCLK High Time
t_4	30	ns min	$\overline{\text{FSYNC}}$, $\overline{\text{PAEN}}$ Setup Time
t_5	40	ns min	$\overline{\text{FSYNC}}$, $\overline{\text{PAEN}}$ Hold Time
t_6	30	ns min	Data Setup Time
t_7	10	ns min	Data Hold Time
t_8	0	ns min	$\overline{\text{LDAC}}$ to $\overline{\text{FSYNC}}$ Setup Time
t_9	40	ns min	$\overline{\text{LDAC}}$ to $\overline{\text{FSYNC}}$ Hold Time
t_{21}	20	ns min	Delay Between Write Operations
AD7835 Specific			
t_{11}	15	ns min	A0, A1, A2, $\overline{\text{BYSHF}}$ to $\overline{\text{CS}}$ Setup Time
t_{12}	15	ns min	A0, A1, A2, $\overline{\text{BYSHF}}$ to $\overline{\text{CS}}$ Hold Time
t_{13}	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Setup Time
t_{14}	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Hold Time
t_{15}	40	ns min	$\overline{\text{WR}}$ Pulse Width
t_{16}	40	ns min	Data Setup Time
t_{17}	10	ns min	Data Hold Time
t_{18}	0	ns min	$\overline{\text{LDAC}}$ to $\overline{\text{CS}}$ Setup Time
t_{19}	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{LDAC}}$ Setup Time
t_{20}	0	ns min	$\overline{\text{LDAC}}$ to $\overline{\text{CS}}$ Hold Time
General			
t_{10}	40	ns min	$\overline{\text{LDAC}}$, $\overline{\text{CLR}}$ Pulse Width

NOTES
[1]All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[2]Rise and fall times should be no longer than 50 ns.
Specifications subject to change without notice.

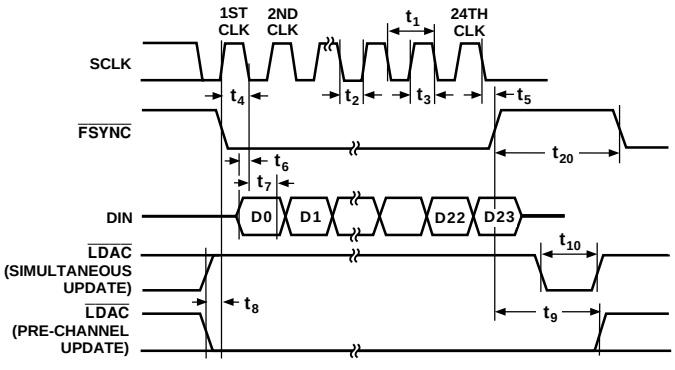


Figure 1. AD7834 Timing Diagram

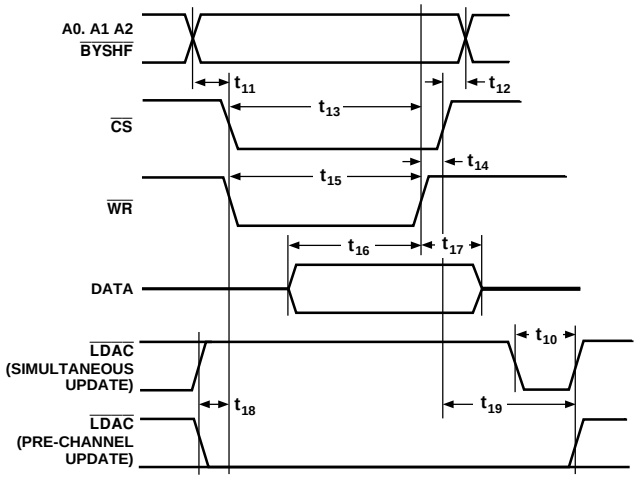


Figure 2. AD7835 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{CC} to DGND . . . . . –0.3 V, +7 V or V_{DD} + 0.3 V (Whichever Is Lower)
V_{DD} to AGND . . . . . –0.3 V, +17 V
V_{SS} to AGND . . . . . +0.3 V, –17 V
AGND to DGND . . . . . –0.3 V, +0.3 V
Digital Inputs to DGND . . . . . –0.3 V, V_{CC} + 0.3 V
V_{REF}(+) to V_{REF}(–) . . . . . –0.3 V, +18 V
V_{REF}(+) to AGND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{REF}(–) to AGND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
DSG to AGND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
V_{OUT} (1–4) to AGND . . . . . V_{SS} – 0.3 V, V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
  Extended (S Version). . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic Package
  θ_{JA} Thermal Impedance . . . . . +75°C/W
  Lead Temperature, Soldering (10 sec) . . . . . +260°C
Cerdip Package
  θ_{JA} Thermal Impedance . . . . . +52°C/W
  Lead Temperature, Soldering (10 sec) . . . . . +300°C
SOIC Package
  θ_{JA} Thermal Impedance . . . . . +75°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
PQFP Package
  θ_{JA} Thermal Impedance . . . . . 95°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
PLCC Package
  θ_{JA} Thermal Impedance. . . . . +55°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . . +215°C
    Infrared (15 sec) . . . . . +220°C
Power Dissipation (Any Package) . . . . . 480 mW

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7834/AD7835 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

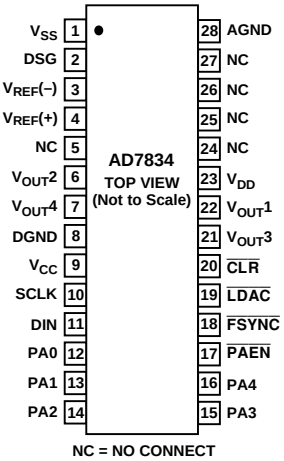
Model	Temperature Range	Linearity Error (LSBs)	DNL (LSBs)	Package Option[1]
AD7834AR	–40°C to +85°C	±2	±0.9	R-28
AD7834BR	–40°C to +85°C	±1	±0.9	R-28
AD7834AN	–40°C to +85°C	±2	±0.9	N-28
AD7834BN	–40°C to +85°C	±1	±0.9	N-28
AD7834SQ	–55°C to +125°C	±2	±0.9	Q-28
AD7835AS[2]	–40°C to +85°C	±2	±0.9	S-44
AD7835BS[2]	–40°C to +85°C	±1	±0.9	S-44
AD7835AP[2]	–40°C to +85°C	±2	±0.9	P-44A

NOTES
[1]R = Small Outline IC (SOIC); N = Plastic DIP; Q = Cerdip; S = Plastic Quad Flatpack (PQFP); P = Plastic Leaded Chip Carrier (PLCC).
[2]Contact Sales Office for availability.

AD7834 PIN DESCRIPTION

Pin Mnemonic	Description
V_{CC}	Logic Power Supply; +5 V ± 5%.
V_{SS}	Negative Analog Power Supply; –15 V ± 5%.
V_{DD}	Positive Analog Power Supply; +15 V ± 5%.
DGND	Digital Ground.
AGND	Analog Ground.
$V_{REF}(+)$	Positive Reference Input. The positive reference voltage is referred to AGND.
$V_{REF}(-)$	Negative Reference Input. The negative reference voltage is referred to AGND.
$V_{OUT}1 \ldots V_{OUT}4$	DAC Outputs.
DSG	Device Sense Ground Input. Used in conjunction with the $\overline{CLR}$ input for power-on protection of the DACs. When $\overline{CLR}$ is low, the DAC outputs are forced to the potential on the DSG pin.
DIN	Serial Data Input.
SCLK	Clock input for writing data to the device.
$\overline{FSYNC}$	Frame Sync Input. Active low logic input used, in conjunction with DIN and SCLK, to write data to the device with serial data expected after the falling edge of this signal. The contents of the 24-bit serial-to-parallel input register are transferred on the rising edge of this signal.
PA0 . . . PA4	Package Address Inputs. These inputs are hardwired high (V_{CC}) or low (DGND) to assign dedicated package addresses in a multipackage environment.
$\overline{PAEN}$	Package Address Enable Input. When low, this input allows normal operation of the device. When it is high, the device ignores the package address (but not the channel address) in the serial data stream and loads the serial data into the input registers. This feature is useful in a multipackage application where it can be used to load the same data into the same channel in each package.
$\overline{LDAC}$	Load DAC Input (level sensitive). This input signal in conjunction with the $\overline{FSYNC}$ input signal, determines how the analog outputs are updated. If $\overline{LDAC}$ is maintained high while new data is being loaded into the device's input registers, no change occurs on the analog outputs. Subsequently, when $\overline{LDAC}$ is brought low, the contents of all four input registers are transferred into their respective DAC latches, updating the analog outputs. Alternatively, if $\overline{LDAC}$ is kept low while new data is shifted into the device, then the addressed DAC latch (and corresponding analog output) is updated immediately on the rising edge of $\overline{FSYNC}$.
$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). When this input is brought low, all analog outputs are switched to the externally set potential on the DSG pin. When $\overline{CLR}$ is brought high, the signal outputs remain at the DSG potential until $\overline{LDAC}$ is brought low. When $\overline{LDAC}$ is brought low, the analog outputs are switched back to reflect their individual DAC output levels. As long as $\overline{CLR}$ remains low, the $\overline{LDAC}$ signals are ignored and the signal outputs remain switched to the potential on the DSG pin.

PIN CONFIGURATION
DIP AND SOIC

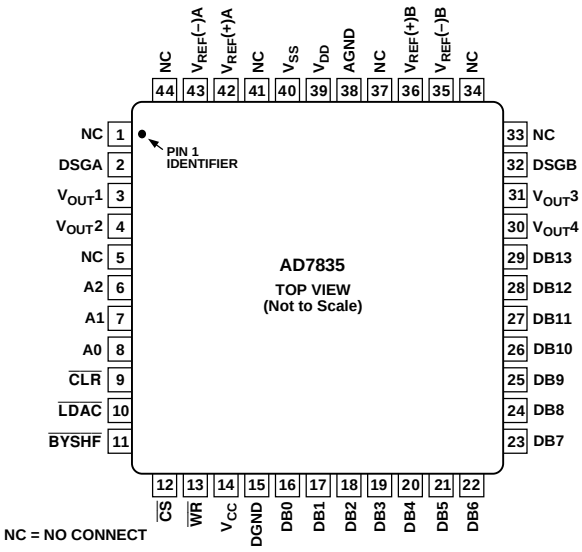


AD7835 PIN DESCRIPTION

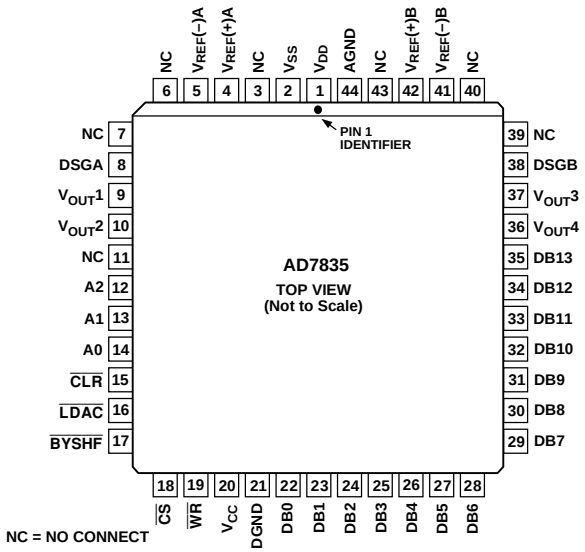
Pin Mnemonic	Description
V_{CC}	Logic Power Supply; +5 V ± 5%.
V_{SS}	Negative Analog Power Supply; –15 V ± 5%.
V_{DD}	Positive Analog Power Supply; +15 V ± 5%.
DGND	Digital Ground.
AGND	Analog Ground.
$V_{REF}(+)A$, $V_{REF}(-)A$	Reference Inputs for DACs 1 and 2. These reference voltages are referred to AGND.
$V_{REF}(+)B$, $V_{REF}(-)B$	Reference Inputs for DACs 3 and 4. These reference voltages are referred to AGND.
$V_{OUT}1 \ldots V_{OUT}4$	DAC Outputs.
$\overline{CS}$	Level-Triggered Chip Select Input (active low). The device is selected when this input is low.
DB0 . . . DB13	Parallel Data Inputs. The AD7835 can accept a straight 14-bit parallel word on DB0 to DB13, where DB13 is the MSB and the $\overline{BYSHF}$ input is hardwired to a logic high. Alternatively for byte loading, the bottom 8 data inputs, DB0–DB7, are used for data loading while the top 6 data inputs, DB8 to DB13, should be hardwired to a logic low. The $\overline{BYSHF}$ control input selects whether 8 LSBs or 6 MSBs of data are being loaded into the device.
$\overline{BYSHF}$	Byte Shift Input. When low, it shifts the data on DB0–DB7 into the DB8–DB13 half of the input register.
A0, A1, A2	Address inputs. A0 and A1 are decoded to select one of the four input latches for a data transfer. A2 is used to select all four DACs simultaneously.
$\overline{LDAC}$	Load DAC Input (level sensitive). This input signal in conjunction with the $\overline{WR}$ and $\overline{CS}$ input signals, determines how the analog outputs are updated. If $\overline{LDAC}$ is maintained high while new data is being loaded into the device's input registers, no change occurs on the analog outputs. Subsequently, when $\overline{LDAC}$ is brought low, the contents of all four input registers are transferred into their respective DAC latches, updating the analog outputs simultaneously. Alternatively, if $\overline{LDAC}$ is brought low while new data is being entered, then the addressed DAC latch (and corresponding analog output) is updated immediately on the rising edge of $\overline{WR}$.
$\overline{CLR}$	Asynchronous Clear Input (level sensitive, active low). When this input is brought low, all analog outputs are switched to the externally set potentials on the DSG pins ($V_{OUT}1$ and $V_{OUT}2$ follow DSGA while $V_{OUT}3$ and $V_{OUT}4$ follow DSGB). When $\overline{CLR}$ is brought high, the signal outputs remain at the DSG potentials until $\overline{LDAC}$ is brought low. When $\overline{LDAC}$ is brought low, the analog outputs are switched back to reflect their individual DAC output levels. As long as $\overline{CLR}$ remains low, the $\overline{LDAC}$ signals are ignored and the signal outputs remain switched to the potential on the DSG pins.
$\overline{WR}$	Level-Triggered Write Input (active low). When active it is used in conjunction with $\overline{CS}$ to write data over the input data bus.
DSGA	Device Sense Ground A Input. Used in conjunction with the $\overline{CLR}$ input for power-on protection of the DACs. When $\overline{CLR}$ is low, DAC outputs $V_{OUT}1$ and $V_{OUT}2$ are forced to the potential on the DSGA pin.
DSGB	Device Sense Ground B Input. Used in conjunction with the $\overline{CLR}$ input for power-on protection of the DACs. When $\overline{CLR}$ is low, DAC outputs $V_{OUT}3$ and $V_{OUT}4$ are forced to the potential on the DSGB pin.

PIN CONFIGURATIONS

PQFP



PLCC



TERMINOLOGY

Relative Accuracy

Relative Accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full-scale error and is normally expressed in Least Significant Bits or as a percentage of full-scale reading.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

DC Crosstalk

Although the common input reference voltage signals are internally buffered, small IR drops in the individual DAC reference inputs across the die can mean that an update to one channel can produce a dc output change in one or other of the channel outputs.

The four DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this can result in a further dc change in one or other channel outputs. This effect is most obvious at high load currents and reduces as the load currents are reduced. With high impedance loads the effect is virtually unmeasurable.

Output Voltage Settling Time

This is the amount of time it takes for the output to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Impulse

This is the amount of charge injected into the analog output when the inputs change state. It is specified as the area of the glitch in nV-secs. It is measured with the reference inputs connected to 0 V and the digital inputs toggled between all 1s and all 0s.

Channel-to-Channel Isolation

Channel-to-channel isolation refers to the proportion of input signal from one DACs reference input which appears at the output of the other DAC. It is expressed in dBs.

The AD7834 has no specification for Channel-to-channel isolation because it has one reference for all DACs. Channel-to-channel isolation is specified for the AD7835.

DAC-to-DAC Crosstalk

DAC-to-DAC Crosstalk is defined as the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog O/P change at another converter. It is specified in nV-s.

Digital Crosstalk

The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as the Digital Crosstalk and is specified in nV-s.

Digital Feedthrough

When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the V_{OUT} pins. This noise is digital feedthrough.

DC Output Impedance

This is the effective output source resistance. It is dominated by package lead resistance.

Full-Scale Error

This is the error in DAC output voltage when all 1s are loaded into the DAC latch. Ideally the output voltage, with all 1s loaded into the DAC latch, should be $V_{REF}(+) - 1$ LSB. Full-Scale Error does not include Zero-Scale Error.

Zero-Scale Error

Zero-Scale Error is the error in the DAC output voltage when all 0s are loaded into the DAC latch. Ideally the output voltage, with all 0s in the DAC latch should be equal to $V_{REF}(-)$. Zero-Scale Error is mainly due to offsets in the output amplifier.

Gain Error

Gain Error is defined as (Full-Scale Error) – (Zero-Scale Error).

AD7834/AD7835–Typical Performance Characteristics

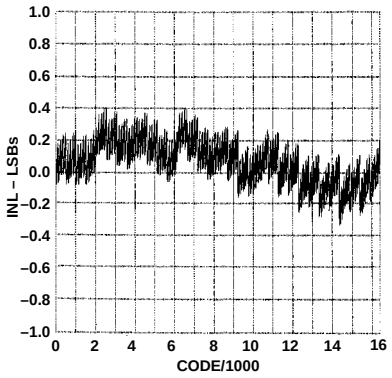


Figure 3. Typical INL Plot

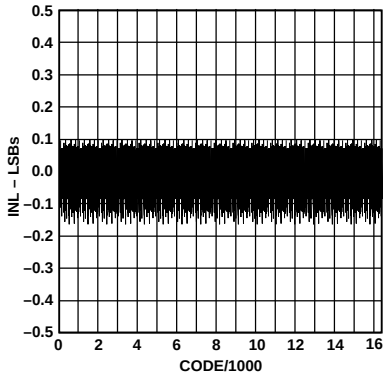


Figure 4. Typical DNL Plot

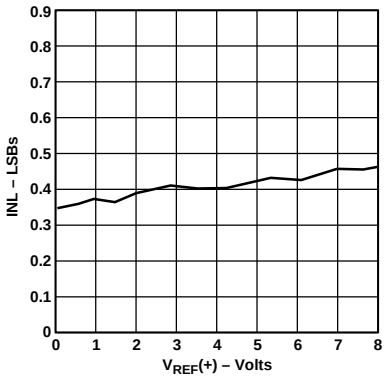


Figure 5. Typical INL vs. $V_{REF}(+)$ ($V_{REF}(–) = –6$ V)

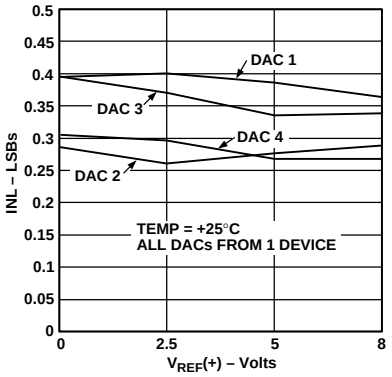


Figure 6. Typical INL vs. $V_{REF}(+)$ ($V_{REF}(+) – V_{REF}(–) = 5$ V)

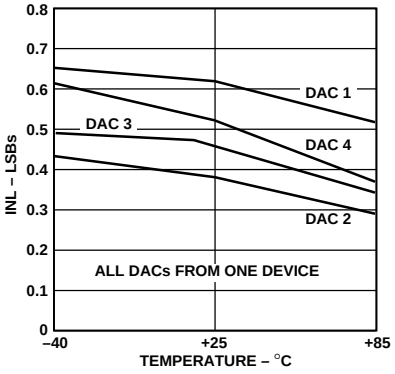


Figure 7. Typical INL vs. Temperature

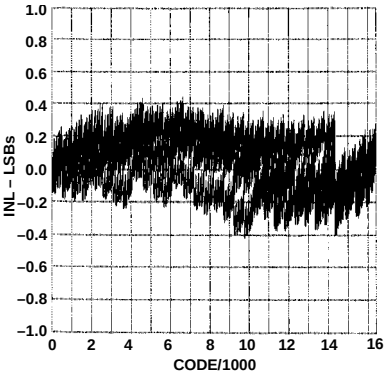


Figure 8. Typical DAC-to-DAC Matching

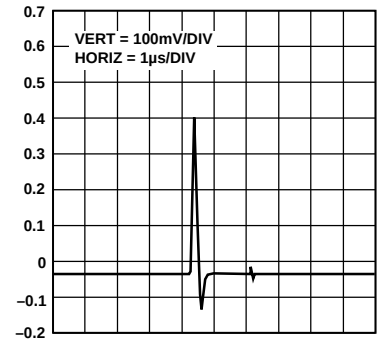


Figure 9. Typical Digital/Analog Glitch Impulse

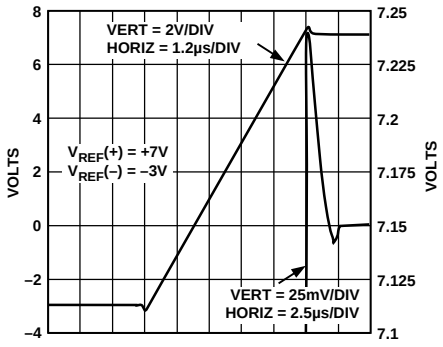


Figure 10. Settling Time (+)

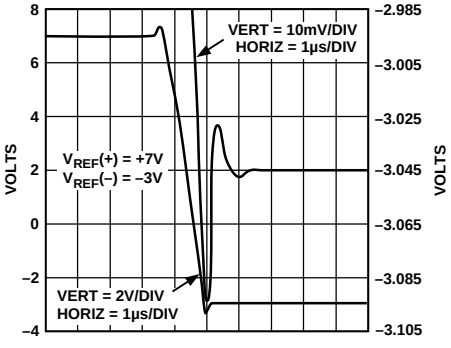


Figure 11. Settling Time (–)

GENERAL DESCRIPTION

DAC Architecture—General

Each channel consists of a segmented 14-bit R-2R voltage-mode DAC. The full- scale output voltage range is equal to the entire reference span of $V_{REF}(+) - V_{REF}(-)$. The DAC coding is straight binary; all 0s produces an output of $V_{REF}(-)$; all 1s produces an output of $V_{REF}(+) - 1$ LSB.

The analog output voltage of each DAC channel reflects the contents of its own DAC latch. Data is transferred from the external bus to the input register of each DAC latch on a per channel basis. The AD7835 has a feature whereby using the A2 pin, data can be transferred from the input data bus to all four input registers simultaneously.

Bringing the $\overline{CLR}$ line low switches all the signal outputs, $V_{OUT}1$ to $V_{OUT}4$, to the voltage level on the DSG pin. The signal outputs are held at this level after the removal of the $\overline{CLR}$ signal and will not switch back to the DAC outputs until the $\overline{LDAC}$ signal is exercised.

Data Loading—AD7834, Serial Input Device

A write operation transfers 24 bits of data to the AD7834. The first 8 bits are control data and the remaining 16 bits are DAC data (see Figure 12). The control data identifies the DAC channel to be updated with new data and which of 32 possible packages the DAC resides in. In any communication with the device the first 8 bits must always be control data.

Note that the DAC output voltages, $V_{OUT}1$ to $V_{OUT}4$, can be updated to reflect new data in the DAC input registers in one of two ways. The first method normally keeps $\overline{LDAC}$ high and only pulses $\overline{LDAC}$ low momentarily to update all DAC latches simultaneously with the contents of their respective input registers. The second method ties $\overline{LDAC}$ low, and channel updating occurs on a per channel basis after new data has been clocked into the AD7834. With $\overline{LDAC}$ low, the rising edge of $\overline{FSYNC}$ transfers the new data directly into the DAC latch, updating the analog output voltage.

Data being shifted into the AD7834 enters a 24-bit long shift register. If more than 24 bits are clocked in before $\overline{FSYNC}$ goes high, the last 24 bits transmitted are used as the control data and DAC data.

Individual bit functions are discussed below.

D23: Determines whether the following 23-bits of address and data should be used or should be ignored. This is effectively a software Chip Select bit. D23 is the first bit to be transmitted in the 24-bit long word.

Table I. D23 Control

D23	Control Function
0	Ignore following 23 bits of information.
1	Use following 23 bits of address and data as normal.

D22 and D21: Decoded to select one of the four DAC channels within a device. The truth table for D22 and D21 is as shown below in Table II.

Table II. D22, D21 Control

D22	D21	Control Function
0	0	Select Channel 1
0	1	Select Channel 2
1	0	Select Channel 3
1	1	Select Channel 4

D20–D16: Determines the package address. The five address bits allow up to 32 separate packages to be individually decoded. Successful decoding is accomplished when these five bits match up with the five hardwired pins on the physical package.

D15–D0: DAC Data to be loaded into identified DAC Input Register. This data must have two leading 0s followed by 14 bits of data, MSB first. The MSB is in location D13 of the 24-bit data stream.

Data Loading—AD7835, Parallel Loading Device

Data can be loaded into the AD7835 in either straight 14-bit wide words or in two 8-bit bytes.

In systems which can transfer 14-bit wide data, the $\overline{BYSHF}$ input should be hardwired to V_{CC}. This sets up the AD7835 as a straight 14-bit parallel-loading DAC.

In 8-bit bus systems where it is required to transfer data in two bytes, it is necessary to have the $\overline{BYSHF}$ input under logic control. In such a system the top 6 pins of the device data bus, DB8–DB13, must be hardwired to DGND. New low byte data is loaded into the lower 8 places of the selected input register by carrying out a write operation while holding $\overline{BYSHF}$ high. A second write operation is subsequently executed with $\overline{BYSHF}$ low and the 6 MSBs on the DB0–DB5 inputs (DB5 = MSB).

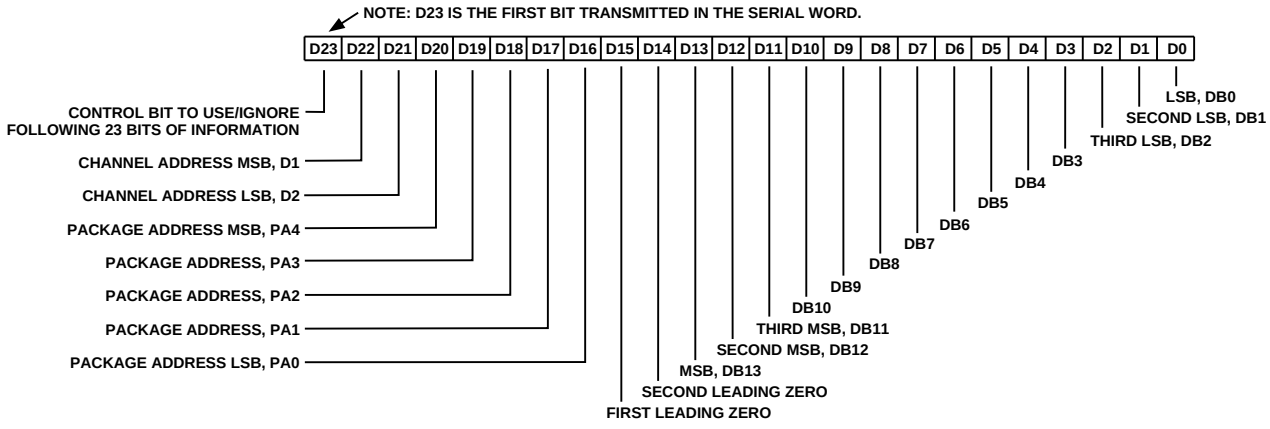


Figure 12. Bit Assignments for 24-Bit Data Stream of AD7834

When 14-bit transfers are being used, the DAC output voltages, $V_{OUT}1$–$V_{OUT}4$, can be updated to reflect new data in the DAC input registers in one of two ways. The first method normally keeps $\overline{LDAC}$ high and only pulses $\overline{LDAC}$ low momentarily to update all DAC latches simultaneously with the contents of their respective input registers. The second method ties $\overline{LDAC}$ low and channel updating occurs on a per channel basis after new data is loaded to an input register.

In order to avoid the DAC output going to an intermediate value during a 2-byte transfer, $\overline{LDAC}$ should not be tied low permanently, but should be held high until the 2 bytes are written to the input register. When the selected input register has been loaded with the 2 bytes, $\overline{LDAC}$ should then be pulsed low to update the DAC latch and, hence, perform the digital-to-analog conversion.

In many applications, it may be acceptable to allow the DAC output to go to an intermediate value during a 2-byte transfer. In such applications, $\overline{LDAC}$ can be tied low, thus using one less control line.

The actual DAC input register that is being written to is determined by the logic levels present on the devices address lines, as shown in Table III.

Table III. AD7835—Address Line Truth Table

A2	A1	A0	DAC Selected
0	0	0	DAC 1
0	0	1	DAC 2
0	1	0	DAC 3
0	1	1	DAC 4
1	X	X	All DACs Selected

Unipolar Configuration

Figure 13 shows the AD7834/AD7835 in the unipolar binary circuit configuration. The $V_{REF}(+)$ input of the DAC is driven by the AD586, a +5 V reference. $V_{REF}(-)$ is tied to ground. Table IV gives the code table for unipolar operation of the AD7834/AD7835.

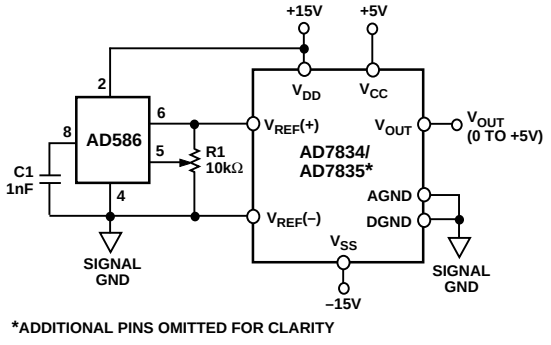


Figure 13. Unipolar +5 V Operation

Offset and gain may be adjusted in Figure 13 as follows: To adjust offset, disconnect the $V_{REF}(-)$ input from 0 V, load the DAC with all 0s and adjust the $V_{REF}(-)$ voltage until V_{OUT} = 0 V. For gain adjustment, the AD7834/AD7835 should be loaded with all 1s and R1 adjusted until V_{OUT} = 5 V(16383/16384) = 4.999695.

Many circuits will not require these offset and gain adjustments. In these circuits R1 can be omitted. Pin 5 of the AD586 may be left open circuit and Pin 2 ($V_{REF}(-)$) of the AD7834/AD7835 tied to 0 V.

Table IV. Code Table for Unipolar Operation

Binary Number in DAC Latch MSB			LSB	Analog Output (V_{OUT})
11	1111	1111	1111	V_{REF} (16383/16384) V
10	0000	0000	0000	V_{REF} (8192/16384) V
01	1111	1111	1111	V_{REF} (8191/16384) V
00	0000	0000	0001	V_{REF} (1/16384) V
00	0000	0000	0000	0 V

NOTE
$V_{REF} = V_{REF}(+)$; $V_{REF}(-)$ = 0 V for unipolar operation.
For $V_{REF}(+)$ = +5 V, 1 LSB = +5 V/2^{14} = +5 V/16384 = 305 μV.

Bipolar Configuration

Figure 14 shows the AD7834/AD7835 set up for ±5 V operation. The AD588 provides precision ±5 V tracking outputs which are fed to the $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the AD7834/AD7835. The code table for bipolar operation of the AD7834/AD7835 is shown in Table V.

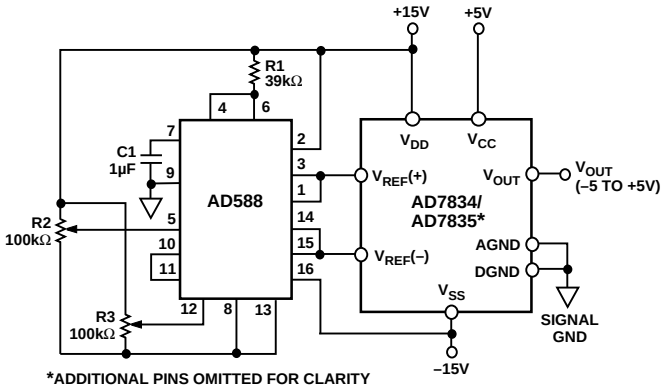


Figure 14. Bipolar ±5 V Operation

Table V. Code Table for Bipolar Operation

Binary Number in DAC Latch MSB			LSB	Analog Output (V_{OUT})
11	1111	1111	1111	$V_{REF}(-) + V_{REF}$ (16383/16384) V
10	0000	0000	0001	$V_{REF}(-) + V_{REF}$ (8193/16384) V
10	0000	0000	0000	$V_{REF}(-) + V_{REF}$ (8192/16384) V
01	1111	1111	1111	$V_{REF}(-) + V_{REF}$ (8191/16384) V
00	0000	0000	0001	$V_{REF}(-) + V_{REF}$ (1/16384) V
00	0000	0000	0000	$V_{REF}(-)$ V

NOTE
$V_{REF} = (V_{REF}(+) - V_{REF}(-))$.
For $V_{REF}(+)$ = +5 V, and $V_{REF}(-)$ = –5 V, 1 LSB = 10 V/2^{14} = 10 V/16384 = 610 μV.

In Figure 14, full-scale and bipolar zero adjustments are provided by varying the gain and balance on the AD588. R2 varies the gain on the AD588 while R3 adjusts the offset of both the +5 V and –5 V outputs together with respect to ground.

For bipolar-zero adjustment, the DAC is loaded with 1000 . . . 0000 and R3 is adjusted until V_{OUT} = 0 V. Full scale is adjusted by loading the DAC with all 1s and adjusting R2 until V_{OUT} = 5(8191/8192) V = 4.99939 V.

When bipolar-zero and full-scale adjustment are not needed, R2 and R3 can be omitted. Pin 12 on the AD588 should be connected to Pin 11 and Pin 5 should be left floating.

CONTROLLED POWER-ON OF THE OUTPUT STAGE

A block diagram of the output stage of the AD7834/AD7835 is shown in Figure 15. It is capable of driving a load of 10 kΩ in parallel with 200 pF. G_1 to G_6 are transmission gates that are used to control the power on voltage present at V_{OUT}. G_1 and G_2 are also used in conjunction with the $\overline{CLR}$ input to set V_{OUT} to the user defined voltage present at the DSG pin.

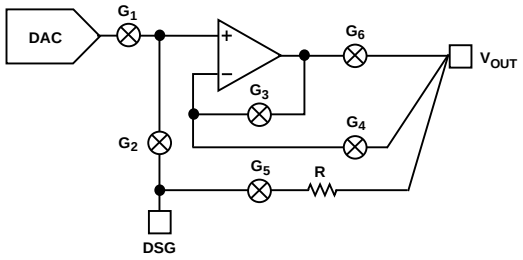


Figure 15. Block Diagram of AD7834/AD7835 Output Stage

Power-On with $\overline{CLR}$ Low, $\overline{LDAC}$ High

The output stage of the AD7834/AD7835 has been designed to allow output stability during power-on. If $\overline{CLR}$ is kept low during power-on, then just after power is applied to the part, the situation is as depicted in Figure 16. G_1, G_4 and G_6 are open while G_2, G_3 and G_5 are closed.

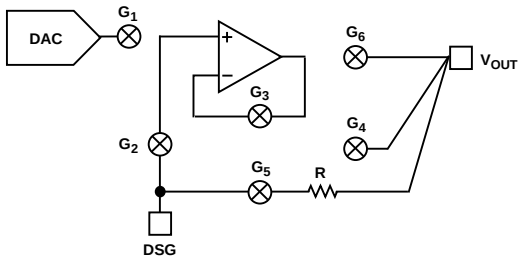


Figure 16. Output Stage with V_{DD} < 10 V

V_{OUT} is kept within a few hundred millivolts of DSG via G_5 and R. R is a thin-film resistor between DSG and V_{OUT}. The output amplifier is connected as a unity gain buffer via G_3 and the DSG voltage is applied to the buffer input via G_2. The amplifiers output is thus at the same voltage as the DSG pin. The output stage remains configured as in Figure 16 until the voltage at V_{DD} and V_{SS} reaches approximately ±10 V. By now the output amplifier has enough headroom to handle signals at its input and has also had time to settle. The internal power-on circuitry opens G_3 and G_5 and closes G_4 and G_6. This situation is shown in Figure 17. Now the output amplifier is connected in unity gain mode via G_4 and G_6. The DSG voltage is still applied to the noninverting input via G_2. This voltage appears at V_{OUT}.

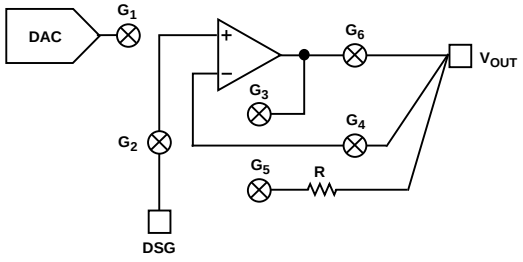


Figure 17. Output Stage with V_{DD} > 10 V and $\overline{CLR}$ Low

V_{OUT} has been disconnected from the DSG pin by the opening of G_5 but will track the voltage present at DSG via the unity gain buffer.

Power-On with $\overline{LDAC}$ Low, $\overline{CLR}$ High

In many applications of the AD7834/AD7835 $\overline{LDAC}$ will be kept continuously low, thus updating the DAC after each valid data transfer. If $\overline{LDAC}$ is low when power is applied, then G_1 is closed and G_2 is open, thus connecting the output of the DAC to the input of the output amplifier. G_3 and G_5 will be closed and G_4 and G_6 open, connecting the amplifier as a unity gain buffer, as before. V_{OUT} is connected to DSG via G_5 and R (a thin film resistance between DSG and V_{OUT}) until V_{DD} and V_{SS} reach approximately ±10 V. Then, the internal power-on circuitry opens G_3 and G_5 and closes G_4 and G_6. This is the situation shown in Figure 18. V_{OUT} is now at the same voltage as the DAC output.

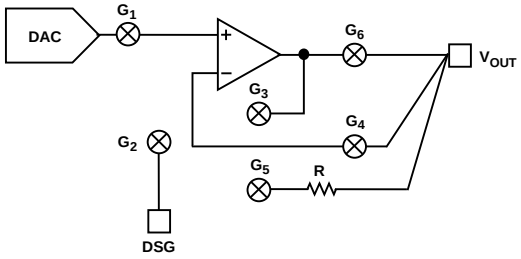


Figure 18. Output Stage with $\overline{LDAC}$ Low

Loading the DAC and Using the $\overline{CLR}$ Input

When $\overline{LDAC}$ goes low, it closes G_1 and opens G_2 as in Figure 18. The voltage at V_{OUT} now follows the voltage present at the output of the DAC. The output stage remains connected in this manner until a $\overline{CLR}$ signal is applied. Then the situation reverts to that shown in Figure 17. Once again V_{OUT} remains at the same voltage as DSG until $\overline{LDAC}$ goes low. This reconnects the DAC output to the unity gain buffer.

DSG Voltage Range

During power-on, the V_{OUT} pins of the AD7834/AD7835 are connected to the relevant DSG pins via G_6 and the thin film resistor, R. The DSG potential must obey the max ratings at all times. Thus, the voltage at DSG must always be within the range V_{SS} – 0.3 V, V_{DD} + 0.3 V. However, in order that the voltages at the V_{OUT} pins of the AD7834/AD7835 stay within ±2 V of the relevant DSG potential during power-on, the voltage applied to DSG should also be kept within the range AGND – 2 V, AGND + 2 V.

Once the AD7834/AD7835 has powered on and the on-chip amplifiers have settled, the situation is as shown as in Figure 17. Any voltage that is now applied to the DSG pin is buffered by the same amplifier that buffers the DAC output voltage in normal operation. Thus, for specified operation, the maximum voltage that can be applied to the DSG pin increases to the maximum allowable $V_{REF}(+)$ voltage, and the minimum voltage that can be applied to DSG is the minimum $V_{REF}(–)$ voltage. After the AD7834/AD7835 has fully powered on, the outputs can track any DSG voltage within this minimum/maximum range.

POWER-ON OF THE AD7834/AD7835

Power should normally be applied to the AD7834/AD7835 in the following sequence: first V_{DD} and V_{SS}, then V_{CC}, then $V_{REF}(+)$ and $V_{REF}(–)$.

The V_{REF} pins should never be allowed to float when power is applied to the part. (V_{REF}(+) should never be allowed to go below V_{REF}(–)–0.3 V. V_{REF}(–) should never be allowed to go below V_{SS}–0.3 V. V_{DD} should never be allowed to go below V_{CC}–0.3 V.

In some systems it may be necessary to introduce one or more Schottky diodes between pins to prevent the above situations arising at power-on. These diodes are shown in Figure 19. However in most systems, with careful consideration given to power supply sequencing, the above rules will be adhered to and protection diodes won't be necessary.

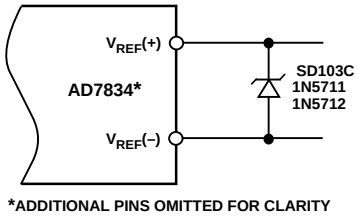


Figure 19. Power-ON Protection

MICROPROCESSOR INTERFACING

AD7834 to 80C51 Interface

A serial interface between the AD7834 and the 80C51 microcontroller is shown in Figure 20. TXD of the 80C51 drives SCLK of the AD7834 while RXD drives the serial data line of the part.

The 80C51 provides the LSB of its SBUF register as the first bit in the serial data stream. The AD7834 expects the MSB of the 24-bit write first. Therefore, the user will have to ensure that the data in the SBUF register is arranged correctly so that this is taken into account. When data is to be transmitted to the part, P3.3 is taken low. Data on RXD is valid on the falling edge of TXD. The 80C51 transmits its data in 8-bit bytes with only 8 falling clock edges occurring in the transmit cycle. To load data to the AD7834, P3.3 is left low after the first eight bits are transferred. A second byte is then transferred, with P3.3 still kept low. After the third byte has been transferred, the P3.3 line is taken high.

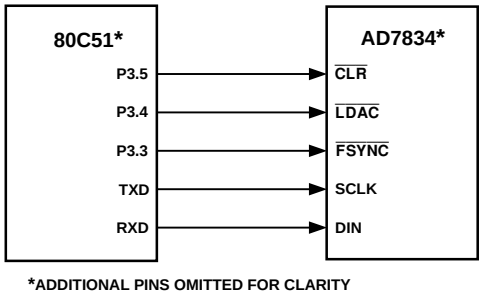


Figure 20. AD7834 to 80C51 Interface

$\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ on the AD7834 are also controlled by 80C51 port outputs. The user can bring $\overline{\text{LDAC}}$ low after every three bytes have been transmitted to update the DAC which has been programmed. Alternatively, it is possible to wait until all the input registers have been loaded (twelve byte transmits) and then update the DAC outputs.

AD7834 to 68HC11 Interface

Figure 21 shows a serial interface between the AD7834 and the 68HC11 microcontroller. SCK of the 68HC11 drives SCLK of the AD7834 while the MOSI output drives the serial data line, DIN, of the AD7834. The FSYNC signal is derived from port line PC7 in this example.

For correct operation of this interface, the 68HC11 should be configured such that its CPOL bit is a 0 and its CPHA bit is a 1. When data is to be transferred to the part, PC7 is taken low. When the 68HC11 is configured like this, data on MOSI is valid on the falling edge of SCK. The 68HC11 transmits its serial data in 8-bit bytes, MSB first. The AD7834 expects the MSB of the 24-bit write first also. Eight falling clock edges occur in the transmit cycle. To load data to the AD7834, PC7 is left low after the first eight bits are transferred. A second byte of data is then transmitted serially to the AD7834. Then a third byte is transmitted, and when this transfer is complete, the PC7 line is taken high.

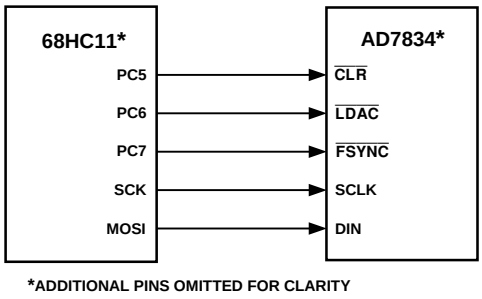


Figure 21. AD7834 to 68HC11 Interface

In Figure 21, $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ are controlled by the PC6 and PC5 port outputs. As with the 80C51, each DAC of the AD7834 can be updated after each three-byte transfer, or else all DACs can be simultaneously updated after twelve bytes have been transferred.

AD7834 to ADSP-2101 Interface

An interface between the AD7834 and the ADSP-2101 is shown in Figure 22. In the interface shown, SPORT0 is used to transfer data to the part. SPORT1 is configured for alternate functions. FO, the flag output on SPORT1, is connected to $\overline{\text{LDAC}}$ and is used to load the DAC latches. In this way data can be transferred from the ADSP-2101 to all the input registers in the DAC and the DAC latches can be updated simultaneously. In the application shown, the CLR pin on the AD7834 is controlled by circuitry that monitors the power in the system.

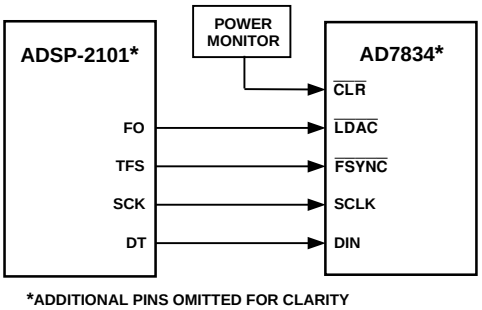


Figure 22. AD7834 to ADSP-2101 Interface

The AD7834 requires 24 bits of serial data framed by a single $\overline{\text{FSYNC}}$ pulse. It is necessary that this $\overline{\text{FSYNC}}$ pulse stays low until all the data has been transferred. This can be provided by the ADSP-2101 in one of two ways. Both require setting the se-

rial word length of the SPORT to 12 bits, with the following conditions: Internal SCLK; Alternate framing mode; Active low framing signal. Data can be transferred using the Autobuffering feature of the ADSP-2101, sending two 12-bit words directly after each other. This ensures a continuous TFS pulse. Alternatively, the first data word can be loaded to the serial port, the subsequent interrupt that is generated can be trapped and then the second data word can be sent immediately after the first. Again this produces a continuous TFS pulse that frames the 24 data bits.

AD7834 to DSP56000/DSP56001 Interface

Figure 23 shows a serial interface between the AD7834 and the DSP56000/DSP56001. The serial port is configured for a word length of 24 bits, gated clock and with FSL0 and FSL1 control bits each set to "0." Normal Mode Synchronous operation is selected which allows the use of SC0 and SC1 as outputs controlling $\overline{CLR}$ and $\overline{LDAC}$. The framing signal on SC2 has to be inverted before being applied to FSYNC. SCK is internally generated on the DSP56000/DSP56001 and is applied to SCLK on the AD7834. Data from the DSP56000/DSP56001 is valid on the falling edge of SCK.

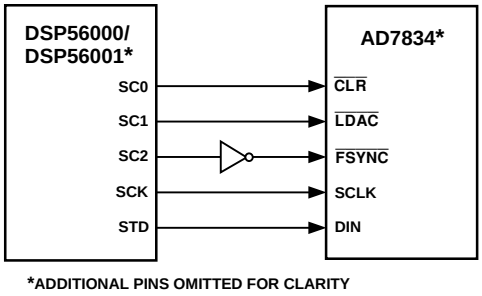


Figure 23. AD7834 to DSP5600/DSP56001 Interface

AD7834 to TMS32020/TMS320C25

A serial interface between the AD7834 and the TMS32020/TMS320C25 DSP processor is shown in Figure 24. The CLKX and FSX signals for the TMS32020/TMS32025 should be generated using an external clock/timer circuit. The CLKX and FSX pin should be configured as inputs. The TMS32020/TMS320C25 should be set up for an 8-bit serial data length. Data can then be written to the AD7834 by writing three bytes to the serial port of the TMS32020/TMS320C25. In the configuration shown in Figure 24 the $\overline{CLR}$ input on the AD7834 is controlled by the XF output on the TMS32020/TMS320C25. The clock/timer circuit controls the $\overline{LDAC}$ input on the AD7834. Alternatively, $\overline{LDAC}$ could also be tied to ground to allow automatic update of the DAC latches after each transfer.

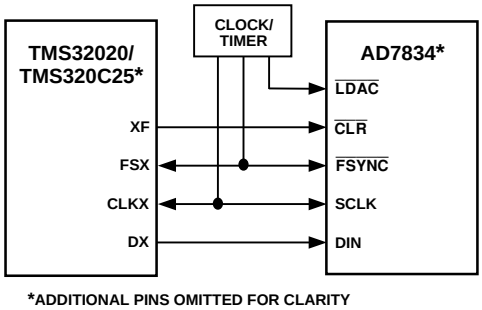


Figure 24. AD7834 to TMS32020/TMS320C25 Interface

Interfacing the AD7835—16-Bit Interface

The AD7835 can be interfaced to a variety of microcontrollers or DSP processors, both 8-bit and 16-bit. Figure 25 shows the AD7835 interfaced to a generic 16-bit microcontroller/DSP processor. $\overline{BYSHF}$ is tied to V_{CC} in this interface. The lower address lines from the processor are connected to A0, A1 and A2 on the AD7835 as shown. The upper address lines are decoded to provide a chip select signal for the AD7835. They are also decoded (in conjunction with the lower address lines if need be) to provide a $\overline{LDAC}$ signal. Alternatively, $\overline{LDAC}$ could be driven by an external timing circuit or just tied low. The data lines of the processor are connected to the data lines of the AD7835. The selection of the DACs is as given in Table III.

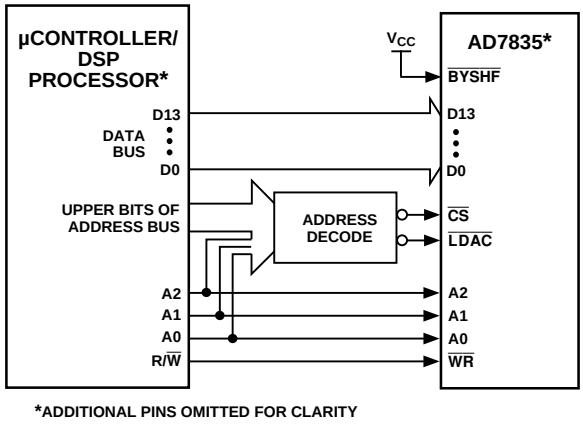


Figure 25. AD7835 16-Bit Interface

8-Bit Interface

Figure 26 shows an 8-bit interface between the AD7835 and a generic 8-bit microcontroller/DSP processor. Pins D13 to D8 of the AD7835 are tied to DGND. Pins D7 to D0 of the processor are connected to pins D7 to D0 of the AD7835. $\overline{BYSHF}$ is driven by the A0 line of the processor. This maps the DAC upper bits and lower bits into adjacent bytes in the processors address space. Table VI shows the truth table for addressing the DACs in the AD7835. If, for example, the base address for the DACs in the processor address space is decoded by the upper address bits to location HC000, then the first DAC's upper and lower bits are at locations HC000 and HC001 respectively.

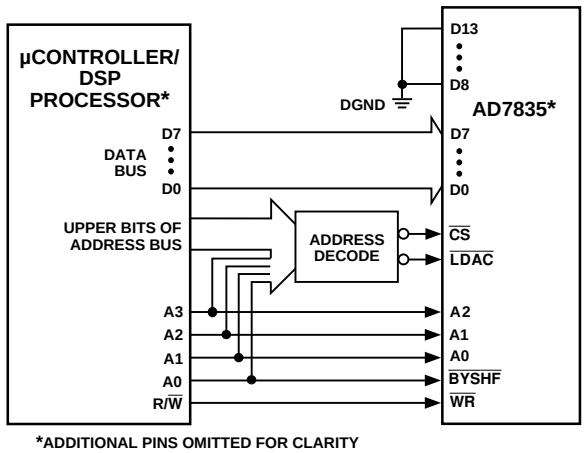


Figure 26. AD7835 8-Bit Interface

When writing to the DACs, the lower 8 bits must be written first, followed by the upper 6 bits. The upper 6 bits should be output on data lines D0 to D5. Once again, the upper address lines of the processor are decoded to provide a $\overline{CS}$ signal. They are also decoded in conjunction with lines A3 to A0 to provide a $\overline{LDAC}$ signal. Alternatively, $\overline{LDAC}$ can be driven by an external timing circuit or, if it's acceptable to allow the DAC output to go to an intermediate value between 8-bit writes, $\overline{LDAC}$ can be tied low.

Table VI. DAC Selection, 8-Bit Interface

Processor Address Lines A3	A2	A1	A0	DAC Selected
1	X	X	0	Upper 6 Bits of All DACs
1	X	X	1	Lower 8 Bits of All DACs
0	0	0	0	Upper 6 Bits, DAC 1
0	0	0	1	Lower 8 Bits, DAC 1
0	0	1	0	Upper 6 Bits, DAC 2
0	0	1	1	Lower 8 Bits, DAC 2
0	1	0	0	Upper 6 Bits, DAC 3
0	1	0	1	Lower 8 Bits, DAC 3
0	1	1	0	Upper 6 Bits, DAC 4
0	1	1	1	Lower 8-Bits, DAC 4

APPLICATIONS

Serial Interface to Multiple AD7834s

Figure 27 shows how the Package Address pins of the AD7834 are used to address multiple AD7834s. The figure shows only 10 devices, but up to 32 AD7834s can each be assigned a unique address by hardwiring each of the Package Address pins to V_{CC} or DGND. Normal operation of the device occurs when $\overline{PAEN}$ is low. When serial data is being written to the AD7834s, only the device with the same package address as the package address contained in the serial data will accept data into the input registers. If, on the other hand, $\overline{PAEN}$ is high, the package address is ignored and the data is loaded into the same channel on each package.

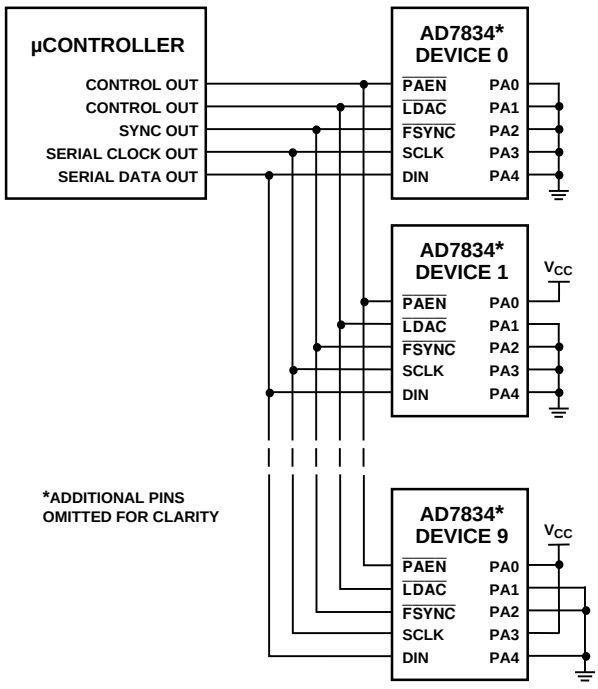


Figure 27. Serial Interface to Multiple AD7834s

The main limitation with multiple packages is the output update rate. For example, if an output update rate of 10 kHz is required, then there are 100 µs to load all DACs. Assuming a serial clock frequency of 10 MHz, it takes 2.5 µs to load data to one DAC. Thus forty DACs or ten packages can be updated in this time. As the update rate requirement decreases, the number of possible packages increases.

Opto-Isolated Interface

In many process control applications it is necessary to provide an isolation barrier between the controller and the unit being controlled. Opto-isolators can provide voltage isolation in excess of 3 kV. The serial loading structure of the AD7834 makes it ideal for opto-isolated interfaces as the number of interface lines is kept to a minimum. Figure 28 shows a 5-channel isolated interface to the AD7834. Multiple devices are connected to the outputs of the opto-coupler and controlled as explained above. To reduce the number of opto-isolators, the $\overline{PAEN}$ line doesn't need to be controlled if it is not used. If the $\overline{PAEN}$ line is not controlled by the microcontroller then it should be tied low at each device. If simultaneous updating of the DACs is not required, then $\overline{LDAC}$ pin on each part can be tied permanently low and a further opto-isolator is not needed.

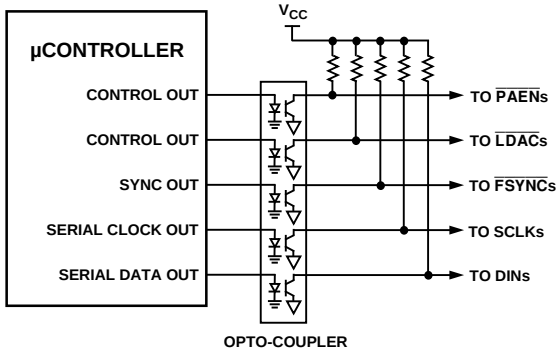


Figure 28. Opto-Isolated Interface

Automated Test Equipment

The AD7834/AD7835 is particularly suited for use in an automated test environment. Figure 29 shows the AD7835 providing the necessary voltages for the pin driver and the window comparator in a typical ATE pin electronics configuration. Two AD588s are used to provide reference voltages for the AD7835. In the configuration shown, the AD588s are configured so that the voltage at Pin 1 is 5 V greater than the voltage at Pin 9 and the voltage at Pin 15 is 5 V less than the voltage at Pin 9.

One of the AD588s is used as a reference for DACs 1 and 2. These DACs are used to provide high and low levels for the pin driver. The pin driver may have an associated offset. This can be nulled by applying an offset voltage to Pin 9 of the AD588. First, the code 1000 . . . 0000 is loaded into the DAC1 latch and the pin driver output is set to the DAC1 output. The

V_{OFFSET} voltage is adjusted until 0 V appears between the pin driver output and DUT GND. This causes both $V_{REF}(+)A$ and $V_{REF}(-)A$ to be offset with respect to AGND by an amount equal to V_{OFFSET}. However the output of the pin driver will vary from –5 V to +5 V with respect to DUT GND as the DAC input code varies from 000 . . . 000 to 111 . . . 111. The V_{OFFSET} voltage is also applied to the DSG A pin. When a clear is performed on the AD7835, the output of the pin driver will be 0 V with respect to DUT GND.

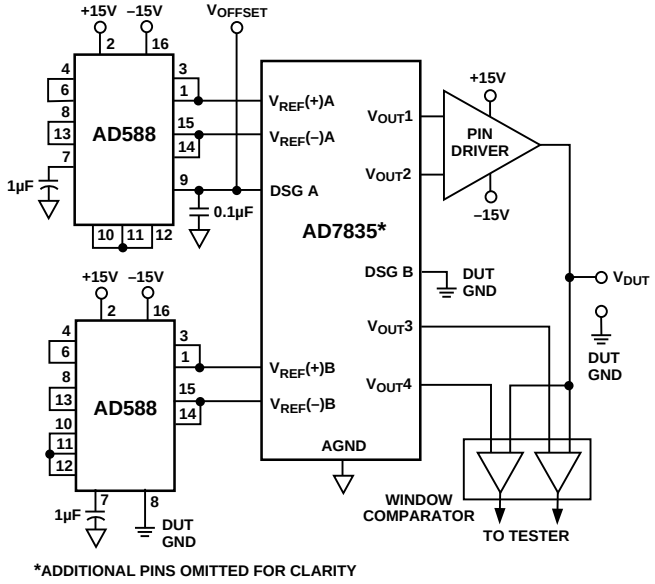


Figure 29. ATE Application

The other AD588 is used to provide a reference voltage for DACs 3 and 4. These provide the reference voltages for the window comparator shown in the diagram. Note that Pin 9 of this AD588 is connected to DUT GND. This causes $V_{REF}(+)B$ and $V_{REF}(-)B$ to be referenced to DUT GND. As DAC 3 and DAC 4 input codes vary from 000 . . . 000 to 111 . . . 111, $V_{OUT}3$ and $V_{OUT}4$ vary from –5 V to +5 V with respect to DUT GND. DUT GND is also connected to DSG B. When the AD7835 is cleared, $V_{OUT}3$ and $V_{OUT}4$ are cleared to 0 V with respect to DUT GND.

Care must be taken to ensure that the maximum and minimum voltage specs for the AD7835 reference voltages are not broken in the above configuration.

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7834/AD7835 is mounted should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should only be joined at one place. If the AD7834/AD7835 is the only device requiring an AGND to DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD7834/AD7835. If the AD7834/AD7835 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point which should be established as close as possible to the AD7834/AD7835.

Digital lines running under the device should be avoided as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7834/AD7835 to avoid noise coupling. The power supply lines of the AD7834/AD7835 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

The AD7834/AD7835 should have ample supply bypassing located as close to the package as possible, ideally right up against the device. Figure 30 shows the recommended capacitor values of 10 µF in parallel with 0.1 µF on each of the supplies. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

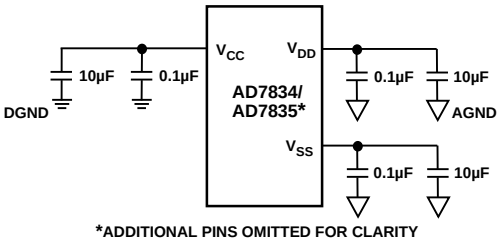
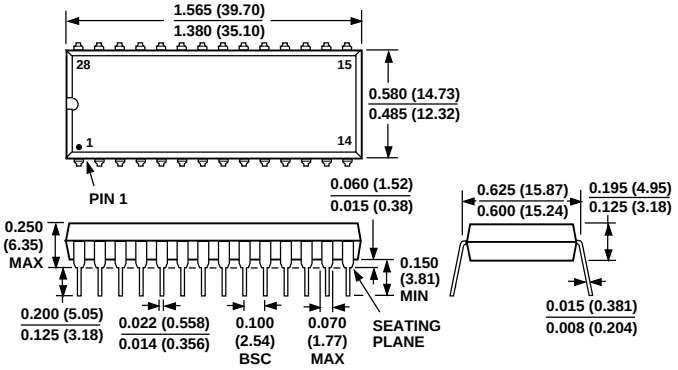


Figure 30. Power Supply Decoupling

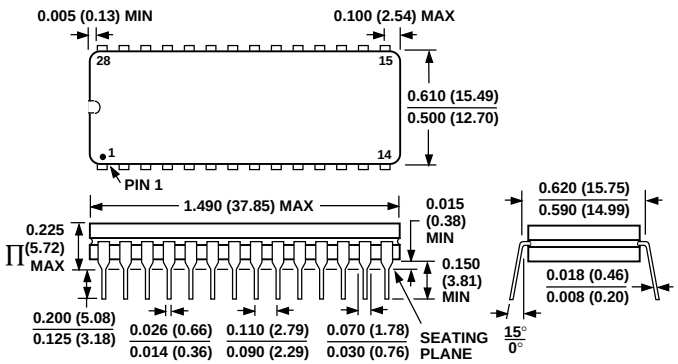
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

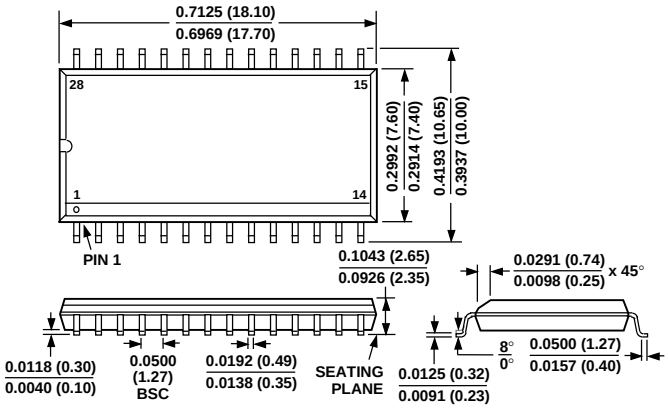
28-Leaded Plastic DIP (N-28)



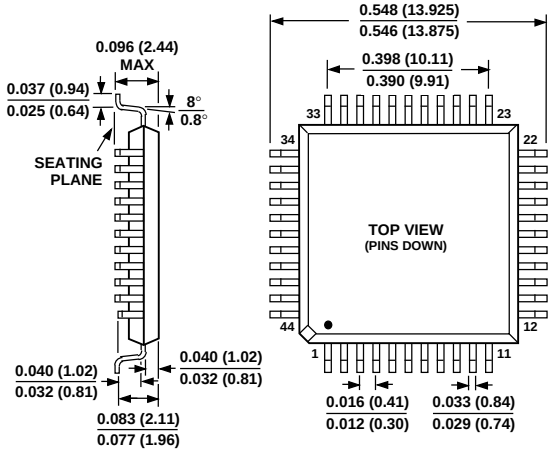
28-Leaded Cerdip (Q-28)



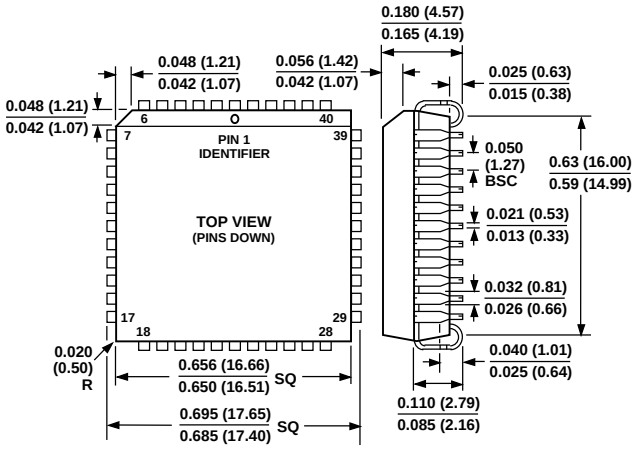
28-Leaded SOIC (R-28)



44-Pin PQFP (S-44)



44-Pin PLCC (P-44A)



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