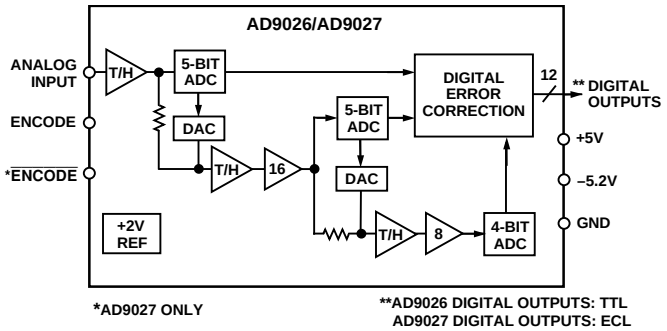
High Speed 12-Bit Monolithic A/D Converters

AD9026/AD9027

FEATURES
25.6 MSPS and 31 MSPS Grades
On-Chip T/H and Reference
1.65 Watt Power Dissipation
75 dBc Spurious-Free Dynamic Range
TTL and ECL Logic Versions

APPLICATIONS
Cellular Base Stations
Communications Receivers
Radar Receivers
Spectrum Analyzers
Electro-optics
Medical Imaging

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9026 and AD9027 are high speed, high performance, monolithic 12-bit analog-to-digital converters. All necessary functions, including track-and-hold (T/H) and reference are included on chip to provide complete conversion solutions. The AD9026 features TTL logic for digital inputs and outputs; the AD9027 uses ECL logic including differential ECL encode. Both the TTL and ECL converters are available at 25.6 Msps (A grade) and 31 Msps (B grade) production tested encode rates.

The on-chip T/H has a 150 MHz input bandwidth and is designed to provide good dynamic performance for input frequencies above Nyquist. This feature is necessary for IF-to-digital conversion applications in which the A/D converter is used in an undersampling mode. In addition, wide spurious-free dynamic range over the entire Nyquist bandwidth makes the AD9026 and AD9027 well suited for multichannel transceiver applications; both 31 Msps converters can digitize bandwidths up to 15 MHz.

The AD9026 and AD9027 are built on a trench isolated bipolar process and use an innovative multipass architecture (see Functional Block Diagram). Both parts are packaged in a 28-pin ceramic DIP; the custom cofired ceramic package forms a multilayer substrate to which internal bypass capacitors and the ADC die are attached. Both the AD9026 and the AD9027 are specified to operate over the industrial (–25°C to +85°C measured at case) temperature range.

PRODUCT HIGHLIGHTS

1. At 31 Msps (B grade devices) conversion rate, the converters can digitize 15 MHz of spectrum.
2. On-chip T/H provides > 70 dB spurious-free dynamic range over entire Nyquist band.
3. On-chip reference sets a 2.048 V p-p input voltage range centered at 0 V.
4. AD9026 outputs connect directly to TTL logic; no ECL-to-TTL chips required.
5. AD9027 ECL outputs offer lowest noise alternative for system designs that prefer reduced output voltage swings.

REV. 0

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AD9026/AD9027–SPECIFICATIONS

DC SPECIFICATIONS ($+V_S$ = +5 V, $-V_S$ = –5.2 V unless otherwise noted)

Parameter	Temp	Test Level	AD9026AD/BD Min	AD9026AD/BD Typ	AD9026AD/BD Max	AD9027AD/BD Min	AD9027AD/BD Typ	AD9027AD/BD Max	Units
RESOLUTION			12			12			Bits
DC ACCURACY									
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	25		5	25	mV
	Full	VI		15	35		15	35	mV
Gain Error	+25°C	I		0.5	5.0		0.5	5.0	% FS
	Full	VI		0.5	5.5		0.5	5.5	% FS
Thermal Noise[1]	+25°C	V		0.7			0.7		LSB rms
ANALOG INPUT									
Input Voltage Range				±1.024			±1.024		V
Input Resistance	Full	IV	225	300	375	225	300	375	Ω
Input Capacitance	+25°C	V		7			7		pF
ENCODE INPUT									
Logic Compatibility				TTL			ECL		
Logic "1" Voltage	Full	VI	2			–1.1			V
Logic "0" Voltage	Full	VI			0.8			–1.5	V
Logic "1" Current	Full	VI		7	20		3	10	µA
Logic "0" Current	Full	VI		7	20		3	10	µA
Input Capacitance	+25°C	V		4			4		pF
DIGITAL OUTPUTS[2]									
Logic Compatibility				TTL			ECL		
Logic "1" Voltage	Full	VI	2.4			–1.1			V
Logic "0" Voltage	Full	VI			0.5			–1.5	V
Output Coding				Offset Binary			Offset Binary		
POWER SUPPLY									
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	V
$+V_S$ Supply Current	Full	VI		120	142		110	130	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	V
$-V_S$ Supply Current	Full	I		205	248		215	260	mA
Power Dissipation[3]	Full	VI		1.65	2.0		1.65	2.0	W
Power Supply Rejection Ratio (PSRR)[4]	Full	VI		20	55		20	55	mV/V

NOTES
[1]ANALOG INPUT is connected to ground.
[2]AD9026AD/BD: outputs sourcing 1 mA when V_{OH} is measured and sinking 2 mA when V_{OL} is measured. AD9027 outputs are terminated with 2 kΩ resistors to $-V_S$.
[3]Does not include power dissipated in termination resistors.
[4]$+V_S$ and $-V_S$ varied independently ±5% from nominal; PSRR in specification table is either PSRR ($+V_S$) or PSRR ($-V_S$), whichever is worse.
Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 25.6 MSPS for A Grade Parts; Encode = 31.0 MSPS for B Grade Parts unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9026AD Min	AD9026AD Typ	AD9026AD Max	AD9026BD Min	AD9026BD Typ	AD9026BD Max	AD9027AD Min	AD9027AD Typ	AD9027AD Max	AD9027BD Min	AD9027BD Typ	AD9027BD Max	Units
Maximum Conversion Rate	Full	VI	25.6			31			25.6			31			MSPS
Minimum Conversion Rate	+25°C	V		4			4			4			4		MSPS
Aperture Delay (t_A)	+25°C	V		3			3			3			3		ns
Aperture Uncertainty (Jitter)	+25°C	V		2			2			2			2		ps rms
ENCODE Pulse Width High	+25°C	IV	14			14			14			14			ns
ENCODE Pulse Width Low	+25°C	IV	14			14			14			14			ns
Output Delay (t_{OD})	Full	IV	13		23	13		23	10		18	10		18	ns

Specifications subject to change without notice.

AC SPECIFICATIONS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; Encode = 25.6 MSPS (50% duty cycle) for A Grade Parts; Encode = 31.0 MSPS (50% duty cycle) for B Grade Parts unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9026AD Min	AD9026AD Typ	AD9026AD Max	AD9026BD Min	AD9026BD Typ	AD9026BD Max	AD9027AD Min	AD9027AD Typ	AD9027AD Max	AD9027BD Min	AD9027BD Typ	AD9027BD Max	Units
AC ACCURACY															
Differential Nonlinearity	+25°C	I		0.25	0.75		0.4	0.75		0.25	0.75		0.4	0.75	LSB
	Full	VI			1.0			1.0			1.0			1.0	LSB
Integral Nonlinearity	+25°C	I		1.2	2.5		1.2	2.5		1.2	2.5		1.2	2.5	LSB
	Full	VI		1.25	3.0		1.25	3.0		1.25	3.0		1.25	3.0	LSB
ANALOG INPUT BANDWIDTH	+25°C	V		150			150			150			150		MHz
TRANSIENT RESPONSE	+25°C	V		10			10			10			10		ns
OVERVOLTAGE RECOVERY	+25°C	V		10			10			10			10		ns
SFDR[1]															
Analog Input @ 1.2 MHz	+25°C	I	70	77		70	77		70	77		70	77		dBc
	Full	VI	68	75		68	75		68	75		68	75		dBc
9.6 MHz	+25°C	I	70	76		70	75		70	76		70	76		dBc
	Full	VI	68	74		68	73		68	74		68	74		dBc
13.4 MHz	+25°C	I	70	75		65	72		70	75		70	74		dBc
	Full	VI	68	73		63	70		68	73		68	72		dBc
SINAD[2]															
Analog Input @ 1.2 MHz	+25°C	I	61	65		60	63		62	65		61	65		dB
	Full	VI	60	64		59	62		61	64		60	64		dB
9.6 MHz	+25°C	I	60	64		59	62		61	65		60	64		dB
	Full	VI	59	63		58	61		60	64		59	63		dB
13.4 MHz	+25°C	I	59	63		57	61		61	64		60	64		dB
	Full	VI	58	62		56	60		60	63		59	63		dB
SNR[3]															
Analog Input @ 1.2 MHz	+25°C	I	62	65		61	64		63	65		62	65		dB
	Full	VI	61	64		60	63		62	64		61	64		dB
9.6 MHz	+25°C	I	61	64		60	63		62	65		61	65		dB
	Full	VI	60	63		59	62		61	64		60	64		dB
13.4 MHz	+25°C	I	60	63		59	62		62	65		61	65		dB
	Full	VI	59	62		58	61		61	64		60	64		dB
Two-Tone IMD Rejection[4]															
F1 = 8.1 MHz; F2 = 9.6 MHz	+25°C	I	75	83		75	83		75	85		75	85		dBc
Two-Tone SFDR[5]															
F1 = 8.1 MHz; F2 = 9.6 MHz	+25°C	I	68	75		68	75		68	75		68	75		dBc

NOTES
[1]Analog Input signal power at –1 dBFS; spurious-free dynamic range (SFDR) is the ratio of the signal level to worst spur, usually limited by harmonics.
[2]Analog Input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics.
[3]Analog Input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed).
[4]Both input tones at –7 dBFS; two tone intermodulation distortion (IMD) rejection is the ratio of either tone to the worst 3rd order intermod product.
[5]Both input tones at –7 dBFS; two tone spurious-free dynamic range (SFDR) is the ratio of either tone to the worst spurious signal.
Specifications subject to change without notice.

WAFER TEST LIMITS[1] ($+V_S$ = +5 V, $-V_S$ = –5.2 V unless otherwise noted)

Parameter	AD9026CHIPS Min	AD9026CHIPS Typ	AD9026CHIPS Max	AD9027CHIPS Min	AD9027CHIPS Typ	AD9027CHIPS Max	Units
POWER SUPPLY							
$+V_S$ Supply Current	100		140	90		128	mA
$-V_S$ Supply Current	160		246	180		258	mA
ENCODE INPUT							
Logic "1" Current			20			10	µA
Logic "0" Current			20			10	µA
ANALOG INPUT							
Input Resistance	225		375	225		375	Ω
DC ACCURACY							
Offset Error	–20		20	–20		20	mV
Gain Error	–4.5		4.5	–4.5		4.5	% FS
No Missing Codes		Guaranteed			Guaranteed		
Differential Nonlinearity	–0.65		0.65	–0.65		0.65	LSB

NOTES
[1]Electrical test is performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice.
[2]Die substrate is connected to $-V_S$.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
$+V_S$	0	+6	V
$-V_S$	–6	0	V
Analog Input	–1.5	+1.5	V
Digital Inputs			
AD9026 (TTL Logic)	0	$+V_S$	V
AD9027 (ECL Logic)	$-V_S$	0	V
Digital Output Current			
AD9026 (TTL Logic)		12	mA
AD9027 (ECL Logic)		12	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Case)	–25	+85	°C
Maximum Junction Temperature		+175	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES

[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2]Typical thermal impedances for "D" package (custom ceramic 28-pin DIP): θ_{JC} = 14°C/W; θ_{JA} = 34°C/W

EXPLANATION OF TEST LEVELS

Test Level

I. 100% Production Tested.

II. 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample Tested Only.

IV. Parameter is guaranteed by design and characterization testing.

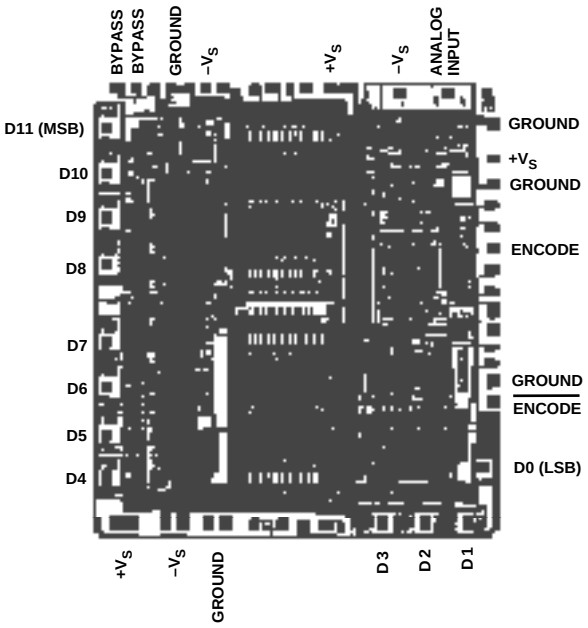
V. Parameter is a typical value only.

VI. All devices are 100% production tested at +25°C; sample tested at temperature extremes.

DIE LAYOUT AND MECHANICAL INFORMATION

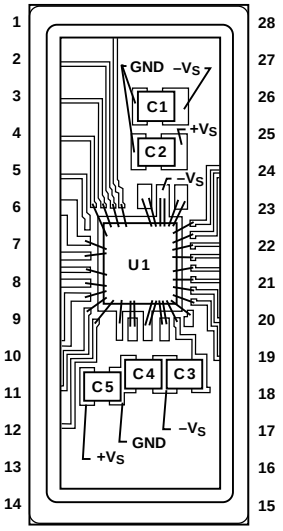
Die Dimensions . . . . . 205 × 228 × 21 (±1) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Transistor Count 4,336
Passivation . . . . . Oxynitride
Die Attach . . . . . Silver Filled
Bond Wire . . . . . Gold

DIE PHOTO/ PAD LABELS



AD9026/AD9027 CUSTOM PACKAGE

CUSTOM 28-PIN COFIRED CERAMIC MULTILAYER DUAL INLINE PACKAGE. (TOP LAYER METALLIZATION SHOWN)

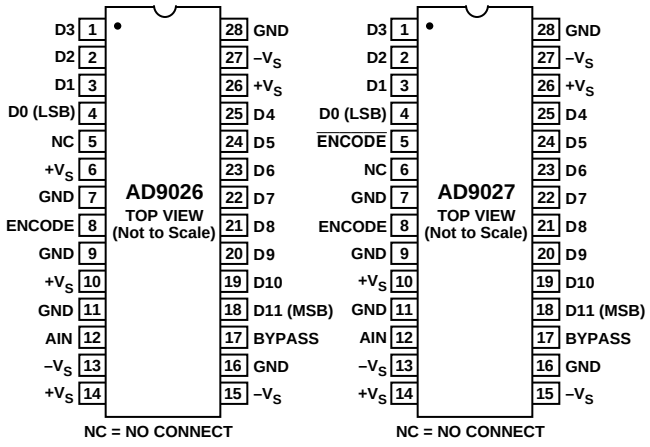


NOTES:
C1 & C4 ARE $-V_S$ SUPPLY DECOUPLING CAPS.
C2 & C5 ARE $+V_S$ SUPPLY DECOUPLING CAPS.
C3 IS A BYPASS CAP FOR INTERNAL DAC REFERENCE.
U1 SUBSTRATE IS TIED TO $-V_S$.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9026/AD9027 features ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESIGNATIONS



BYPASS (PIN 17) SHOULD BE CONNECTED TO $-V_S$ (PIN 15) THROUGH 0.1µF CAP

ORDERING GUIDE

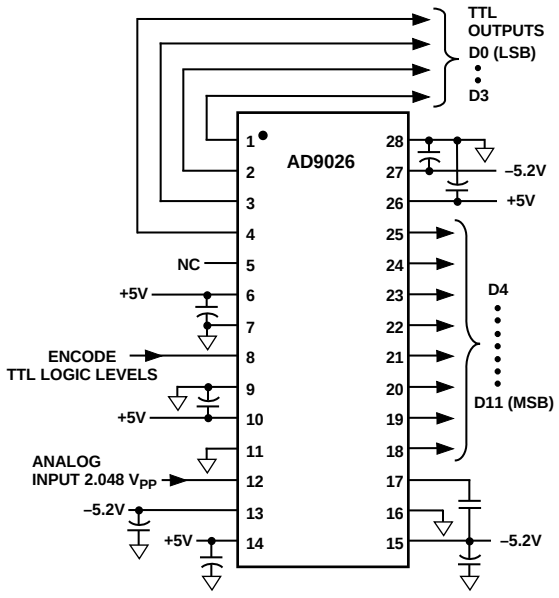
Model	Temperature Range	Package Description
AD9026AD	–25°C to +85°C (Case)	28-Pin 600 mil Hermetic Ceramic DIP (DH-28)
AD9026BD	–25°C to +85°C (Case)	28-Pin 600 mil Hermetic Ceramic DIP (DH-28)
AD9026CHIPS		Unpackaged Die
AD9026/PCB-T		Evaluation Board with AD9026BD
AD9027AD	–25°C to +85°C (Case)	28-Pin 600 mil Hermetic Ceramic DIP (DH-28)
AD9027BD	–25°C to +85°C (Case)	28-Pin 600 mil Hermetic Ceramic DIP (DH-28)
AD9027CHIPS		Unpackaged Die
AD9027/PCB-E		Evaluation Board with AD9027BD

PIN DESCRIPTIONS

Pin No.	Name	Function
1–3	D3–D1	Digital Output Bits.
4	D0 (LSB)	Digital Output Bit (Least Significant Bit).
5*	NC	No connection internally on AD9026.
	$\overline{\text{ENCODE}}$	Complement of encode clock input on AD9027.
6*	$+V_S$	+5 V power supply on AD9026.
	NC	No connection internally on the AD9027.
7	GND	Ground.
8	ENCODE	Encode Clock Input. Conversion initiated on rising edge of clock.
9	GND	Ground.
10	$+V_S$	+5 V power supply.
11	GND	Ground.
12	AIN	Analog Input.
13	$-V_S$	–5.2 V power supply.
14	$+V_S$	+5 V power supply.
15	$-V_S$	–5.2 V power supply.
16	GND	Ground.
17	BYPASS	Connect to $-V_S$ through 0.1 µF capacitor.
18	D11 (MSB)	Digital Output Bit (Most Significant Bit).
19–25	D10–D4	Digital output bits.
26	$+V_S$	+5 V power supply.
27	$-V_S$	–5.2 V power supply.
28	GND	Ground.

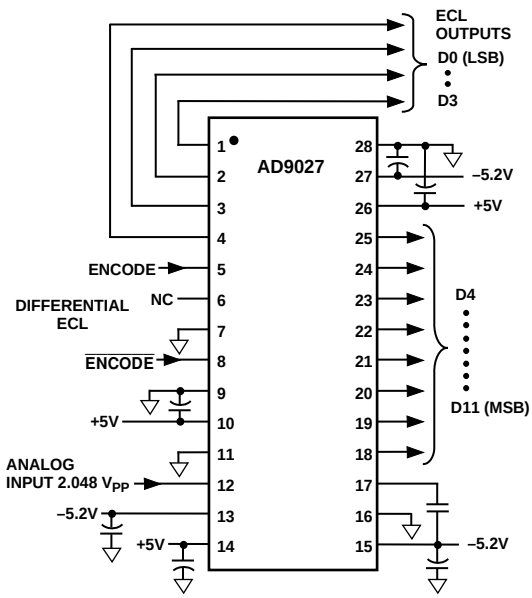
*Pin descriptions for the AD9026 and AD9027 are identical with the exception of Pins 5 and 6.

AD9026 Basic Hook-Up



1. ALL DECOUPLING/BYPASS CAPACITORS ARE 0.1µF
2. NC = NOT CONNECTED

AD9027 Basic Hook-Up



1. ALL DECOUPLING/BYPASS CAPACITORS ARE 0.1µF
2. NC = NOT CONNECTED
3. TERMINATE ECL OUTPUTS WITH 2kΩ to –5.2V

DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.2% accuracy after an analog input signal 150% of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

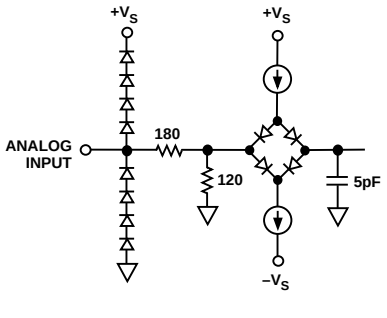
Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Transient Response
The time required for the converter to achieve 0.2% accuracy when a one-half full-scale step function is applied to the analog input.

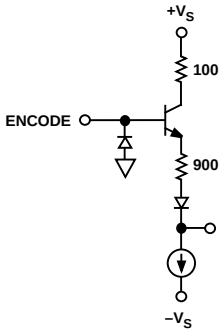
Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

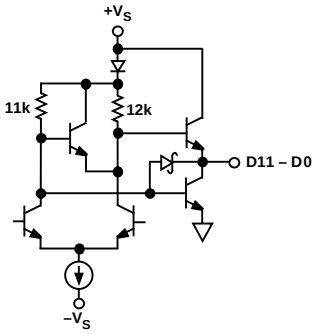
EQUIVALENT CIRCUITS



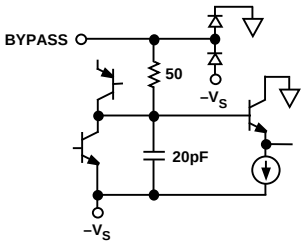
Analog Input Stage



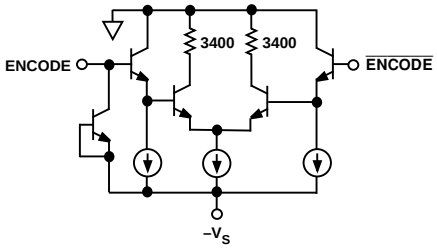
AD9026 Encode Input



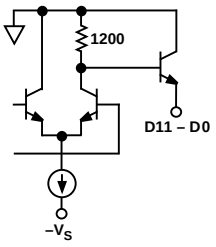
AD9026 Output Stage



Bypass



AD9027 Encode Input



AD9027 Output Stage

Typical AD9026 Performance

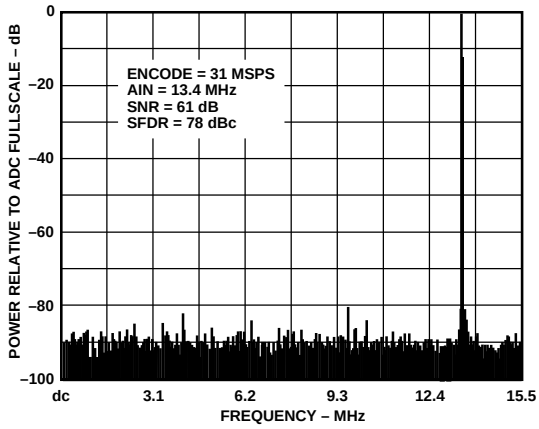


Figure 1. Single Tone at 13.4 MHz

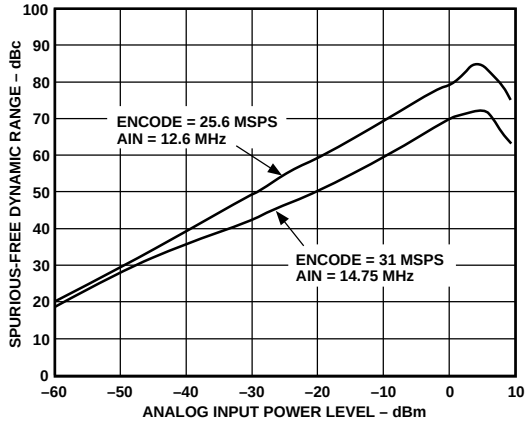


Figure 4. SFDR vs. Analog Input Level

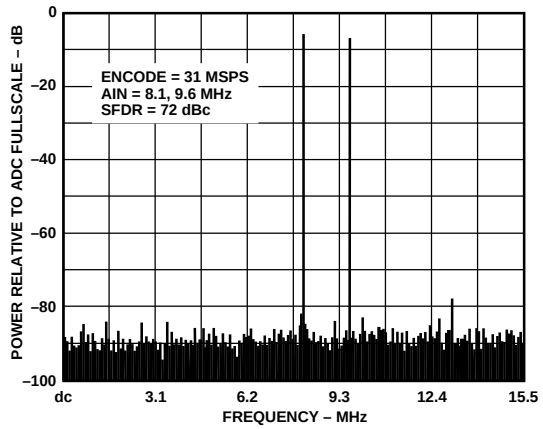


Figure 2. Two Tones @ 8.1 MHz & 9.6 MHz

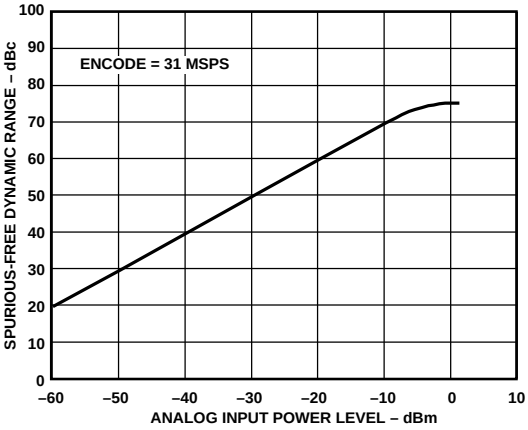


Figure 5. Two-Tone SFDR vs. Analog Input Level

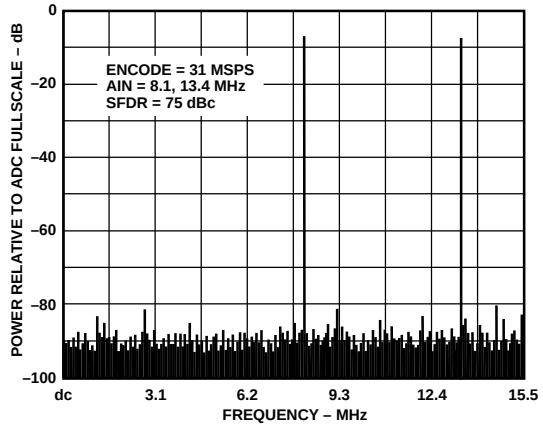


Figure 3. Two Tones @ 8.1 MHz & 13.4 MHz

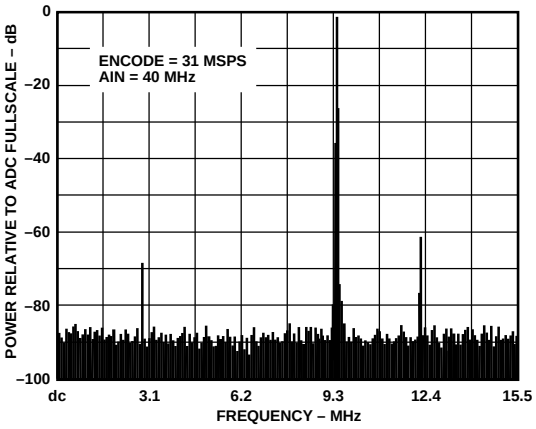


Figure 6. Undersampling a 40 MHz Input Tone

Typical AD9027 Performance

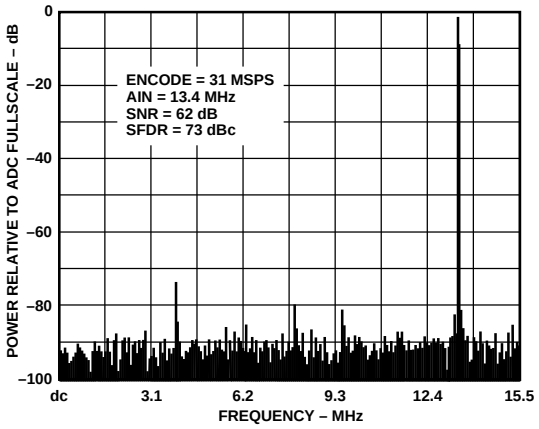


Figure 7. Single Tone at 13.4 MHz

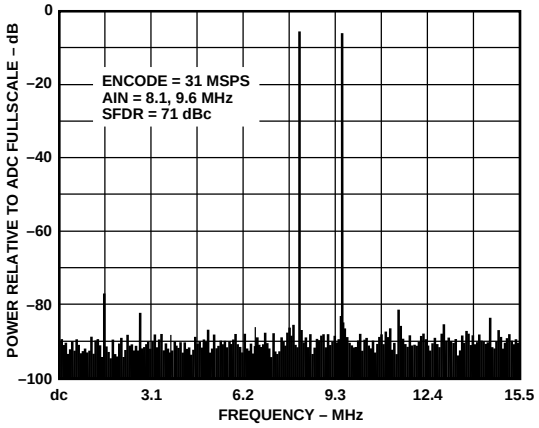


Figure 8. Two Tones @ 8.1 MHz & 9.6 MHz

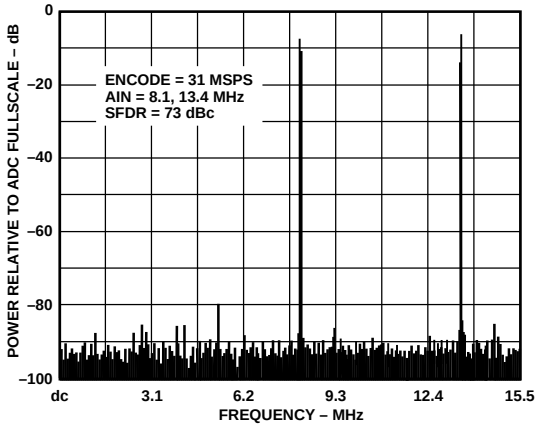


Figure 9. Two Tones @ 8.1 MHz & 13.4 MHz

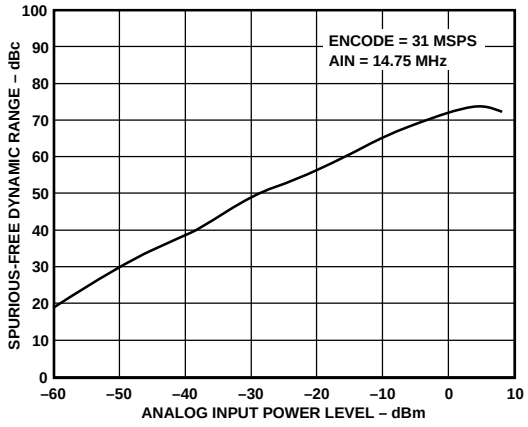


Figure 10. SFDR vs. Analog Input Level

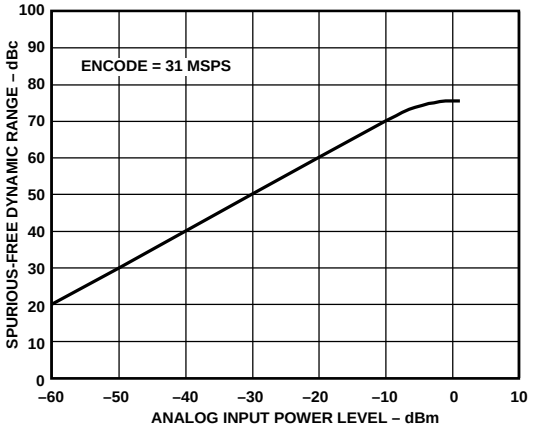


Figure 11. Two-Tone SFDR vs. Analog Input Level

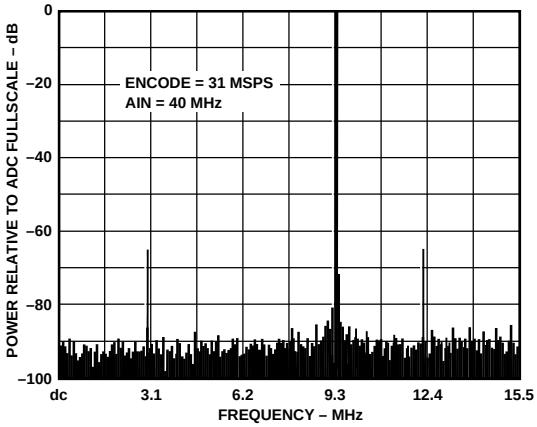


Figure 12. Undersampling a 40 MHz Input Tone

Typical AD9026 Performance

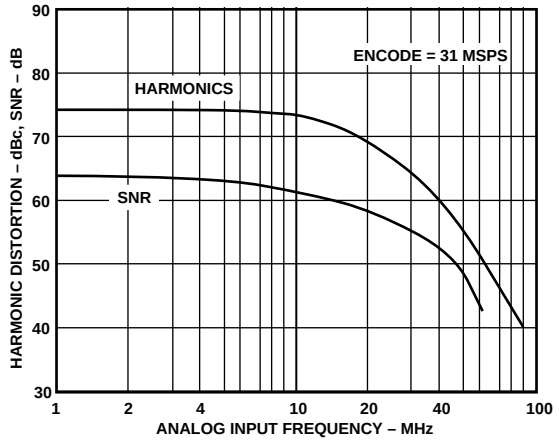


Figure 13. Noise and Distortion vs. AIN Frequency

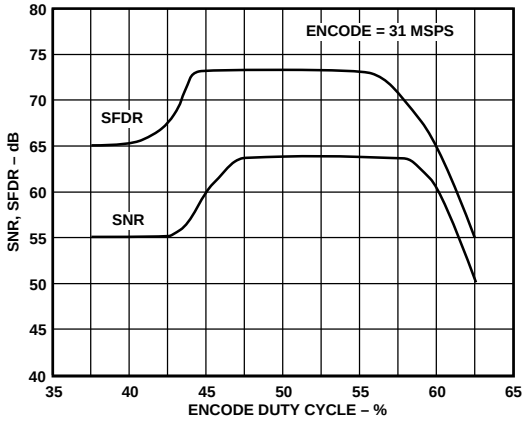


Figure 14. SNR , SFDR vs. Encode Duty Cycle

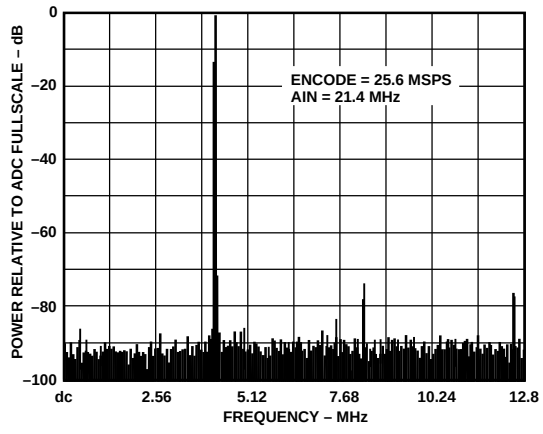


Figure 15. Undersampling a 21.4 MHz Input Tone

Typical AD9027 Performance

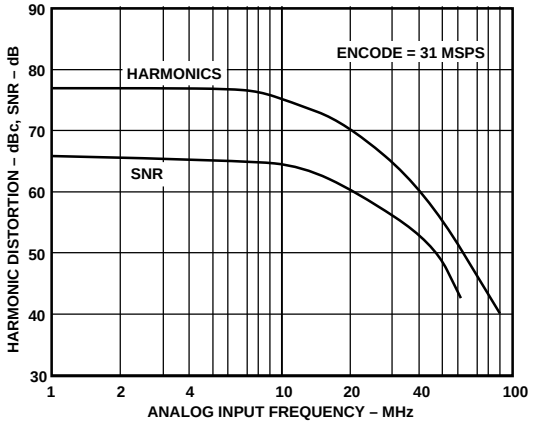


Figure 16. Noise and Distortion vs. AIN Frequency

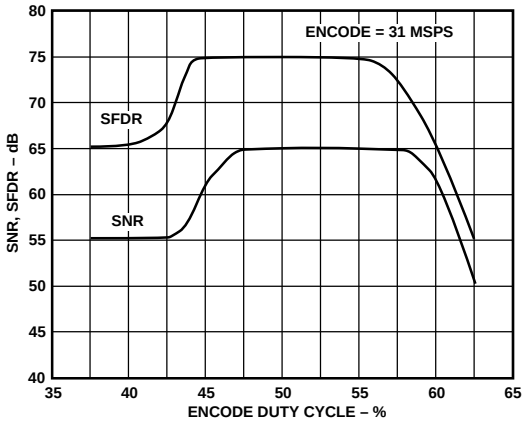


Figure 17. SNR, SFDR vs. Encode Duty Cycle

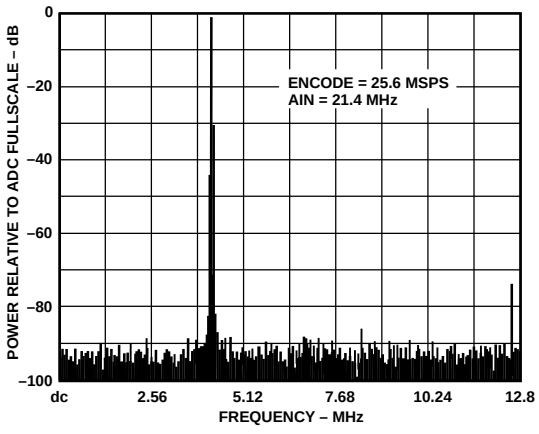


Figure 18. Undersampling a 21.4 MHz Input Tone

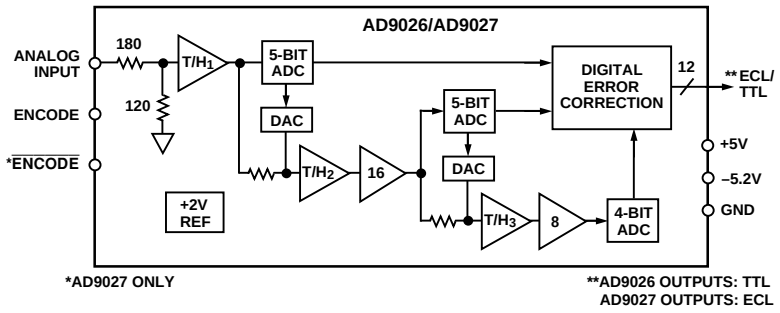


Figure 19. AD9026/AD9027 Functional Block Diagram

THEORY OF OPERATION

The AD9026/AD9027 analog-to-digital converters (ADCs) employ a three-pass subranging architecture and digital error correction. This combination of design techniques ensures 12-bit accuracy at relatively low power.

As shown in Figure 19, analog input signals are immediately attenuated through a resistor divider and applied directly to the sampling bridge of a track-and-hold (T/H). The rising edge of the ENCODE pulse places this first track-and-hold, T/H_1, into hold mode. The held value of T/H_1 is applied to a 5-bit flash ADC. The 5-bit converter resolves the most significant bits (MSBs) of the held analog voltage. These five bits are reconstructed by a 5-bit digital-to-analog converter (DAC) and subtracted from T/H_1's output to form a residual signal. Note that the reconstruction DAC has a resolution of 5 bits but must maintain 12-bit accuracy.

A second track-and-hold, T/H_2, holds the amplified residue signal while it is encoded by a second 5-bit flash ADC. These five bits are reconstructed and subtracted from T/H_2's output to form a second residual signal. A third and final track-and-hold, T/H_3, precedes a gain stage which in turn drives a 4-bit flash ADC.

Digital error correction logic corrects and aligns the data from the three flash converters and presents the result as a 12-bit parallel digital word. In the case of the AD9026, the digital output stage provides TTL logic levels; the AD9027 parallel output provides ECL logic levels.

APPLYING THE AD9026/AD9027

Timing

Conversion is initiated by asserting a logic "high" state on the ENCODE command for both the AD9026 and AD9027 converters, as shown in Figure 20. The digital output data which corresponds to a given encode rising edge is available after two pipeline delays and one propagation delay.

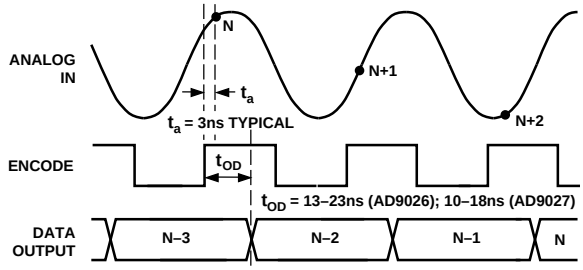


Figure 20. Timing Diagram

Internally, the encode clock is delayed and gated to generate all of the timing necessary for data conversion. The allocation of hold and acquisition time for the first track-and-hold is critical and is affected by the duty cycle of the encode clock. Performance is optimized for encode duty cycles of 50%. Duty cycle variations that exceed 50 ± 5% will negatively impact performance at 31 Msps (see Performance Curves for detail).

Operation at encode rates less than 4 Msps is not recommended. At these low encodes, the internal T/Hs will droop out of error correction range and cease to function properly. For the same reason, burst mode operation at the ENCODE pin is not recommended. If burst mode is required, gate the digital output data instead of the encode to the ADC; do not leave the ENCODE pin in a static "logic high" state.

Encoding the AD9026

Care should be taken when selecting drive logic for this single-ended TTL-compatible input. Fast, clean, symmetrical output swings with low jitter will yield optimal performance.

Gates from the "LS" logic family are not recommended because of their extreme differences in rising versus falling characteristics.

"AC" logic on the other hand, is too fast with excessive drive capability, and tends to couple clock noise into the converter's first T/H stage. "AS" logic offers the best compromise of the TTL families evaluated, but optimal performance was achieved with AD969X family of TTL comparators (see AD9026/PCB-T schematic).

Encoding the AD9027

A differential ECL encode is required for the AD9027: ENCODE (Pin 8), $\overline{\text{ENCODE}}$ (Pin 5). This signal should be "clean" and fast, with a minimum amount of jitter. Such a signal may be generated by using a spectrally pure low phase noise sine wave to drive an AD96687 ECL comparator (see AD9027/PCB-E schematic).

Analog Input

The analog input (Pin 12) voltage range is nominally ±1.024 V. The range is set with an internal voltage reference and cannot be adjusted by the user. The input resistance is 300 Ω, and the analog small signal bandwidth is 150 MHz, making the AD9026 and AD9027 suitable for undersampling applications. Sample FFTs of 40 MHz large signal inputs can be found in the Performance section (Figures 6, 12).

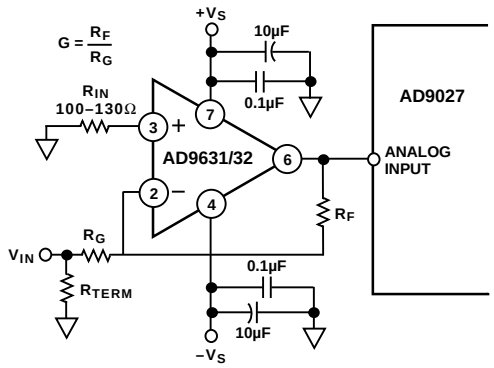


Figure 21. Low Distortion Drive Circuit for AD9026/AD9027

Driving the Analog Input

Special care must be taken to ensure that the analog input signal is not compromised before it reaches the ADC. Any required filtering should be done as close to the AD9026/AD9027 as possible, and away from any digital lines.

In systems that have impedance matching problems or require gain before the converter, a low noise, low distortion, wideband op amp may be used. Typically this amplifier will degrade overall performance, but this degradation will be minimal if the correct amplifier is selected.

Figure 21 shows the ultralow distortion, wide bandwidth AD9631 driving an AD9027 converter at a gain of –1. This amplifier/ADC combination maintains >70 dB harmonic distortion over the Nyquist band. The low output impedance of the AD9631 also reduces drive circuitry sensitivity to the small current spikes that can come from an ADC's internal track-and-hold.

Power Supplies

The power supplies of the AD9026 and AD9027 should be isolated from the supplies used for noisy devices (digital logic especially) to reduce the amount of noise coupled into the ADC. For optimum performance, linear supplies ensure that switching noise from the supplies does not introduce distortion products during the encoding process. If switching supplies *must* be used, decoupling recommendations should be observed.

Layout Information

Preserving the accuracy and dynamic performance of the AD9026 and AD9027 requires that designers pay special attention to layout of the printed circuit board.

Analog paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input connection should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section. Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. The AD9026 and AD9027 outputs should be buffered or latched close to the device (<2 cm). This prevents load transients which may feed back into the device.

In high speed circuits, layout of the ground is critical. A single low impedance ground plane on the component side of the board is the minimum requirement (an internal ground plane is preferred). Power supplies should be capacitively coupled to the ground plane with high quality 0.1 µF chip capacitors to reduce noise in the circuit. All power pins of the AD9026 and AD9027 should be bypassed individually. The bypass pin (BYPASS Pin 17) should be connected to the $-V_S$ supply (Pin 15) through a 0.1 µF chip capacitor as close to the part as possible.

Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance return paths. In systems with dedicated analog and digital grounds, all grounds for the AD9026 and AD9027 should be connected to the analog ground plane.

In systems using multilayer boards, dedicated power planes are recommended to provide low impedance connections for device power. Sockets limit dynamic performance and are not recommended for use with the AD9026 or AD9027.

EVALUATING PERFORMANCE OF THE AD9026/AD9027

Noise Performance

High speed, wide bandwidth ADCs such as the AD9026 and AD9027 are optimized for dynamic performance over a wide range of analog input frequencies. Due to this wide input bandwidth, for a given analog input voltage there will be a range of output codes that may occur. This is caused by unavoidable circuit noise within the wideband circuits of the ADC. If a dc signal is applied to the ADC and several thousand outputs are recorded, a distribution of codes such as that shown in the histogram may result (Figure 22).

The correct code appears most of the time, but adjacent codes also appear with reduced probability. If a normal probability density curve is fitted to this Gaussian distribution of codes, the standard deviation will be equal to the equivalent input rms noise of the ADC. The rms input noise may also be approximated by converting the signal-to-noise ratio (SNR), as measured by a low frequency FFT, to an equivalent input noise. This method is accurate only if the SNR performance is dominated by random thermal noise (the low frequency SNR without harmonics is the best measure); 63 dB equates to 1 LSB rms for a 2 V p-p (0.707 V rms) input signal.

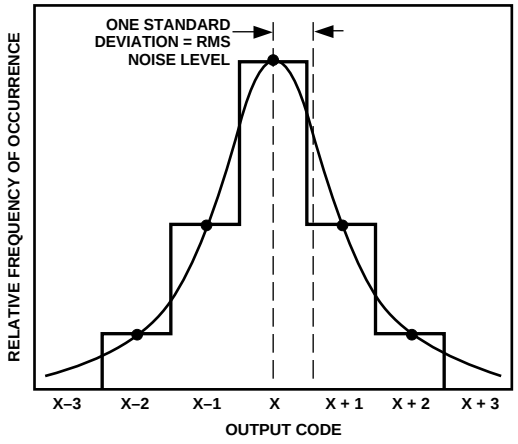


Figure 22. ADC Equivalent Input Noise

The AD9027 has approximately 0.7 LSB of rms input noise which would predict a noise-limited SNR of 66 dB. Since the actual SNR of the AD9027 is 65 dB for a 1.2 MHz input, thermal noise alone does not limit the SNR performance of the device. Differential nonlinearities, aperture uncertainty, and digital switching noise account for the additional degradation in SNR as measured at the ADC output.

Performance curves illustrate SNR vs. input frequency for the AD9026 and AD9027 at encode rates of 31 Msps (Figures 13, 16). Because the AD9026 TTL converter has larger digital output voltage swings, it tends to have slightly worse noise performance than its ECL counterpart.

For a fixed analog input frequency, reducing the encode rate on the AD9026 actually improves SNR (note specifications at 31 Msps vs. 25.6 Msps). This improvement results because the rms noise coupled to internal circuits decreases as the time between samples increases.

Performance in the Frequency Domain

The AD9026 and AD9027 were designed to minimize harmonic distortion over the entire Nyquist bandwidth. Performance curves are included which illustrate >70 dB spurious-free dynamic range (SFDR) for –1 dBFS signals from dc to 15 MHz (Figures 13 and 16).

Typically, the spurious levels generated by tones near full scale are dominated by low order harmonics generated in the converter's first track-and-hold. As the strength of the analog input signal is reduced, there is actually a slight increase in spurious-free dynamic range relative to the carrier. At approximately –7 dBFS the SFDR decreases linearly as input power is reduced (Figures 4 and 10).

Two-tone intermodulation distortion rejection was also characterized on the AD9026 and AD9027. Two tones, each at –7 dBFS, were varied in frequency to determine flatness of IMD rejection across the Nyquist band. A "Two-Tone SFDR" specification was created to distinguish between the typical level of IMD products and other spurious levels. In most cases, second order terms and direct harmonics limited Two-Tone SFDR on these converters. Third order products were typically >80 dBc (dBc indicates strength relative to the carrier), while first and second order products were >72 dBc (Figures 2, 3, 5, 8, 9, and 11).

Performance Over Temperature

Signal-to-noise ratio (SNR) is typically flat over the specified operating temperature range for both the AD9026 and AD9027 across the entire Nyquist band.

Spurious-free dynamic range (SFDR) for a given input frequency varies by a few dB over the rated operating temperature range as indicated in the specification table.

Harmonic distortion consistently increases with input frequency at the maximum operating temperature of +85°C measured at device case. For example, the SFDR of the ADC may vary from a low of 71 dBc (13.4 MHz analog in), to a high of 80 dBc (1.2 MHz analog in) at +85°C.

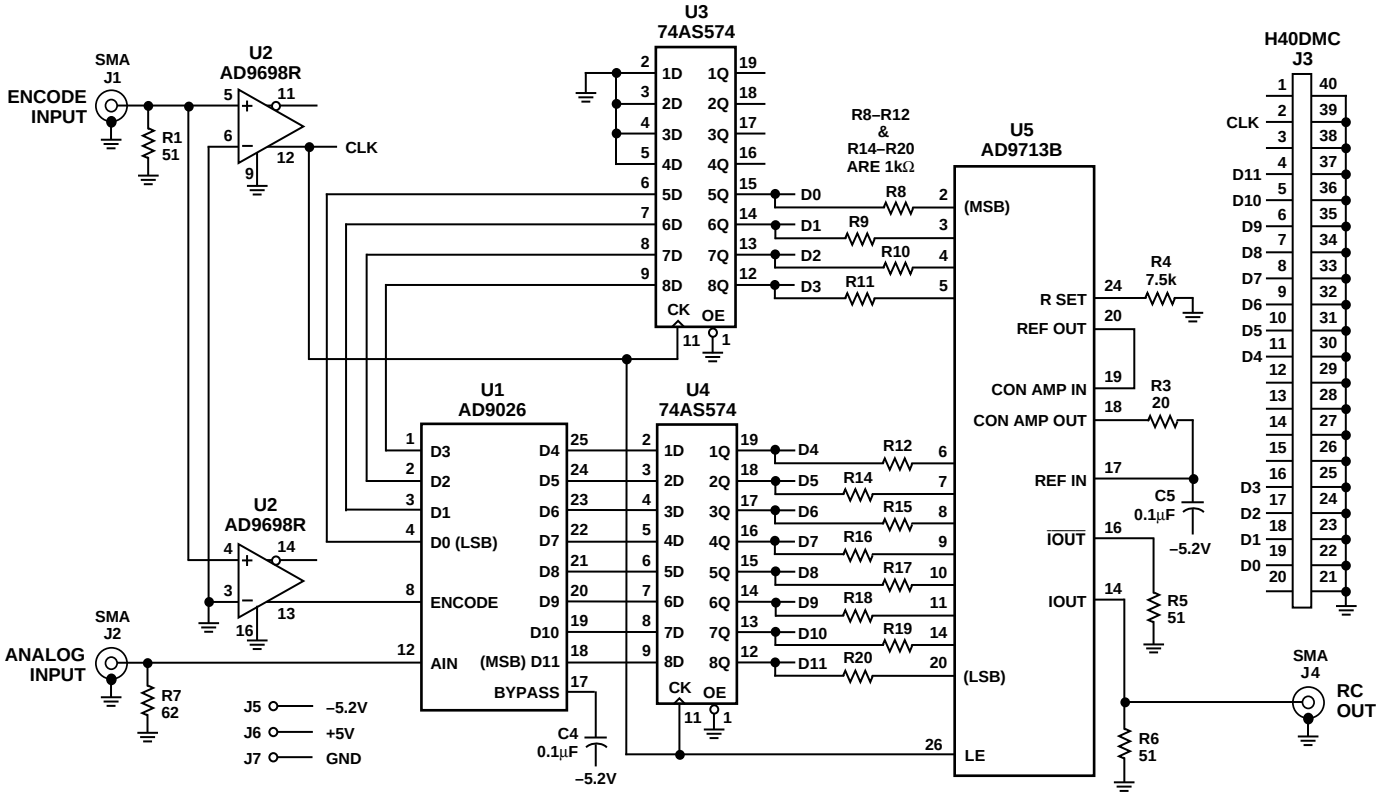


Figure 23. AD9026 Evaluation Board Schematic (AD9026/PCB-T)

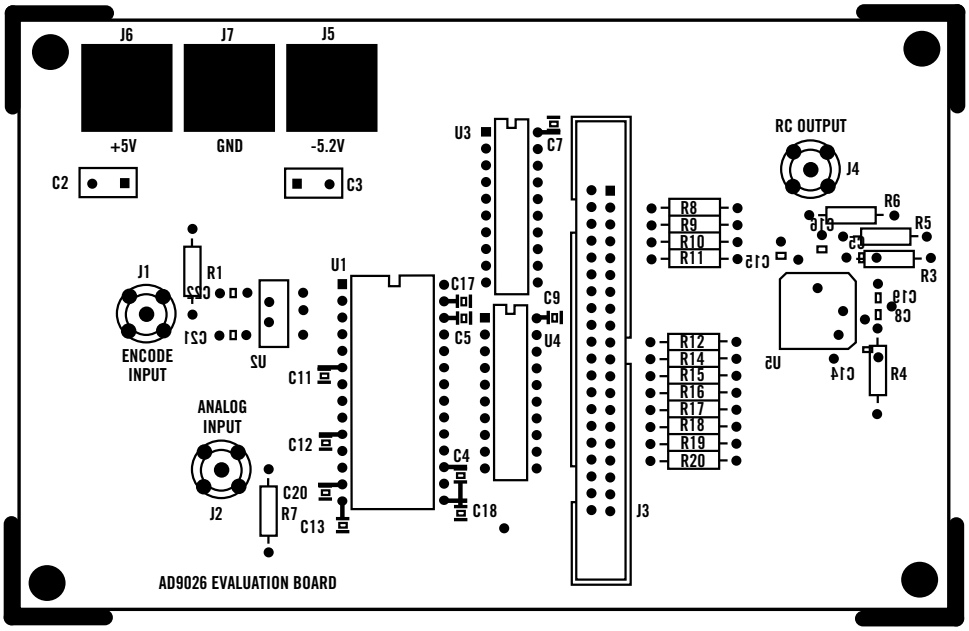


Figure 24. AD9026/PCB-T Top Side

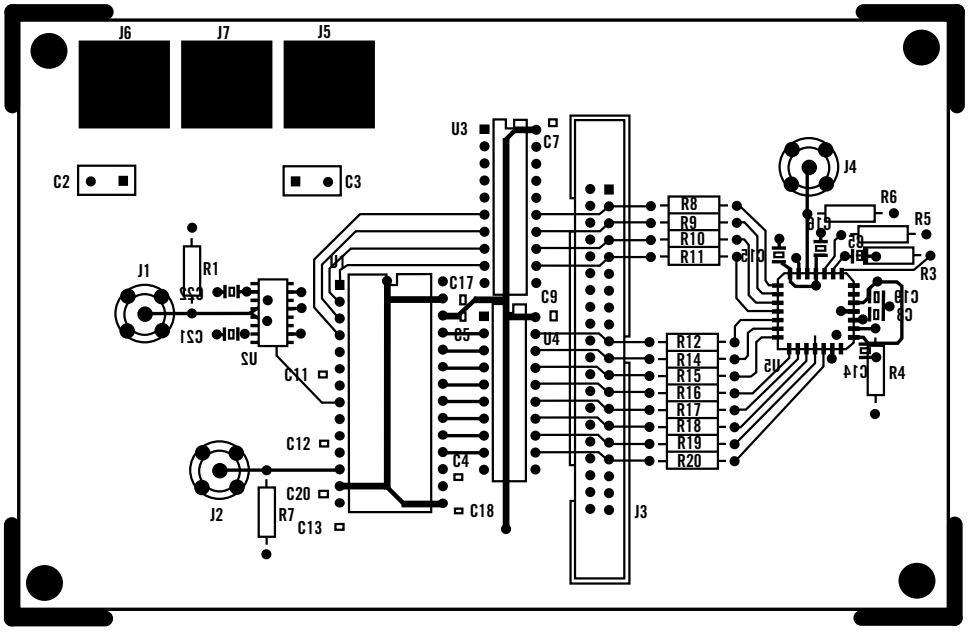


Figure 25. AD9026/PCB-T Bottom Side

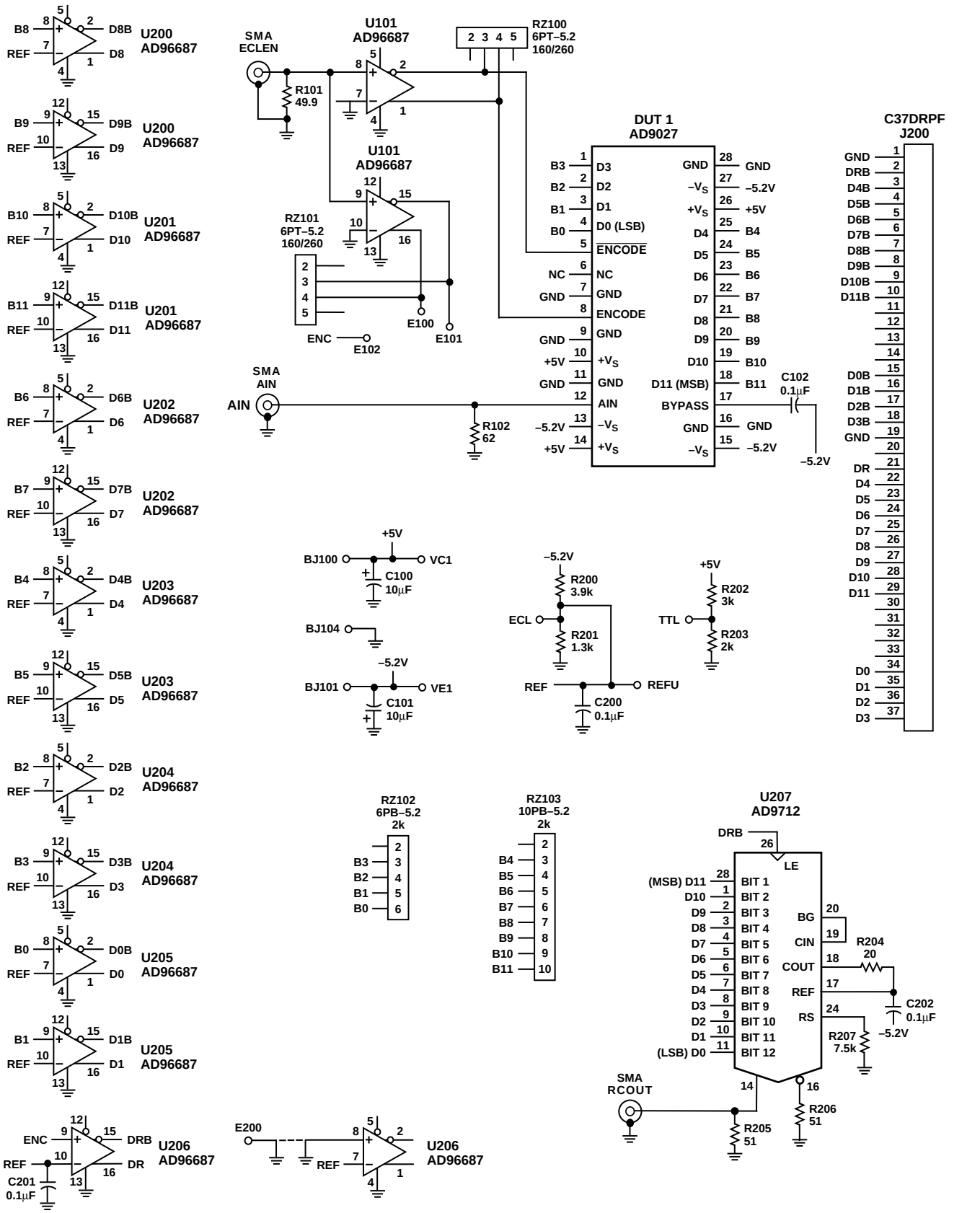


Figure 26. AD9027 Evaluation Board Schematic (AD9027/PCB-E)

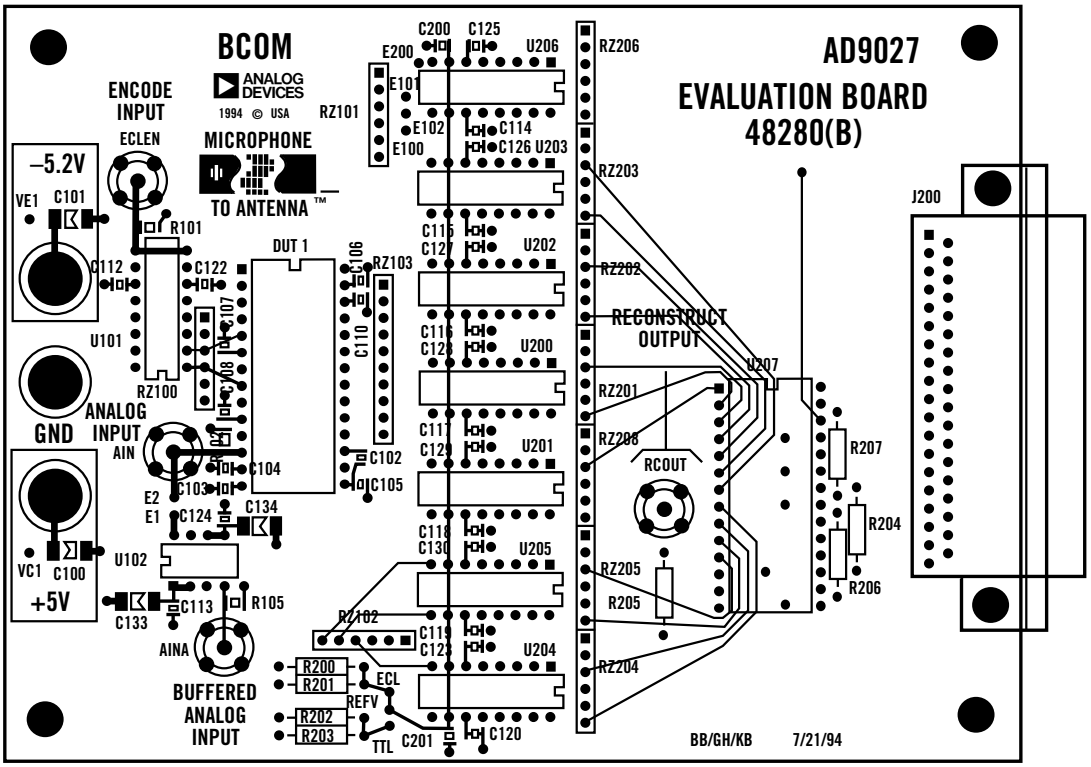


Figure 27. AD9027/PCB-E Top Side

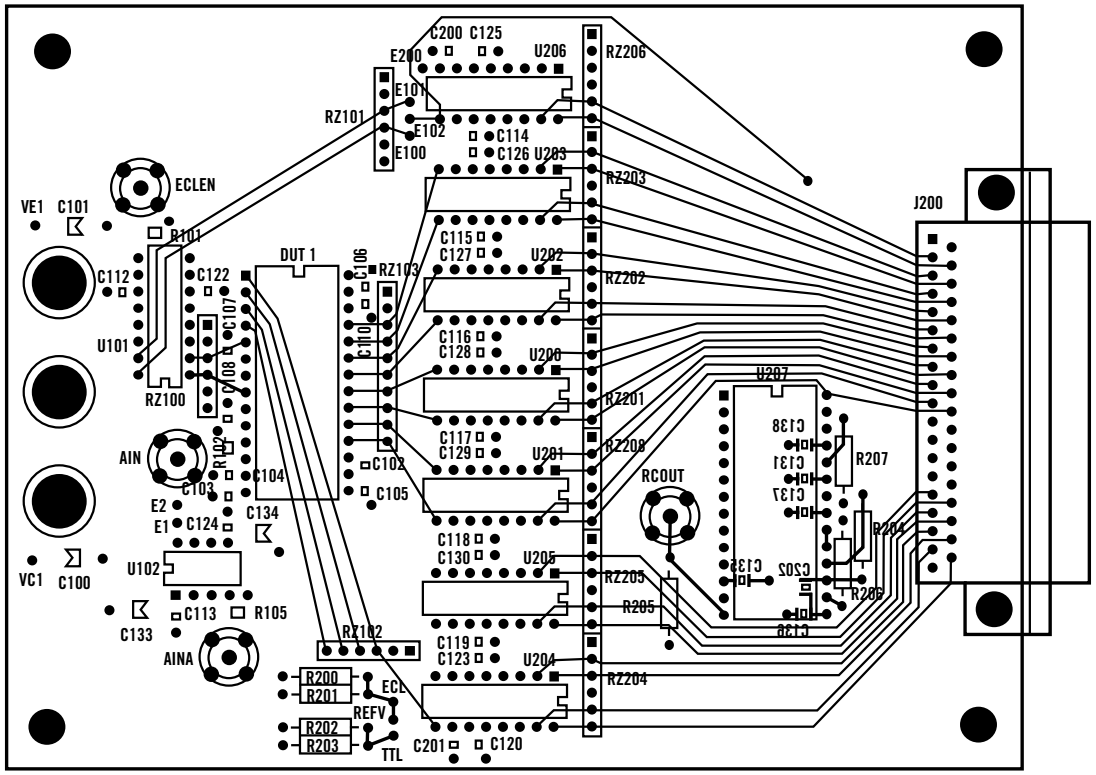
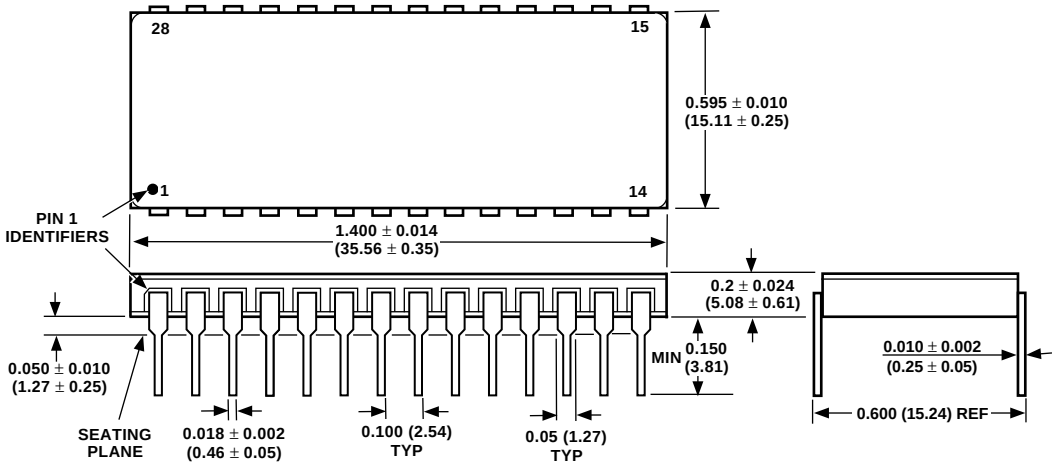


Figure 28. AD9027PCB-E Bottom Side

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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