

### FEATURES

- Data Readback Capability for System Self Check
- Fast TTL/CMOS Compatible Data Register
- $\pm 1/2$  LSB Max Linearity Error Over the Full Operating Temperature Range
- $\pm 1$  LSB Max Gain Error — No User Adjustment Required
- Less Than 0.04 LSB Max Zero Scale Error (10nA)
- Single +5V to +15V Supply
- Small 20-Pin 0.3" Wide DIP
- Improved ESD Resistance
- Latch-Up Resistant
- Adds Data Readback Feature to PM-7545 Pinout
- Available in Die Form

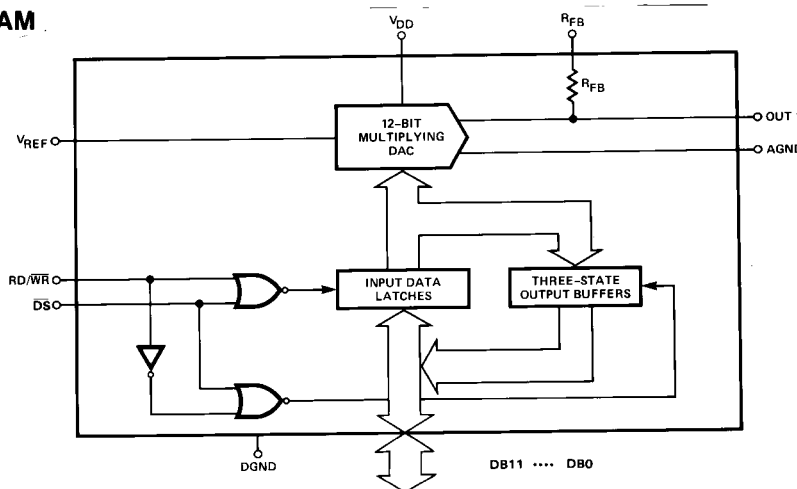
### GENERAL DESCRIPTION

The DAC-8012 is a monolithic 12-bit CMOS multiplying DAC with internal data latches and three-state data readback buffers. The latches and readback buffers perform like a "memory" location. Data loads into the latches as a single 12-bit wide word allowing direct connection to 12-bit and 16-bit busses.

Four-quadrant multiplying capability and 12-bit linearity simplifies wide-bandwidth, low-distortion, digitally-controlled precision attenuator and filter applications.

The powerful data readback function allows users to perform data path verification between the controlling processor and the DAC-8012. System self check results after writing a data word to the DAC-8012, then reading it back to the processor, verifying no change in data takes place. The readback function simplifies the design of automatic test equipment, industrial automation, robotics, and processor-controlled instrumentation. Reduction of software coding results with processors using direct memory execution instructions. In remote systems, data set-points are held in the DAC register which can be interrogated upon system fault recovery.

### FUNCTIONAL DIAGRAM



### REV. A

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### ORDERING INFORMATION †

PACKAGE: 20-PIN

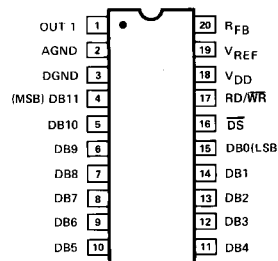
RELATIVE ACCURACY	MAXIMUM GAIN ERROR	MILITARY* TEMPERATURE	EXTENDED INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
	$T_A = +25^\circ\text{C}$ $V_{DD} = +5\text{V}$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	$0^\circ\text{C}$ to $+70^\circ\text{C}$
$\pm 1/2$ LSB	$\pm 1$ LSB	DAC8012AR	DAC8012ER	DAC8012GP
$\pm 1$ LSB	$\pm 3$ LSB	DAC8012BR	DAC8012FR	DAC8012HP
$\pm 1$ LSB	$\pm 3$ LSB	—	DAC8012FP	—
$\pm 1$ LSB	$\pm 3$ LSB	—	DAC8012FPC	—

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

‡ For availability and burn-in information on SO and PLCC packages, contact your local sales office.

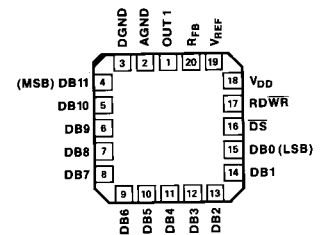
### PIN CONNECTIONS



20-LEAD PLCC (PC-Suffix)

20-PIN EPOXY DIP (P-Suffix)

20-PIN HERMETIC DIP (R-Suffix)



# DAC-8012

## ABSOLUTE MAXIMUM RATINGS

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

$V_{DD}$ to DGND .....	-0.3V, +17V
Digital Input Voltage to DGND .....	-0.3V, $V_{DD}$
AGND to DGND .....	-0.3, $V_{DD}$
$V_{RFB}$ , $V_{REF}$ to DGND .....	$\pm 25\text{V}$
$V_{PIN 1}$ to DGND .....	-0.3V, $V_{DD}$
<b>Operating Temperature Range</b>	
Military (AR, BR) Grades .....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
Industrial (ER, FR, FP, FPC) Grades .....	$-40^\circ\text{C}$ to $+85^\circ\text{C}$
Commercial (GP, HP) Grades .....	$0^\circ\text{C}$ to $+70^\circ\text{C}$
Junction Temperature .....	$+150^\circ\text{C}$
Storage Temperature .....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec) .....	$+300^\circ\text{C}$

PACKAGE TYPE	$\theta_{JA}$ (Note 1)	$\theta_{JC}$	UNITS
20-Pin Hermetic DIP (R)	76	11	$^\circ\text{C/W}$
20-Pin Plastic DIP (P)	69	27	$^\circ\text{C/W}$
20-Contact PLCC (PC)	73	33	$^\circ\text{C/W}$

### NOTE:

- $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for CerDIP and P-DIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO package.

### CAUTION:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
- Do not apply voltages higher than  $V_{DD}$  or less than GND potential on any terminal except  $V_{REF}$ .
- The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
- Remove power before inserting or removing units from their sockets.

**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5\text{V}$  or  $+15\text{V}$ ,  $V_{REF} = +10\text{V}$ ,  $V_{OUT1} = 0\text{V}$ ,  $\text{AGND} = \text{DGND} = 0\text{V}$ ,  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$  apply for DAC-8012AR/BR,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  apply for DAC-8012ER/FR/FP/FPC,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>STATIC ACCURACY</b>									
Resolution			12	—	—	12	—	—	Bits
Relative Accuracy	INL	$T_A = \text{Full Temp. Range}$	—	—	$\pm 1/2$	—	—	$\pm 1$	LSB
Differential Nonlinearity (Note 1)	DNL	$T_A = \text{Full Temp. Range}$	—	—	$\pm 1$	—	—	$\pm 1$	LSB
Gain Error (Notes 2, 3)	$G_{FSE}$	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	—	—	$\pm 1$ $\pm 2$	—	—	$\pm 3$ $\pm 4$	LSB
Gain Temperature Coefficient $\Delta\text{Gain}/\Delta\text{Temperature}$ (Notes 4, 5)	$TCG_{FS}$		—	—	$\pm 5$	—	—	$\pm 5$	ppm/ $^\circ\text{C}$
DC Supply Rejection $\Delta\text{Gain}/\Delta V_{DD}$ (Note 4)	PSR	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$ ( $\Delta V_{DD} = \pm 5\%$ )	—	—	0.002 0.004	—	—	0.002 0.004	%/%
Output Leakage Current at OUT 1	$I_{LKG}$	$T_A = +25^\circ\text{C}$ , RD/WR = DS = 0V, All Digital Inputs = 0V $T_A = \text{Full Temp. Range}$ A/B Versions E/F/G/H Versions	—	—	10 200 25	—	—	10 200 25	nA
<b>DYNAMIC PERFORMANCE</b>									
Propagation Delay (Notes 4, 6, & 7)	$t_{pD}$	$T_A = +25^\circ\text{C}$ (OUT 1 Load = 100 $\Omega$ , $C_{EXT} = 13\text{pF}$ )	—	—	300	—	—	300	ns
Current Settling Time (Notes 4, 7)	$t_s$	$T_A = \text{Full Temp. Range}$ (To 1/2 LSB) $I_{OUT1}$ Load = 100 $\Omega$	—	—	1	—	—	1	$\mu\text{s}$
Glitch Energy (Note 4)	Q	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$ $V_{REF} = \text{AGND}$	—	—	400 500	—	—	400 500	nVs
AC Feedthrough at $I_{OUT1}$ (Note 4)	FT	$T_A = \text{Full Temp. Range}$ $V_{REF} = \pm 10\text{V}$ , $f = 10\text{kHz}$	—	—	5	—	—	5	mV <sub>p-p</sub>
<b>REFERENCE INPUT</b>									
Input Resistance (Pin 19 to GND)	$R_{REF}$	$T_A = \text{Full Temp. Range}$ Input Resistance	7	11	15	7	11	15	k $\Omega$

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**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = +5V$ ,  $V_{REF} = +10V$ ,  $V_{OUT1} = 0V$ ,  $AGND = DGND = 0V$ ,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$  apply for DAC-8012AR/BR,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$  apply for DAC-8012ER/FR/FP/FPC,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$  apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>ANALOG OUTPUTS</b>									
Output Capacitance (Note 4)	$C_{OUT}$	$V_{DD} = +5V$ or $+15V$ $T_A =$ Full Temp. Range DB0-DB11 = 0V, RD/WR = $\overline{DS} = 0V$	—	—	70	—	—	70	pF
$C_{OUT1}$		DB0-DB11 = $V_{DD}$ , RD/WR = $\overline{DS} = 0V$	—	—	150	—	—	150	
<b>DIGITAL INPUTS</b>									
Input High Voltage	$V_{INH}$	$T_A =$ Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	$V_{INL}$		—	—	0.8	—	—	0.8	
Input Current	$I_{IN}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	—	—	1 10	—	—	1 10	$\mu A$
Input Capacitance DB0-DB11 RD/WR, $\overline{DS}$ (Note 4)	$C_{IN}$	$T_A =$ Full Temp. Range	—	—	12	—	—	12	pF
			—	—	6	—	—	6	
<b>DIGITAL OUTPUTS</b>									
Output High Voltage	$V_{OH}$	$I_O = 400\mu A$	4.0	—	—	4.0	—	—	V
Output Low Voltage	$V_{OL}$	$I_O = -1.6mA$	—	—	0.4	—	—	0.4	V
Three-State Output Leakage Current			—	—	10	—	—	10	$\mu A$
<b>SWITCHING CHARACTERISTICS</b> (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	$t_{WSU}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	0 0	—	—	0 0	—	—	ns
Data Strobe to Write Hold Time		$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	0 0	—	—	0 0	—	—	
Read to Data Strobe Setup Time	$t_{RSU}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	0 0	—	—	0 0	—	—	ns
Data Strobe to Read Hold Time		$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	0 0	—	—	0 0	—	—	
Write Mode Data Strobe Width	$t_{WRS}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	180 250	—	—	180 250	—	—	ns
Read Mode Data Strobe Width		$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	220 290	—	—	220 290	—	—	
Data Setup Time	$t_{DSU}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	210 250	—	—	210 250	—	—	ns
Data Hold Time		$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	0 0	—	—	0 0	—	—	
Data Strobe to Data Valid Time (Notes 4, 9)	$t_{CO}$	$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	— —	—	300 400	— —	—	300 400	ns
Output Active Time from Deselection (Notes 4, 9)		$T_A = +25^{\circ}C$ $T_A =$ Full Temp. Range	— —	—	215 375	— —	—	215 375	
<b>POWER SUPPLY</b>									
Supply Current	$I_{DD}$	$T_A =$ Full Temp. Range (All Digital Inputs $V_{INL}$ or $V_{INH}$ )	—	—	2	—	—	2	mA
	$I_{DD}$	$T_A =$ Full Temp. Range (All Digital Inputs 0V or $V_{DB}$ )	—	10	100	—	10	100	$\mu A$

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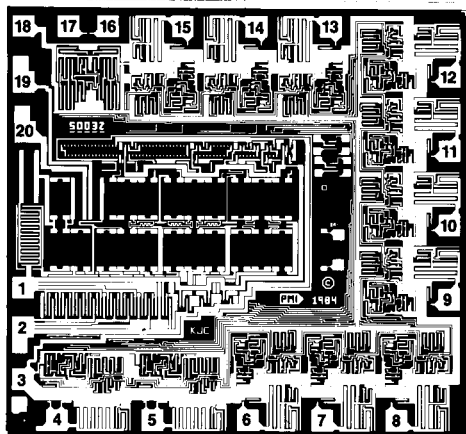
**ELECTRICAL CHARACTERISTICS** at  $V_{DD} = \pm 15V$ ,  $V_{REF} = +10V$ ,  $V_{OUT1} = 0V$ ,  $AGND = DGND = 0V$ ,  $T_A = -55^\circ C$  to  $+125^\circ C$  apply for DAC-8012AR/BR,  $T_A = -40^\circ C$  to  $+85^\circ C$  apply for DAC-8012ER/FR/FP/FPC,  $T_A = 0^\circ C$  to  $+70^\circ C$  apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>DIGITAL INPUTS</b>									
Input High Voltage	$V_{INH}$	$T_A = \text{Full Temp. Range}$	13.5	—	—	13.5	—	—	V
Input Low Voltage	$V_{INL}$		—	—	1.5	—	—	1.5	V
Input Current	$I_{IN}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1	—	—	1	$\mu A$
Input Capacitance DB0-DB11 RD/WR, DS (Note 4)	$C_{IN}$	$T_A = \text{Full Temp. Range}$	—	—	12	—	—	12	pF
			—	—	10	—	—	10	pF
<b>DIGITAL OUTPUTS</b>									
Output High Voltage	$V_{OH}$	$I_O = 3mA$	13.5	—	—	13.5	—	—	V
Output Low Voltage	$V_{OL}$	$I_O = -3mA$	—	—	1.5	—	—	1.5	V
Three-State Output Leakage Current			—	—	10	—	—	10	$\mu A$
<b>SWITCHING CHARACTERISTICS</b> (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	$t_{WSU}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
Data Strobe to Write Hold Time	$t_{WH}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
Read to Data Strobe Setup Time	$t_{RSU}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
Data Strobe to Read Hold Time	$t_{RH}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
Write Mode Data Strobe Width	$t_{WRS}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	100	—	—	100	—	—	ns
			120	—	—	120	—	—	ns
Read Mode Data Strobe Width	$t_{RDS}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	110	—	—	110	—	—	ns
			150	—	—	150	—	—	ns
Data Setup Time	$t_{DSU}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	90	—	—	90	—	—	ns
			120	—	—	120	—	—	ns
Data Hold Time	$t_{DH}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0	—	—	0	—	—	ns
			0	—	—	0	—	—	ns
Data Strobe to Output Valid Time (Note 9)	$t_{CO}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	180	—	—	180	ns
			—	—	220	—	—	220	ns
Output Active Time for Deselection (Note 9)	$t_{OTD}$	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	180	—	—	180	ns
			—	—	250	—	—	250	ns
<b>POWER SUPPLY</b>									
Supply Current	$I_{DD}$	$T_A = \text{Full Temp. Range}$ (All Digital Inputs $V_{INL}$ or $V_{INH}$ )	—	—	2	—	—	2	mA
	$I_{DD}$	$T_A = \text{Full Temp. Range}$ (All Digital Inputs 0V or $V_{DD}$ )	—	10	100	—	10	100	$\mu A$

## NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal  $R_{FB}$ . DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED but NOT TESTED.
- Typical value is 2ppm/ $^\circ C$  for  $V_{DD} = +5V$ .
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to  $V_{DD}$ ; or  $V_{DD}$  to 0V.
- Sample tested at  $+25^\circ C$  to ensure compliance.
- See load circuits for switching tests.

## DICE CHARACTERISTICS



- |               |                      |
|---------------|----------------------|
| 1. OUT 1      | 11. DB4              |
| 2. AGND       | 12. DB3              |
| 3. DGND       | 13. DB2              |
| 4. DB11 (MSB) | 14. DB1              |
| 5. DB10       | 15. DB0 (LSB)        |
| 6. DB9        | 16. DS               |
| 7. DB8        | 17. RD/WR            |
| 8. DB7        | 18. V <sub>DD</sub>  |
| 9. DB6        | 19. V <sub>REF</sub> |
| 10. DB5       | 20. R <sub>FB</sub>  |

**DIE SIZE 0.121 × 0.112 inch, 13,552 sq. mils**  
**(3.07 × 2.85 mm, 8.75 sq. mm)**

**WAFER TEST LIMITS** at V<sub>DD</sub> = +5V or +15V, V<sub>REF</sub> = +10V, V<sub>OUT 1</sub> = 0V, AGND = DGND = 0V, T<sub>A</sub> = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	
			LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G <sub>FSE</sub>	DAC Latches Loaded with 1111 1111 1111	±3	LSB MAX
Output Leakage	I <sub>LKG</sub>	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R <sub>REF</sub>	Pad 19	6/15	kΩ MIN/ kΩ MAX
Output High Voltage	V <sub>OH</sub>	V <sub>DD</sub> = 5V, I <sub>O</sub> = 400μA	4.0	V MIN
Output Low Voltage	V <sub>OL</sub>	V <sub>DD</sub> = 5V, I <sub>O</sub> = -1.6mA	0.4	V MAX
Digital Input High	V <sub>INH</sub>	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	2.4 13.5	V MIN
Digital Input Low	V <sub>INL</sub>	V <sub>DD</sub> = 5V V <sub>DD</sub> = 15V	0.8 1.5	V MAX
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0V or V <sub>DD</sub>	±1	μA MAX
Supply Current	I <sub>DD</sub>	All Digital Inputs V <sub>INL</sub> or V <sub>INH</sub> All Digital Inputs 0V or V <sub>DD</sub>	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV <sub>DD</sub> )	PSRR	V <sub>DD</sub> = ±5%	0.004	%/% MAX

**NOTE:**

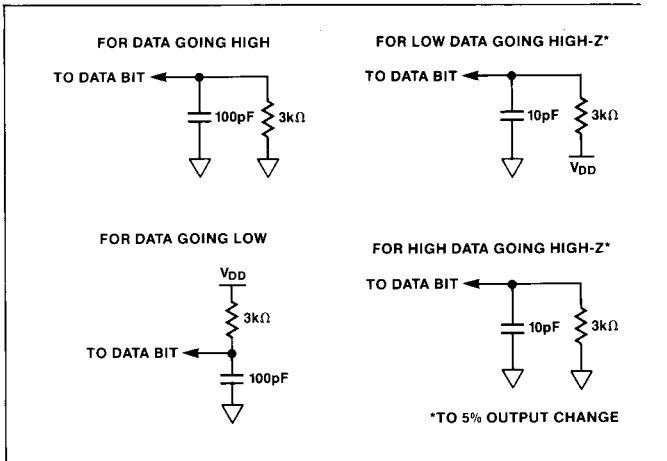
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at V<sub>DD</sub> = +5V or +15V, V<sub>REF</sub> = +10V, V<sub>OUT 1</sub> = 0V; T<sub>A</sub> = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	
			TYPICAL	UNITS
Digital Input Capacitance	C <sub>IN</sub>		12	pF
Output Capacitance	C <sub>OUT 1</sub>	DAC Latches Loaded with 0000 0000 0000	70	pF
	C <sub>OUT 1</sub>	DAC Latches Loaded with 1111 1111 1111	150	pF
Propagation Delay	t <sub>pD</sub>	V <sub>DD</sub> = 15V V <sub>DD</sub> = 5V	300	ns

# DAC-8012

## LOAD CIRCUITS FOR SWITCHING TESTS



## PARAMETER DEFINITIONS

### RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

### DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of  $\pm 1$  LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will not decrease for an increase in digital code applied).

### GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is  $V_{REF}$  minus 1 LSB. The gain error is adjustable to zero using external resistance.

### OUTPUT CAPACITANCE

The capacitance from OUT1 to AGND.

### PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

### FEEDTHROUGH GLITCH ENERGY

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with  $V_{REF} = AGND$ .

## LOGIC INFORMATION

### D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A Converter section of the DAC-8012, and Figure 2 gives an approximate equivalent switch circuit. R is typically 11k $\Omega$ .

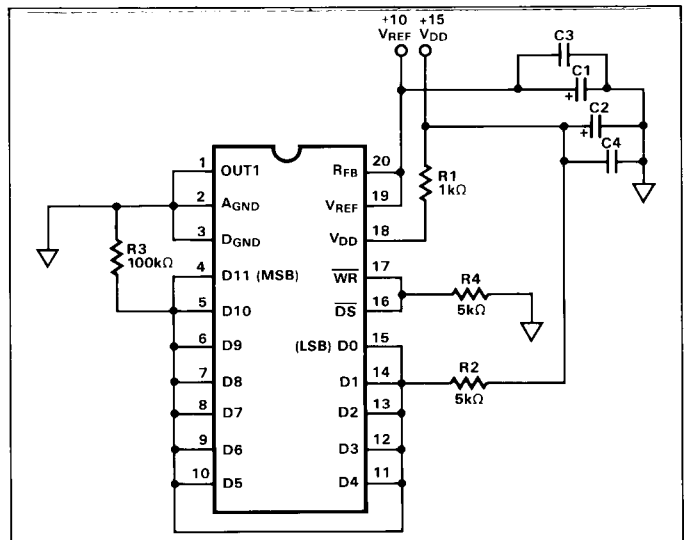
The binary-weighted currents are switched between OUT 1 and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT 1 terminal,  $C_{OUT 1}$ , is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT 1). One of the current switches is shown in Figure 2.

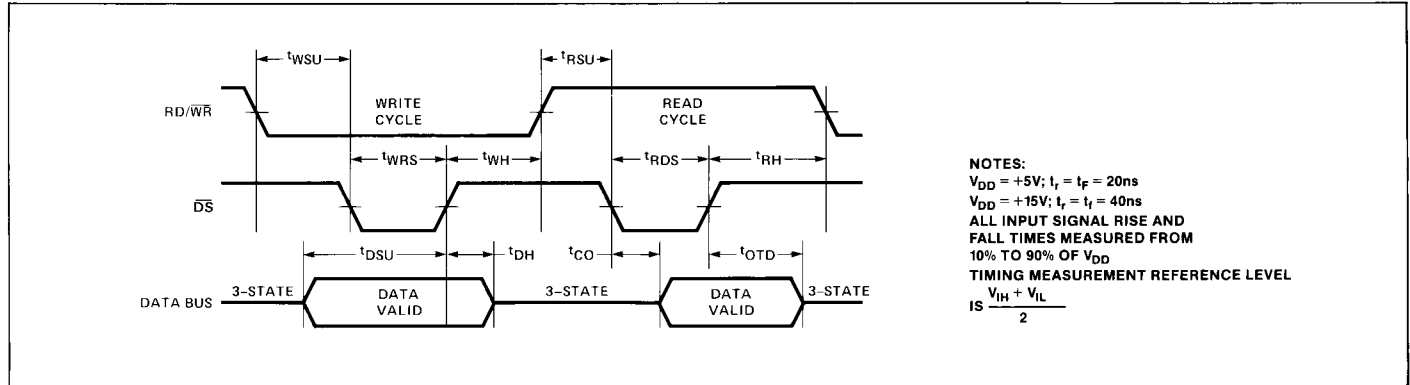
The input resistance at  $V_{REF}$  (Figure 1) is always equal to  $R_{LDR}$  ( $R_{LDR}$  is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the  $V_{REF}$  pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external  $R_{FB}$  is recommended to define scale factor.)

The internal feedback resistor ( $R_{FB}$ ) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however, when the circuit is not powered up the switch assumes an open state.

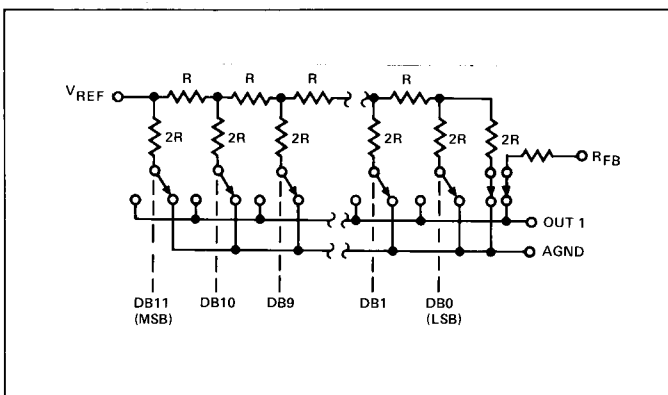
## BURN-IN CIRCUIT



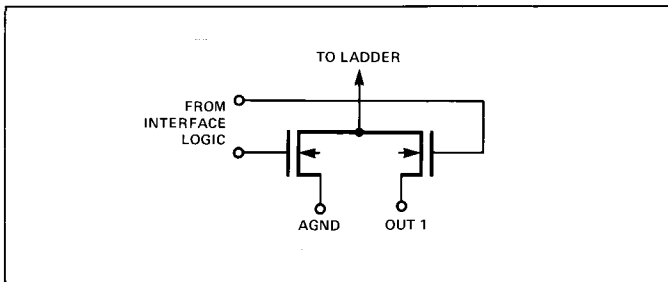
**TIMING DIAGRAM**



**FIGURE 1: Simplified D/A Circuit of DAC-8012**



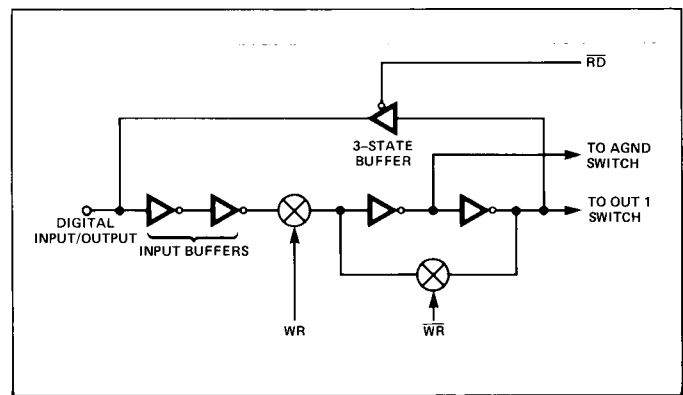
**FIGURE 2: N-Channel Current Steering Switch**



**DIGITAL SECTION**

Figure 3 shows the digital I/O structure for one bit. When the data strobe ( $\overline{DS}$ ) and the  $\overline{RD}/\overline{WR}$  lines are held low, data at the digital input is fed through the input buffers and the data latches which control the DAC current output switches are transparent. Data is latched when either  $\overline{DS}$  or  $\overline{RD}/\overline{WR}$  go high. When the data strobe  $\overline{DS}$  is held low and the  $\overline{RD}/\overline{WR}$  line is held high, the three-state buffer becomes active and the data from the latches is

**FIGURE 3: Digital Input/Output Structure**



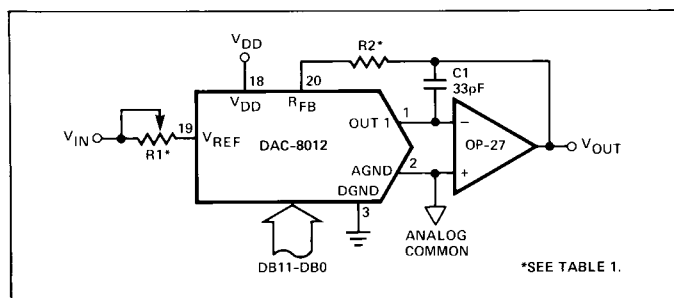
fed through the three-state buffers to the digital input/output lines. This is known as the Read Cycle, or data readback.

The input buffers are simple CMOS inverters designed such that when the DAC-8012 is operated with  $V_{DD} = +5V$ , the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0V to 3.0V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails ( $V_{DD}$  and  $D_{GND}$ ) as is practically possible. The DAC-8012 may be operated with any supply voltage in the range  $5V \leq V_{DD} \leq 15V$ . With  $V_{DD} = +15V$ , the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

The three-state output buffers, in the active mode, provide TTL-compatible digital outputs with a fan-out of one TTL load when the DAC-8012 is operated with +5V power supply. When powered from +15V, the output buffers provide output logic levels of 1.5V and 13.5V. Three-state output leakage is typically 10nA.

# DAC-8012

**FIGURE 4:** Unipolar Binary Operation



## BASIC APPLICATIONS

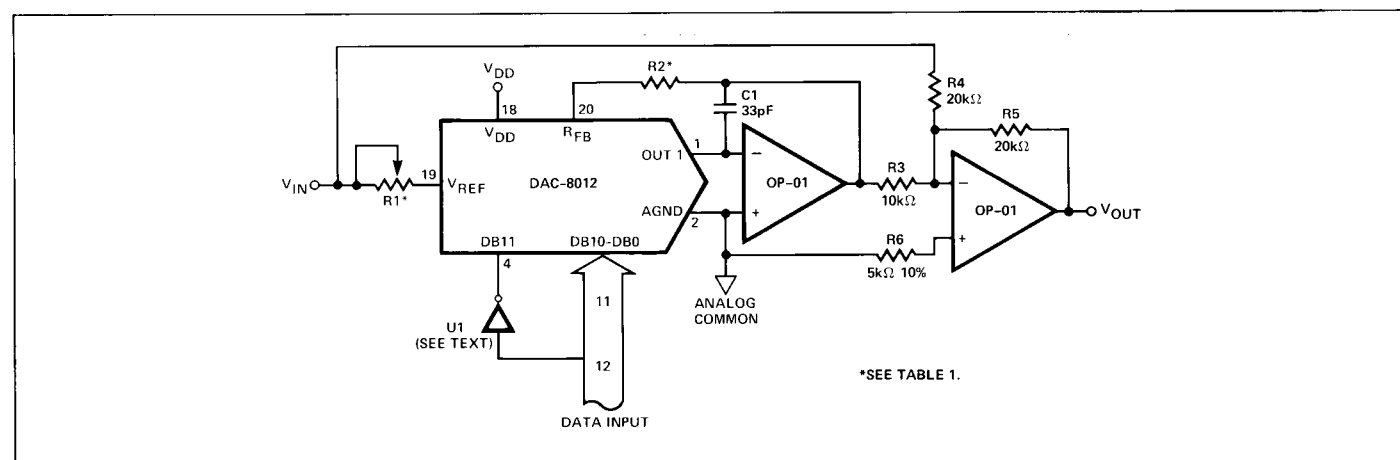
Figures 4 and 5 show simple unipolar and bipolar circuits using the DAC-8012. Resistor R1 is used to trim for full scale. The following versions: DAC-8012AR, DAC-8012ER, DAC-8012GP, have a guaranteed maximum gain error of  $\pm 1$  LSB at  $+25^\circ\text{C}$  and  $V_{DD} = +5\text{V}$ , and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the  $V_{REF}$  terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to  $-V_{IN}$  (the inversion is introduced by the op amp); or  $V_{IN}$  can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier).  $V_{IN}$  can be any voltage in the range  $-20\text{V} \leq V_{IN} \leq +20\text{V}$  (provided the op amp can handle such voltages) since  $V_{REF}$  is permitted to exceed  $V_{DD}$ . Table II shows the code relationship for the circuit of Figure 4.

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U<sub>1</sub> on the MSB line, converts 2's-complement input code to offset binary code. The inverter U<sub>1</sub> may be omitted if the inversion is done in software, using an exclusive OR instruction.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

**FIGURE 5:** Bipolar Operation (2's Complement Code)



**TABLE I:** Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1	100Ω	20Ω
R2	33Ω	6.8Ω

**TABLE II:** Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left( \frac{4095}{4096} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left( \frac{2048}{4096} \right) = -1/2 V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN} \cdot \left( \frac{1}{4096} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts

**TABLE III:** 2's Complement Code Table for Circuit of Figure 5

DATA INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN} \cdot \left( \frac{2047}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN} \cdot \left( \frac{1}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left( \frac{1}{2048} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left( \frac{2048}{2048} \right)$



**APPLICATIONS HINTS**

**Output Offset:** CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is  $0.67 V_{OS}$  where  $V_{OS}$  is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that  $V_{OS}$  be no greater than 10% of 1 LSB over the temperature range of operation.

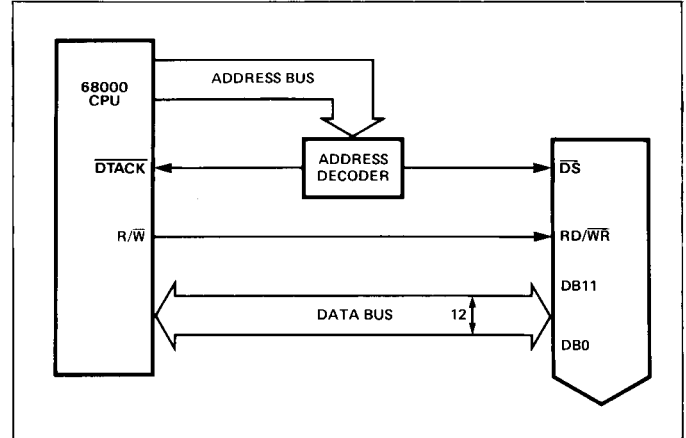
**General Ground Management:** AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the DAC-8012. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

**Digital Glitches:** When RD/WR and DS are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which RD/WR is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse RD/WR, so that it only occurs when data is valid, will eliminate the problem.

**INTERFACING THE DAC-8012 TO MICROPROCESSORS**

Figure 6 shows the interface configuration for the 68000 16-bit microprocessor. No external logic is required to write data into the DAC or to readback data from the DAC-8012 latches. Analog circuitry has been removed for clarity.

**FIGURE 6:** 68000 16-Bit Microprocessor to DAC-8012 Interface



**FIGURE 7:** 8-Bit Processor to DAC-8012 Interface

