# Octal 8-Bit CMOS D/A Converter

# DAC8800

## Scope

This specification covers the detail requirements for an octal 8-bit, voltage output, CMOS digital-to-analog converter. A serial data input interface updates one of eight internal DACs at a time. A $\overline{CLR}$ input resets all internal DAC registers to zero. The DAC8800 operates from single ($V_{DD}$ = +12 V, $V_{SS}$ = 0 V) or dual ($V_{DD}$ = +12 V, $V_{SS}$ = –5 V) power supplies.

It is highly recommended that this data sheet be used as a baseline for new military or aerospace spec control drawings.

## Part Number/Case Outline

For case outline dimensions, see Package Information Appendix of General Specifications ADI-M-1000. The complete part number of this 883 device is as follows:

| Device Type | ADI 883 Part Number | Package Description | Package Designation ADI | Package Designation MIL-STD-1835 |
|---|---|---|---|---|
| 01 | DAC8800BR/883 | 0.3" Cerdip | Q-20 | GDIP1-T20 |

## Absolute Maximum Ratings[1] ($T_A$ = +25°C unless otherwise noted)

$V_{DD}$ to $V_{SS}$ . . . . . 0 V, +20 V
$V_{DD}$ to GND . . . . . 0 V, +20 V
$V_{SS}$ to GND . . . . . –20 V, 0 V
Digital Input Voltage to GND . . . . . GND – 0.3 V, $V_{DD}$ + 0.3 V
$V_{REF}H$ to GND . . . . . $V_{REF}L$, $V_{DD}$
$V_{REF}L$ to GND . . . . . $V_{SS}$, $V_{REF}H$
$V_{OUT}$ to GND . . . . . $V_{REF}L$, $V_{REF}H$
Maximum Junction Temperature ($T_J$ Max) . . . . . +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C
Package Power Dissipation . . . . . $(T_J Max – T_A)/\theta_{JA}$

## Recommended Operating Conditions

Operating Temperature Range ($T_A$) . . . . . –55°C to +125°C

## Thermal Characteristics

Thermal Resistance, Junction-to-Case ($\theta_{JC}$) . . . . . 11°C/W max
Thermal Resistance, Junction-to-Ambient ($\theta_{JA}$) . . . . . 76°C/W max

NOTE
[1]Permanent damage may occur if any absolute maximum rating is exceeded. Functional operation is not implied, and device reliability may be impaired by exposure to higher than recommended voltages for extended periods of time.

REV. A



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# DAC8800–SPECIFICATIONS

**Table 1. Electrical Performance Characteristics**

| Test | Symbol | Conditions ($V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $V_{REF}H$ = +5 V, $V_{REF}L$ = 0 V; –55°C ≤ $T_A$ ≤ +125°C unless otherwise noted) | Group A Subgroups | Device Type | Limits Min | Limits Max | Units |
|---|---|---|---|---|---|---|---|
| STATIC ACCURACY | | All Specifications Apply for DACs A, B, C, D, E, F, G, H | | | | | |
| Resolution | N | | 1, 2, 3 | 01 | 8 | | Bits |
| Total Unadjusted Error[1] | TUE | | 1, 2, 3 | 01 | | ±1/2 | LSB |
| Differential Nonlinearity Error[2] | DNL | | 1, 2, 3 | 01 | | ±1 | LSB |
| Full-Scale Error | $G_{FSE}$ | | 1, 2, 3 | 01 | | ±1/2 | LSB |
| Zero Code Error | $V_{ZSE}$ | | 1, 2, 3 | 01 | | ±1/2 | LSB |
| DAC Output Resistance | $R_{OUT}$ | | 1, 2, 3 | 01 | 8 | 16 | kΩ |
| DAC Output Resistance Match | $\Delta R_{OUT}/R_{OUT}$ | | 1, 2, 3 | 01 | | ±2 | % |
| REFERENCE INPUT[3] | | | | | | | |
| Input Resistance | $V_{REF}H$ | Digital Inputs = 55 H | 1, 2, 3 | 01 | 2 | | kΩ |
| Input Resistance Match | $\Delta R_{REF}/R_{REF}H$ | Digital Inputs = 55 H | 1, 2, 3 | 01 | | ±2 | % |
| DIGITAL INPUTS | | | | | | | |
| Logic High | $V_{INH}$ | | 1, 2, 3 | 01 | 2.4 | | V |
| Logic Low | $V_{INL}$ | | 1, 2, 3 | 01 | | 0.8 | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0 V or +5 V | 1, 2, 3 | 01 | | ±1 | μA |
| POWER SUPPLIES[4] | | | | | | | |
| Positive Supply Current | $I_{DD}$ | $V_{SS}$ = –5 V, TTL<br>CMOS | 1, 2, 3 | 01 | | 2<br>0.4 | mA |
| Negative Supply Current | $I_{SS}$ | $V_{SS}$ = –5 V | 1, 2, 3 | 01 | | 0.2 | mA |
| Power Dissipation | $P_{DISS}$ | Single Supply Operation, $V_{SS}$ = 0<br>Dual Supply Operation $V_{SS}$ = –5 V | 1, 2, 3 | 01 | | 24<br>25 | mW |
| DC Power Supply Rejection Ratio | PSRR | $\Delta V_{DD}$ = ±5%, $V_{SS}$ = –5 V | 1, 2, 3 | 01 | | 0.01 | %/% |
| SWITCHING CHARACTERISTICS[5] | | | | | | | mW |
| Input Clock Pulse Width | $t_{CH}$, $t_{CL}$ | Clock Level High or Low | 9, 10, 11 | 01 | 60 | | ns |
| Data Setup Time | $t_{DS}$ | | 9, 10, 11 | 01 | 30 | | ns |
| Data Hold Time | $t_{DH}$ | | 9, 10, 11 | 01 | 30 | | ns |
| DAC Register Load Pulse Width | $t_{LD}$ | | 9, 10, 11 | 01 | 50 | | ns |
| Clear Pulse Width | $t_{CLR}$ | | 9, 10, 11 | 01 | 50 | | ns |
| Clock Edge to Load Time | $t_{CKLD}$ | | 9, 10, 11 | 01 | 50 | | ns |
| Load Edge to Next Clock Edge Time | $t_{LDCK}$ | | 9, 10, 11 | 01 | 50 | | ns |

NOTES

[1]Includes full-scale error, relative accuracy, and zero code error.

[2]All devices guaranteed monotonic over the full operating temperature range.

[3]$V_{DD}$ –4 volts is the maximum operating reference voltage. Also $V_{REF}H \geq V_{REF}L$.

[4]Digital input voltages $V_{IN} = V_{INL}$ or $V_{INH}$ for TTL condition; $V_{IN}$ = 0 V or +5 V for CMOS condition. DAC outputs unloaded. $P_{DISS}$ is calculated form $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.

[5]See timing diagram for location of measured values.

**Table 2. Electrical Test Requirements for Class B Devices**

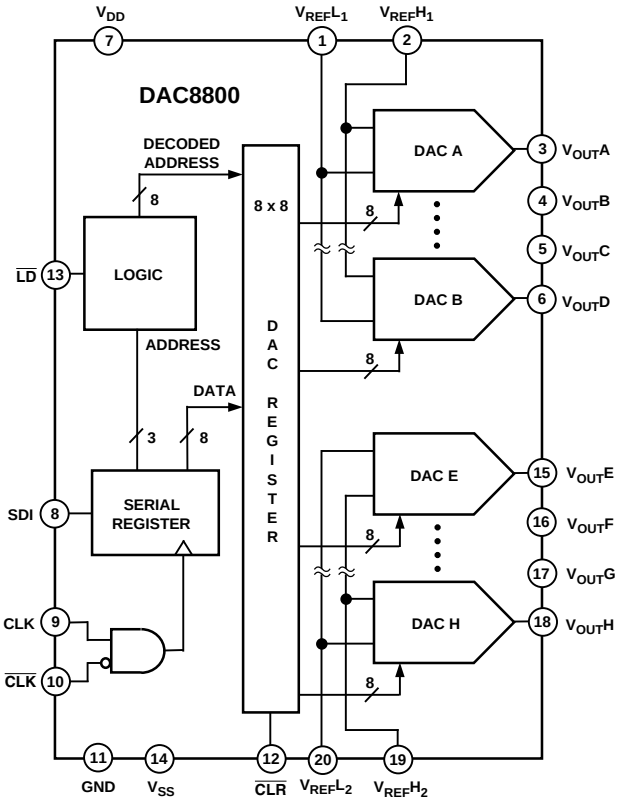
| MIL-STD-883 Test Requirements | Subgroups (See Table 1) |
|---|---|
| Interim Electrical Parameters (Pre Burn-In) | 1 |
| Final Electrical Test Parameters | 1,* 2, 3 |
| Group A Test Requirements | 1, 2, 3, 9 |

NOTE
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

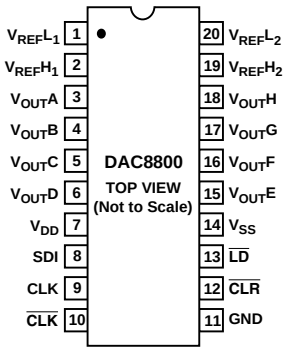
**Table 3. Pin Function Descriptions**

| Pin | Mnemonic | Description |
|---|---|---|
| 1 | $V_{REF}L_1$ | External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}L_1$ determines the lowest negative DAC output voltage. $V_{REF}L_1$ must be equal to or more positive than $V_{SS}$. |
| 2 | $V_{REF}H_1$ | External DAC voltage reference input shared by DAC A, B, C, D. $V_{REF}H_1$ determines the highest positive DAC output voltage. |
| 3 | $V_{OUT}A$ | DAC A Output |
| 4 | $V_{OUT}B$ | DAC B Output } Output voltage determined by external $V_{REF}H_1$ and $V_{REF}L_1$. |
| 5 | $V_{OUT}C$ | DAC C Output |
| 6 | $V_{OUT}D$ | DAC D Output |
| 7 | $V_{DD}$ | Positive supply, allowable input voltage range +4.5 V to +16 V. |
| 8 | SDI | Serial Data Input |
| 9 | CLK | Serial Clock Input, positive edge triggered } TTL Input Compatible |
| 10 | $\overline{CLK}$ | Clock Enable or Serial Clock Input negative edge triggered |
| 11 | GND | Ground |
| 12 | $\overline{CLR}$ | Clear Input (Active Low), Asynchronous TTL compatible input that resets all DAC registers to zero code. |
| 13 | $\overline{LD}$ | Load DAC Register Strobe, TTL compatible input that transfers data bits from serial input register into the decoded DAC register. See Table 2. |
| 14 | $V_{SS}$ | Negative Supply, allowable input voltage range 0 V to –12 V. |
| 15 | $V_{OUT}E$ | DAC E Output |
| 16 | $V_{OUT}F$ | DAC F Output } Output voltage determined by external $V_{REF}H_2$ and $V_{REF}L_2$. |
| 17 | $V_{OUT}G$ | DAC G Output |
| 18 | $V_{OUT}H$ | DAC H Output |
| 19 | $V_{REF}H_2$ | External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}H_2$ determines the highest positive DAC Output voltage. |
| 20 | $V_{REF}L_2$ | External DAC voltage reference input shared by DAC E, F, G, H. $V_{REF}L_2$ determines the lowest negative DAC output voltage. $V_{REF}L_2$ must be equal to or more positive than $V_{SS}$. |

### Functional Block Diagram and Terminal Assignment




**Q-20 Package**

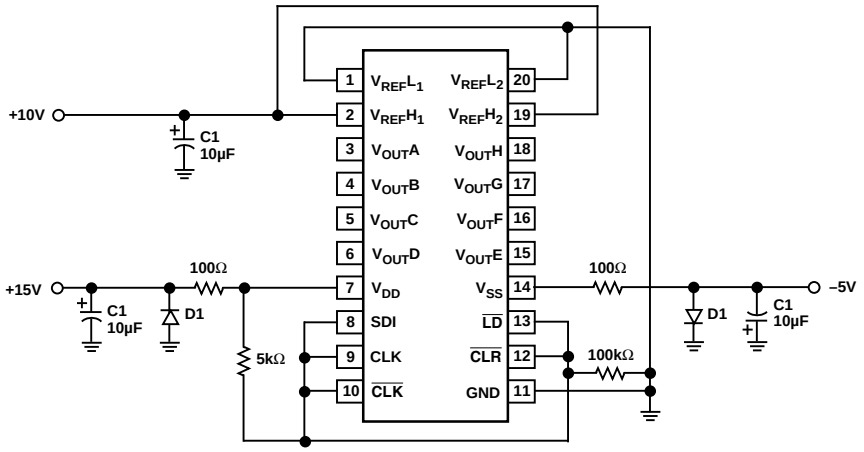



### Microcircuit Technology Group

This microcircuit is covered by technology group (80).

### Life Test /Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



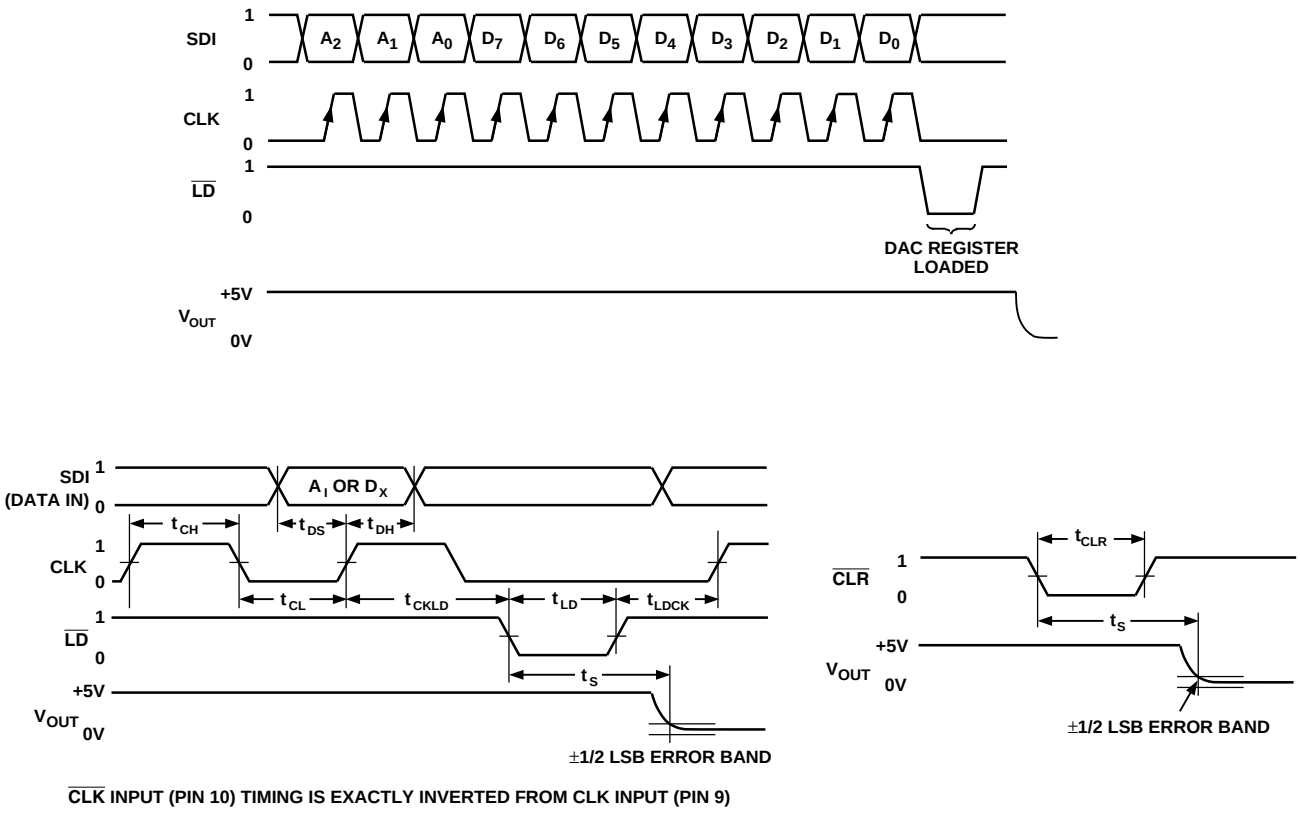



*Figure 1. Timing Diagrams*

**Table 4. Serial Input Decode Table**

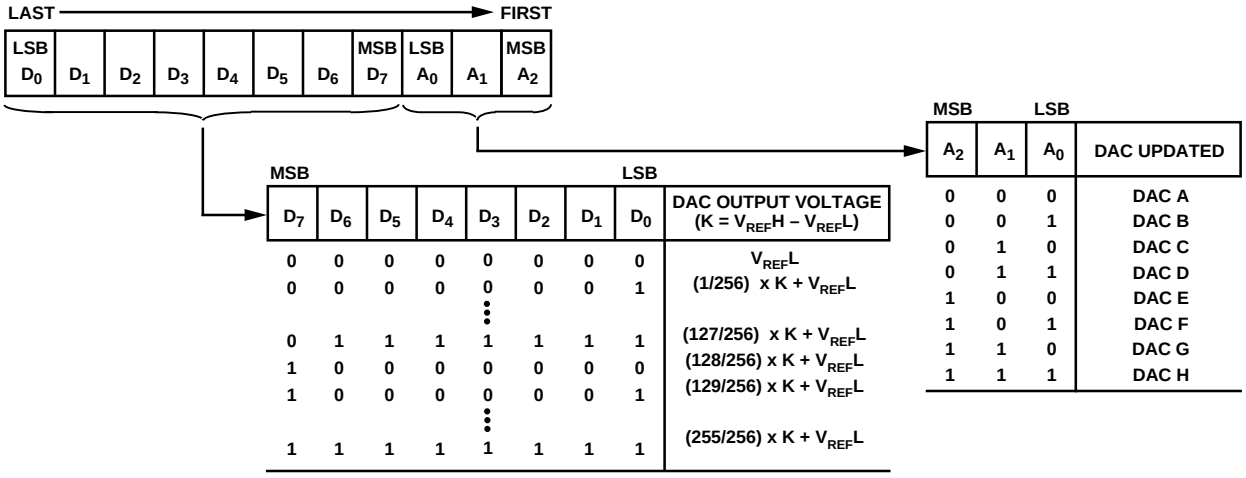



**Table 5. Logic Control Input Truth Table**

| CLK | $\overline{CLK}$ | Input Shift Register Operation |
|---|---|---|
| ↑ | L | Shift Data |
| H | ↓ | Shift Data |
| L | X | No Operation |
| X | H | No Operation |