AN40_1A

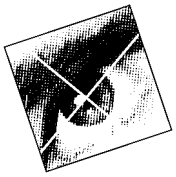
Bt81x/Bt82x/Bt848

Sync Locking In Source Multiplexed Applications

Rockwell Semiconductor Systems

Print date: May 1997

PRINTED IN THE UNITED STATES OF AMERICA



Sync Locking in Source-Multiplexed Applications

In applications such as security, time to lock sync after switching sources can be critical. The method used to acquire lock after switching from one NTSC source to another non genlocked NTSC source is addressed here.

Conditions that must exist for these explanations to be valid are:

1. All sources are clamped to ground. This discussion considers only sync locking time, not including AGC and clamping times, which are independent functions. Not clamping can greatly extend the lock period because the part must first clamp, and possibly AGC, before lock can be achieved. How long this takes depends on the magnitude of the difference between the source being switched to and the present source.
2. SYNC tip to back porch levels must be similar enough so that sync detection is not affected. See 1 above.
3. Phase error only is considered. Frequency error will further extend each lock period respectively.
4. Discussions pertain only to the NTSC standard.
5. Non-genlocked conditions represent worst case, asynchronous switching is assumed, and the worst combination of the two is depicted.
6. Mux switching does not involve a change in video standards, e.g., NTSC to PAL.

Loops

There are actually four different loops to be locked to video upon interruption from a locked source to an asynchronous source: field polarity, vertical, horizontal, and burst.

FIELD

Field must detect eight consecutive wrong fields before changing polarity. If the type of field (even or odd) indicated in a vertical sync detection has been opposite of the decoder's expectation for eight consecutive vertical sync detections, the FIELD signal will not change value at that vertical sync (VRESET).

Otherwise, the FIELD signal will be inverted following each VRESET. The type of field indicated in a vertical sync detection is determined by the location of the trailing edge of the serration pulses relative to the horizontal sync. If the trailing edge of the serration pulses occurs within +/- 1/4 line of a horizontal sync, the next field is detected as odd for NTSC and even for PAL. If the trailing edge of the serration pulses occurs more that 1/4 line from the nearest horizontal sync, the next field is detected as even for NTSC and odd for PAL.

The worst case settling time for the FIELD pin is thus 8 fields, although it may settle in as few as 0 fields.

VERTICAL

When vertical lock has been achieved, a 64 line VWINDOW will open 32 lines prior to the next expected vertical sync. If a vertical sync is detected before the VWINDOW opens, it will be ignored. A VRESET will be output at the expected vertical sync location whether a vertical sync has been detected or not.

Any vertical sync that is detected within the 64 line VWINDOW will reset the counters that control the VACTIVE signal and the location of the next expected vertical sync.

If no vertical sync is detected within a VWINDOW, the first vertical sync detected prior to the next VWINDOW will be accepted as legitimate and the vertical timing will be reset to synchronize it to that vertical sync. A VRESET will be output and the counters that control the VACTIVE signal, the location of the next expected vertical sync, and the VWINDOW will be reset.

Since the VWINDOW counter is reset, the VWINDOW will remain open for 32 lines after the vertical sync. Any additional vertical syncs detected while the VWINDOW is open will also reset the counters that control the VACTIVE signal and the location of the next expected vertical sync.

Assuming that DC levels are the same, vertical lock will be achieved in 1–2 fields. DC offsets between the two signals due to unclamped video can extend vertical lock up to 4 fields (the greater the DC offset, the longer the locking time). For fast vertical locking it is recommended that all inputs be DC restored to a common DC level prior to switching. This can be easily accomplished by simply using a diode to clamp to ground.

HORIZONTAL

Horizontal locking is implemented as a digital Phase Lock Loop (PLL), with no reset. If a horizontal sync is detected and the HWINDOW is open, the HWINDOW is closed and an error signal is generated based on the difference between the detected horizontal sync location and its expected location. This error signal is fed back to adjust the next expected horizontal sync location. The HWINDOW will open 12 clocks prior to the next expected horizontal sync, and will not close until a horizontal sync has been detected. An HRESET will be output at each expected hsync location.

Full lock (settling to ±1 clock) is achieved 12 lines from when the actual horizontal pulse is acquired. This occurs independently of the vertical loop.

BURST

Burst lock, or color lock, requires satisfaction of three conditions to complete lock.

1. HSYNC must achieve ±1 clock of expected before further evaluation is made.
2. After HSYNC is within ±1 clock, frequency error is corrected.
3. Subcarrier loop phase error is corrected (this may occur while frequency is corrected). This error is corrected to less than 5 degrees in 8–9 lines (12 lines in PAL for polarity), even for phase errors of as much as 180 degrees.

The amount of time to achieve color lock is dependent first, on the frequency error of the two subcarriers being switched. The maximum subcarrier frequency error that can be corrected without residual hue error is ±244 ppm. Therefore, the total range is 488 ppm. While frequency lock can be achieved at up to 400 ppm, phase correction is not guaranteed, and hue error will result.

If the subcarrier frequency difference between the two sources is 0 ppm, then color lock will be achieved (within 5 degrees) in 8–9 lines (phase correction only).

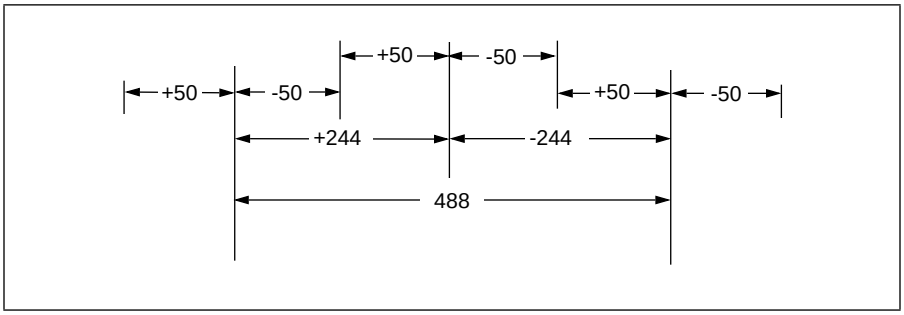
If the subcarrier frequency difference between the two sources is 244 ppm, then color lock will be achieved (within 5 degrees) in about 320 lines (phase error is corrected during this time). Values between 0 and 244 ppm are approximately linearly related. The following table can be used to estimate the time to correct a particular error.

Table 1. Numbers of Lines to Correct Various F_{sc} Errors.

ΔF_{sc} (PPM)	Lines to Lock
0	8–9
10	90
100	245
244	320
488	400

Keep in mind that the recommended crystal is rated at ±50 ppm. Accordingly, this can cause a range offset of ±50 ppm.

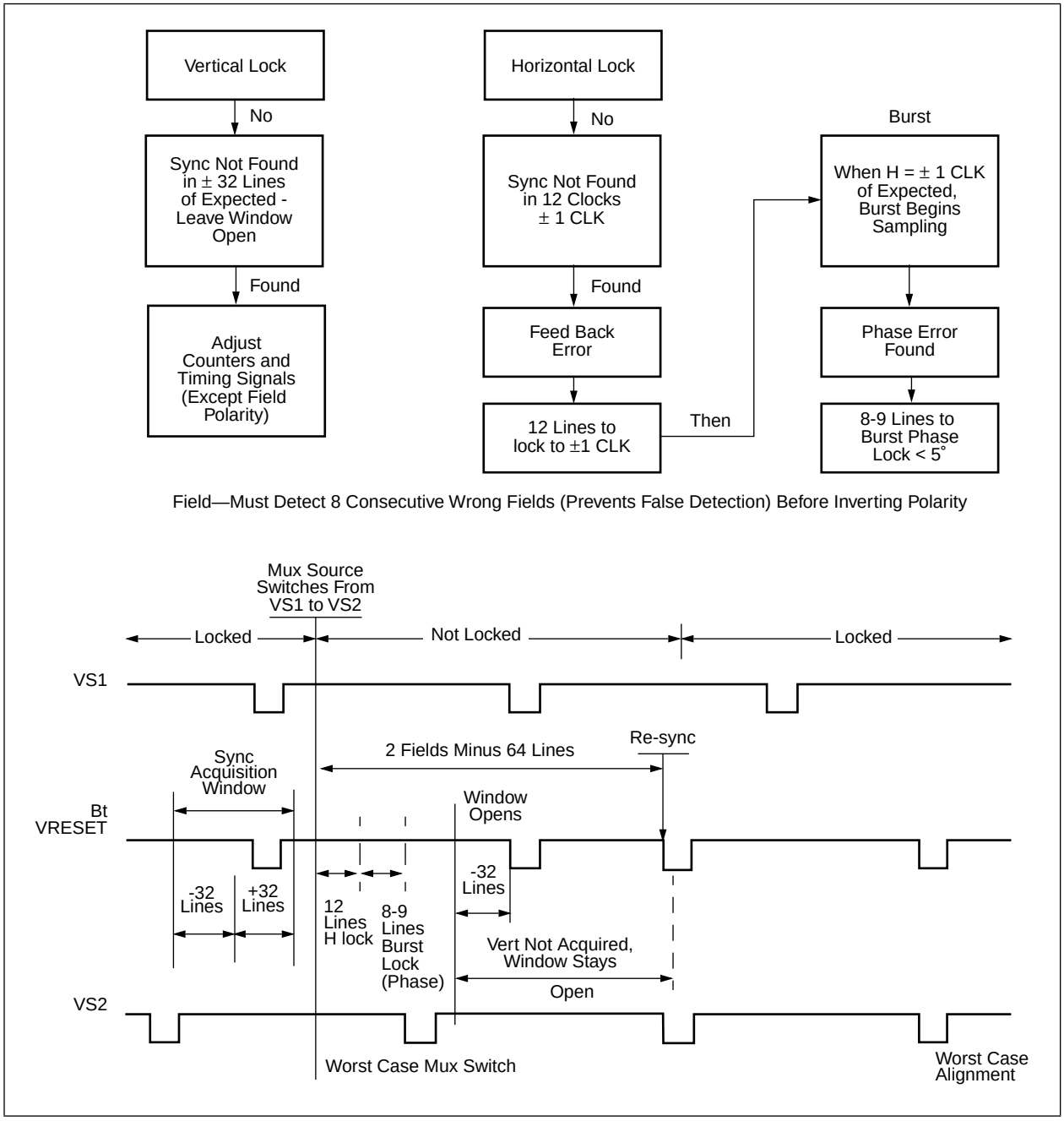
Figure 1. Subcarrier Range



Error correction is also dependent on correctly programming the IIC programmable burst delay values.

Figure 2 shows a block diagram of the various sync relationships.

Figure 2. Sync Relationships



SUMMARY

In summary, except for field polarity requiring eight fields of assurance, and given that no frequency errors are considered, and all inputs are relatively the same gain and clamped to ground, vertical lock can actually be achieved within two fields minus 64 lines, or, to put it another way, within 40 to 460 lines for NTSC, and 60 to 560 lines in PAL. HLOCK will be achieved within 12 lines from the MUX switch point, and burst lock within 8–9 lines after achieving HLOCK. Both HLOCK and burst are independent of VLOCK.

To be safe, after switching MUXed sources, ignore the first VRESET. By the second VRESET, full sync lock, except field polarity, can be assured.

Switching within 1 field can be achieved if:

1. DC levels have been restored to a common level.
2. The system has control over when the signal is switched into the new source. If the switch takes place just prior to the serration pulses of the new source then the period of the first VRESET pulses will be correct.

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