

### INTRODUCTION

The DS1WM 1-Wire Master, termed 1WM, was created to facilitate host CPU communication with devices over a 1-Wire bus without concern for bit timing. This application note shows how to incorporate the 1-Wire Master into a user's ASIC design. The DS89C200 referred to in this document is a theoretical micro controller. It is assumed the reader has knowledge of the DS1WM 1-Wire Master and Dallas Semiconductor's 1-Wire protocol. For more detailed information see [1] **Book of iButton Standards** and [2] **DS1WM Datasheet**.

### STRUCTURE

The 1WM is arranged as a top-level harness that connects four sub-modules together to form a complete unit. There is no HDL code in the top-level harness. The four sub-module files consist of the `one_wire_interface`, the `one_wire_master`, the `clk_prescaler` and the `one_wire_io`. For applications that do not need the clock prescaler, this module can be left out if an external 1 MHz clock source for the `clk_1us` signal is supplied (Noted as  $\tau$  in the DS1WM datasheet, the input clock is specified from 0.8 to 1.0 MHz).

The `one_wire_io` module provides the bi-directional signals for the DATA and the DQ signals. In most applications the DQ signal will be an I/O pin. If this is the case, the pad driver for DQ must be an open drain pad with the proper ESD protection (figure 1). Also, if the peripheral devices use a pull-up voltage that is greater than the 1WM supply, then a pad driver must be chosen that can tolerate the extra voltage and diode clamps must not be used. Dallas recommends that the output driver (Q1) of 100 $\Omega$  and an external DQ pull up of 4.7 k $\Omega$  to chip VCC. Chip VCC must be greater than  $V_{IH}$  of the 1-Wire slave for proper communication.

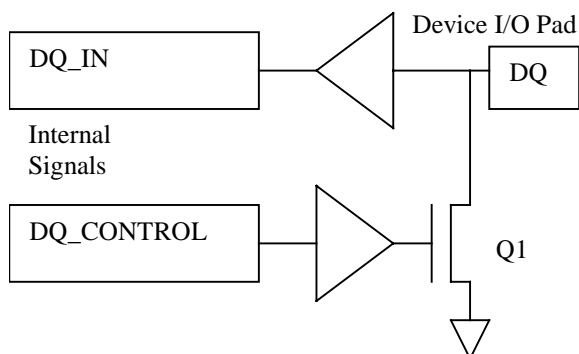


Figure 1. DQ Pad Driver (`one_wire_io`)

### LIBRARIES

To compile the Verilog source no external libraries are required. The VHDL source version requires both `IEEE.std_logic_1164` and `work.std_arith` libraries.

### CONNECTIONS

The following table lists the wires that needed to be connected for proper operation of the 1-Wire Master.

PIN	OPERATION
DQ	Open Drain Bi-directional 1-Wire Bus Connection
DATA	Bi-directional 8 Bit Data Bus
ADDRESS	3 Bit Address Bus
ADS_bar	Address Strobe
EN_bar	Instance Enable
RD_bar	Read Data Strobe
WR_bar	Write Data Strobe
INTR	Interrupt Detection
CLK	System Clock
MR	Mater Reset

If no address strobe is available in the system, the `ADS_bar` may be tied low making the address latch transparent. The `EN_bar` signal should be generated by address decode logic external to the 1WMaster module. If the 1WM is the only instance on the data bus, `EN_bar` may be tied low. The system clock wired to `CLK` must be between

3.2 and 128 MHz. For detailed operation of all connections see the [2] DS1WM 1-Wire Master datasheet.

## INSTANCE

The following is an example of how to create a 1-Wire Master instance in Verilog.

```
module DS89C200 (...top level list...);

wire [7:0] DB;
wire [2:0] ADDR;
wire sysclk, read_bar,
      write_bar, master_reset,
      interrupt, addr_strobe;
wire DQ_OUT;

supply1 Tie1;
supply0 Tie0;

cpu xcpu(.CLK(sysclk),
        .DB(DB),
        .EXTRD_BAR(read_bar),
        .EXTWR_BAR(write_bar),
        .EXTADDR(ADDR),
        .RESET(master_reset),
        .EXTINTR(interrupt),
        .ADDR_ST(addr_strobe),
        ... other I/O signals ...);

onewiremaster xonewiremaster(
    .ADDRESS(ADDR),
    .ADS_bar(addr_strobe),
    .EN_bar(Tie0),
    .RD_bar(read_bar),
    .WR_bar(write_bar),
    .DATA(DB),
    .INTR(interrupt),
    .CLK(sysclk),
    .DQ(DQ_OUT),
    .MR(master_reset) );

... rest of design ...
```

All signals generated by xcpu meet the 1-Wire Master timing requirements. The EN\_bar signal is tied low because there is no other addressable logic on the data bus. The DQ\_OUT signal is wired directly to an I/O pad.

## SYNTHESIS

Synthesis of this design is very straightforward. A bottom up approach is recommended compiling the individual submodules individually and afterwards optionally compiling

the top level. Timing constraints need to be placed on the clk\_1us signal along with sysclk signal. Further timing constraints may be necessary for some of the asynchronous control signals such as WR\_bar, RD\_bar, EN\_bar ADS\_bar and MR. Additional constraints may be necessary for clk\_1us to keep buffers from being inserted on the clock signal. In most cases will be necessary to have strategy for clock distribution such as a clock tree.

Included with the source code are example synthesis scripts and Makefile to be used with Synopsys design compiler. To use these it is necessary to create a .synopsys\_dc.setup file that defines the target synthesis library. In addition, it is necessary to modify the included environment file (named "environment") to specify the device from the target library to be used for specifying output drive strengths and input loads. These example scripts are very generic. The actual scripts and constraint files would be generated by the engineer to meet the timing requirements of the specific design. One thing to keep in mind is that the timing in the 1-Wire Master block is not entirely synchronous by design. The DQ output is synchronized to CLK, but the bus read/write timing will only be synchronous to CLK if the CPU uses CLK to generate RD\_bar, WR\_bar and ADS\_bar. See the specification for the timing relationships for these signals.

This example design is fully self contained. It has been successfully compiled to FPGA and ASIC targets with success. When synthesized to a typical ASIC target library, the design uses about 110 flip-flops, 3 latches, and a total of 1492 gates.

## REFERENCES:

- [1] **Book of iButton Standards**, Dallas Semiconductor, online at <http://www.ibutton.com/iButtons/standard.pdf>
- [2] **DS1WM Datasheet**, Dallas Semiconductor, online at <http://www.dalsemi.com/DocControl/PDFs/1WM.pdf>