Lista rozkazów mikrokomputerów jednoukładowych serii MCS51

kod mnemoniczny	**kod dwójkowy**	**B/C**	**operacja**
operacje arytmetyczne			
ADD A, R_n	00101rrr	1/1	A←A + R_n
ADD A, adr8	00100101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←A + M[adr8]
ADD A, @R_i	0010011i	1/1	A←A + M[R_i]
ADD A, #n	00100100 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←A + m[PC + 1]
ADDC A, R_n	00111rrr	1/1	A←A + R_n + C
ADDC A, adr8	00110101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←A + M[adr8] + C
ADDC A, @R_1	0011011i	1/1	A←A + M[R_i] + C
ADDC A, #n	00110100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	A←A + m[PC + 1] + C
SUBB A, R_n	10011rrr	1/1	A←A – C - R_n
SUBB A, adr8	10010101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←A - C - M[adr8]
SUBB A, @R_i	1001011i	1/1	A←A - C - M.[R_i]
SUBB A, #n	10010100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	A←A - C - m[PC + 1]
INC A	00000100	1/1	A←A + 1
INC R_n	00001rrr	1/1	R_n←R_n + 1
INC adr8	00000101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[adr8]←M[adr8] + 1
INC @R_i	0000011i	1/1	M[R_i]←M[R_i] + 1
INC DPTR	10100011	1/2	DPTR←DPTR + 1
DEC A	00010100	1/1	A←A – 1

DEC R_n	00011rrr	1/1	$R_n \leftarrow R_n - 1$
DEC adr8	00010101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[adr8]←M[adr8] - 1
DEC @R_i	0001011i	1/1	$M[R_i] \leftarrow M[R_i] - 1$
MUL AB	10100100	1/4	$\underline{B} \square \underline{A} \leftarrow \underline{A \bullet B}$
DIV AB	10000100 $a_7a_6a_5a_4a_3a_2a_1a_0$	1/4	A□B←A / B {A←wynik, B←reszta}
DA A	11010100	1/1	korekcja dziesiętna A
operacje logiczne na bajtach			
ANL A, R_n	01011rrr	1/1	$A \leftarrow A \wedge R_n$
ANL A, adr8	01010101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	$A \leftarrow A \wedge M[adr8]$
ANL A, @R_i	0101011i	1/1	$A \leftarrow A \wedge M[R_i]$
ANL A, #n	01010100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	$A \leftarrow A \wedge m[PC + 1]$
ANL adr8, A	01010010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	$M[adr8] \leftarrow M[adr8] \wedge A$
ANL adr8, #n	01010011 $a_7a_6a_5a_4a_3a_2a_1a_0$ $n_7n_6n_5n_4n_3n_2n_1n_0$	3/2	$M[adr8] \leftarrow M[adr8] \wedge m[PC + 2]$
ORL A, R_n	01001rrr	1/1	$A \leftarrow A \vee R_n$
ORL A, adr8	01000101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	$A \leftarrow A \wedge M[adr8]$
ORL A, @R_i	0100011i	1/1	$A \leftarrow A \vee M[R_i]$
ORL A, #n	01000100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	$A \leftarrow A \vee m[PC + 1]$
ORL adr8, A	01000010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	$M[adr8] \leftarrow M[adr8] \vee A$

ORL adr8, #n	01000011 $a_7a_6a_5a_4a_3a_2a_1a_0$ $n_7n_6n_5n_4n_3n_2n_1n_0$	3/2	M[adr8]←M[adr8] ∨ m[PC + 2]
XRL A, R_n	01101rrr	1/1	A←A ⊕ M[R_n]
XRL A, adr8	01100101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←A ⊕ M[adr8]
XRL A, @R_i	0110011i	1/1	A←A ⊕ M[R_i]
XRL A, #n	01100100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	A←A ⊕ m[PC + 1]
XRL adr8, A	01100010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[adr8]←M[adr8] ⊕ A
XRL adr8, #n	01100011 $a_7a_6a_5a_4a_3a_2a_1a_0$ $n_7n_6n_5n_4n_3n_2n_1n_0$	3/2	M[adr8]←M[adr8] ⊕ m[PC + 2]
CRL A	11100100	1/1	A←0
CPL A	11110100	1/1	A←A\
RL A	00100011	1/1	A< 7:0 >←A< 6:0 >□A< 7 >
RLC A	00110011	1/1	C□A< 7:0 >←A< 7:0 >□C
RR A	00000011	1/1	A< 7:0 >←A< 0 >□A< 7:1 >
RRC A	00010011	1/1	A< 7:0 >□C←C□A< 7:0 >
SWAP A	11000100	1/1	A< 3:0 >↔A< 7:4 >
operacje przesłań			
MOV A, R_n	11101rrr	1/1	A←R_n
MOV A, adr8	11100101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	A←M[adr8]
MOV A, @R_i	1110011i	1/1	A←M[R_i]
MOV A, #n	01110100 $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	A←m[PC + 1]
MOV R_n, A	11111rrr	1/1	R_n←A

MOV $R_{n,}$ adr8	10101rrr $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	R_n←M[adr8]
MOV $R_{n,}$ #n	01111rrr $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	R_n←m[PC + 1]
MOV adr8, A	11110101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[adr8]←A
MOV adr8, R_n	10001rrr $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	M[adr8]←R_n
MOV adr8d, adr8s	10000101 $(a_7a_6a_5a_4a_3a_2a_1a_0)$s $(a_7a_6a_5a_4a_3a_2a_1a_0)$d	3/2	M[adr8d]←M[adr8s]
MOV adr8, @R_i	1000011i $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	M[adr8]←M[R_i]
MOV adr8, #n	01110101 $a_7a_6a_5a_4a_3a_2a_1a_0$ $n_7n_6n_5n_4n_3n_2n_1n_0$	3/2	M[adr8d]←m[PC + 2]
MOV @$R_{i,}$ A	1111011i	1/1	M[R_i]←A
MOV @R_i, adr8	1010011i $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	M[R_i]←M[adr8]
MOV @R_i, #n	0111011i $n_7n_6n_5n_4n_3n_2n_1n_0$	2/1	M[R_i]←m[PC + 1]
MOV DPTR, #nn	10010000 $n_{15}n_{14}n_{13}n_{12}n_{11}n_{10}n_9n_8$ $n_7n_6n_5n_4n_3n_2n_1n_0$	3/2	DPH□DPL←m[PC + 1]□ m[PC + 2]
MOVC A, @A + DPTR	10010011	1/2	A←m[A + DPTR]
MOVC A, @A + PC	10000011	1/2	PC←PC + 1 A←m[A + PC]
MOVX A, @R_i	11100011	1/2	A←M[R_i]
MOVX A, @DPTR	11100000	1/2	A←M[DPTR]
MOVX @R_i, A	1111001i	1/2	M[R_i]←A
MOVX @ DPTR, A	11110000	1/2	M[DPTR]←A

PUSH adr8	11000000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	SP←SP + 1 M[SP]←M[adr8]
POP adr8	11010000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	M[adr8]←M[SP] SP←SP - 1
XCH A, R_n	11001rrr	1/1	$\underline{A \leftrightarrow R_n}$
XCH A, adr8	11000101 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M↔M[adr8]
XCH A, @R_i	1100011i	1/1	A↔M[R_i]
XCHD A, @R_i	1101011i	1/1	A< 3:0 >↔M[R_i]< 3:0 >
operacje na bitach			
CLR C	11000011	1/1	C←0
CLR bit	11000010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[bit]←0
SETB C	11010011	1/1	C←1
SETB bit	11010010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[bit]←1
CPL C	10110011	1/1	C←C\
CPL bit	10110010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	M[bit]← M[bit]\
ANL C, bit	10000010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	C←C ∧ M[bit]
ANL C, bit\	10110000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	C←C ∧ M[bit]\
ORL C, bit	01110010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	C←C ∨ M[bit]
ORL C, bit\	10100000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	C←C ∨ M[bit]\
MOV C, bit	10100010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/1	C←M[bit]

MOV bit, C	10010010 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	M[bit]←C
JC rel	01000000 $d_7d_6d_5d_4d_3d_2d_1d_0$	2/2	PC←PC + 2 if C = 1 then PC←PC + rel
JNC rel	01010000 $d_7d_6d_5d_4d_3d_2d_1d_0$	2/2	PC←PC + 2 if C = 0 then PC←PC + rel
JB bit, rel	00100000 $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if M[bit] = 1 then PC←PC + rel
JNB bit, rel	00110000 $a_7a_6a_5a_4a_3a_2a_1a_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if M[bit] = 0 then PC←PC + rel
JBC bit, rel	00010000 $a_7a_6a_5a_4a_3a_2a_1a_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if M[bit] = 1 then M[bit]←0 PC←PC + rel
rozkazy skoków i rozkazy sterujące			
ACALL adr11	$a_{10}a_9a_8$10001 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	PC←PC + 2 SP←SP + 1 M[SP]←PC < 7:0 > SP←SP + 1 M[SP]←PC < 15:8 > PC < 10:0 >←adr11
LCALL adr16	00010010 $a_{15}a_{14}a_{13}a_{12}a_{11}a_{10}a_9a_8$ $a_7a_6a_5a_4a_3a_2a_1a_0$	3/2	PC←PC + 3 SP←SP + 1 M[SP]←PC < 7:0 > SP←SP + 1 M[SP]←PC < 15:8 > PC←adr16
RET	00100010	1/2	PC < 15:8 >←M.[SP] SP←SP - 1 PC < 7:0 >←M.[SP] SP←SP - 1

RET1	00110010	1/2	PC < 15:8 >←M[SP] SP←SP - 1 PC < 7:0 >←M[SP] SP←SP - 1 rozkaz ten odtwarza również stan priorytetów przerwań
AJMP adr11	$a_{10}a_9a_8$00001 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	PC←PC + 2 PC < 10:0 >←adr11
LJMP adr16	00000010 $a_{15}a_{14}a_{13}a_{12}a_{11}a_{10}a_9a_8$ $a_7a_6a_5a_4a_3a_2a_1a_0$	3/2	PC←PC + 3 PC←adr16
SJMP rel	10000000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	PC←PC + 2 PC←PC + rel
JMP @A + DPTR	01110011	1/2	PC←A + DPTR
JZ rel	01100000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	PC←PC + 2 if A = 0 then PC←PC + rel
JNZ rel	01110000 $a_7a_6a_5a_4a_3a_2a_1a_0$	2/2	PC←PC + 2 if A ≠ 0 then PC←PC + rel
CJNE A, adr8, rel	10110101 $a_7a_6a_5a_4a_3a_2a_1a_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if M[adr8] < A then PC←PC + rel and C←0 or, if M[adr8] > A then PC←PC + rel and C←1
CJNE A, #n, rel	10110100 $n_7n_6n_5n_4n_3n_2n_1n_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if #n < A then PC←PC + rel and C←0 or, if #n > A then PC←PC + rel and C←1
CJNE R_n, #n, rel	10111rrr $n_7n_6n_5n_4n_3n_2n_1n_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if #n < R_n then PC←PC + rel and C←0 or, if #n > R_n then PC←PC + rel and C←1
CJNE @R_i, #n, rel	1011011i $n_7n_6n_5n_4n_3n_2n_1n_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 3 if #n < M[R_i] then PC←PC + rel and C←0 or, if #n > M[R_i] then PC←PC + rel and C←1
DJNZ R_n, rel	11011rrr $d_7d_6d_5d_4d_3d_2d_1d_0$	2/2	PC←PC + 2 R_n← R_n - 1 if R_n < > 0 then PC←PC + rel

DJNZ adr8, rel	11010101 $a_7a_6a_5a_4a_3a_2a_1a_0$ $d_7d_6d_5d_4d_3d_2d_1d_0$	3/2	PC←PC + 2 M[adr8]← M[adr8] - 1 if M[adr8] < > 0 then PC←PC + rel
NOP	00000000	1/1	PC←PC + 1

M – pamięć danych lub SFR
m – pamięć programu

Rozkazy ustawiające znaczniki w MCS51

rozkazy ustawiające znaczniki			
rozkaz	**C**	**AC**	**OV**
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0		X
DIV	0		X
DA	X		
RRC	X		
RLC	X		
SETB C	1		
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, bit\	X		
ORL C, bit	X		
ORL C, bit\	X		
MOV C, bit	X		
CJNE	X		

X – znacznik ustawiany zgodnie z wynikiem operacji